ARMY TM 11-5895-490-35
NAVY NAVAIR 16-30APX72-2
NAVY NAVSHIPS 0967-217-4020
AIR FORCE TO 12P4-2APX72-2

INTERMEDIATE AND DIRECT/GENERAL SUPPORT

MAINTENANCE WITH DEPOT OVERHAUL INSTRUCTIONS

RECEIVER-TRANSMITTER, RADIO RT-859/APX-72, RT-859A/APX-72 AND MOUNTINGS MT-3809/APX-72, MT-3948/APX-72

This copy is a reprint which includes current pages from Change 1

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

DECEMBER 1977

NAVAIR 16-30APX72-2
NAVSHIPS 0967-217-4020
TM 11-5895-490-35
T.O. 12P4-2APX72-2

Technical Manual

Intermediate and Direct/General Support Maintenance with Depot Overhaul Instructions

RECEIVER-TRANSMITTER, RADIO RT-859/APX-72, RT-859A/APX-72 AND MOUNTINGS MT-3809/APX-72, MT-3948/APX-72

Hazeltine Corporation
N00019-74-C-0469
N00383-81-C-0117

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1 December 1977
Change 1 - 15 September 1981

LIST OF EFFECTIVE PAGES

Insert latestchanged pages; dispose of superseded pages in accordance with applicable regulations.

Note: On a changed page, the portion of the text affected by the latest change is indicated by a vertical line, or other change symbols, in the outer margin of the page.

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REPORTING OF ERRORS

You can improve this manual by recommending improvements using DA Form 2028-2 located in the back of the manual. Simply tear out the self-addressed form, fill it out as shown on the sample, fold it where shown, and drop it in the mail.

If there are no blank DA Form 2028-2 in the back of your manual, use the standard DA Form 2028 (Recommended Changes to Publications and Blank Forms) and forward to the Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703.

In either case, a reply will be furnished direct to you.

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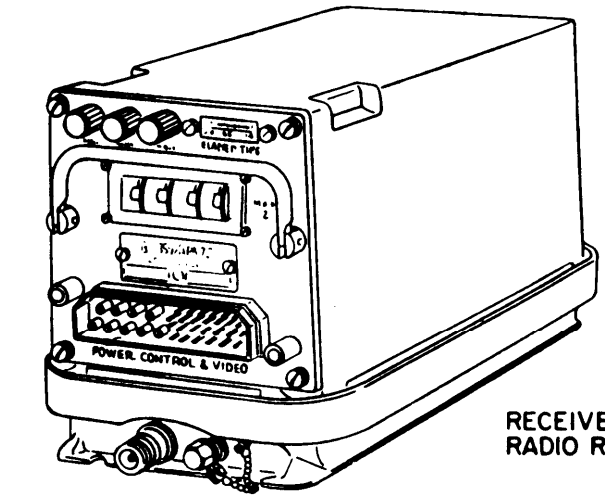
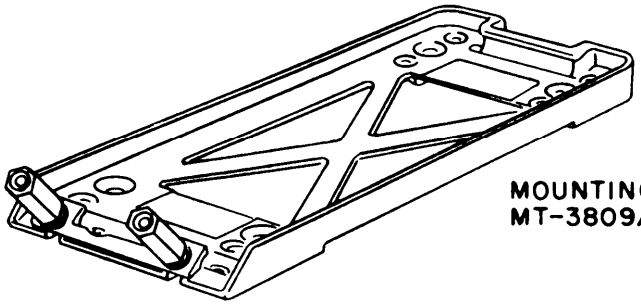
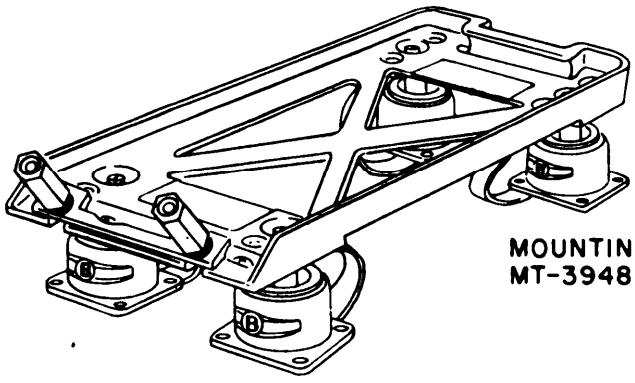


RECEIVER-TRANSMITTER,
RADIO RT-859/APX-72



MOUNTING
MT-3809/APX-72



MOUNTING
MT-3948/APX-72

Figure 1-1. Receiver-Transmitter, Radio RT-859/APX-72 and Mountings MT-3809/APX-72 and MT-3948/APX-72

SECTION I

INTRODUCTION

1-1. NOMENCLATURE AND DESIGNATION OF EQUIPMENT.

1-2. Receiver-Transmitter, Radio RT-859/APX-72 or RT-859AIAPX-72, and Mountings MT-3809/APX-72 and MT-3948/APX-72 (hereinafter referred to as RT-859/APX-72 and RT-859A/APX-72, or (receiver-transmitter, if applicable to both) MT-3809/APX-72, and MT-39481APX-72, respectively), see figure 1-1. RT-859/APX-72 and early versions of RT-859A/APX-72 were manufactured by The Bendix, Honeywell, Wilcox, and Melpar Corporations. Improved models of RT-859A/APX-72 are manufactured by Hazeltine Corporation, Cuba Hill Road, Greenlawn, New York, 11740.

1-3. PURPOSE OF MANUAL.

1-4. The purpose of this manual is to provide information which will enable the performance of intermediate and direct/general support maintenance and depot (overhaul) maintenance on this equipment.

1-5. SCOPE OF MANUAL.

1-6. Sections I through VI of this manual contain procedures for intermediate maintenance and for depot (overhaul) maintenance for the receiver-transmitter, MT 3809/APX-72, and MT 39481APX-72. The scope of intermediate and depot maintenance, as defined by the Department of Defense (DOD), follows:

a. Intermediate maintenance is that maintenance which is the responsibility of and formed by designated maintenance activities for direct support of using organizations; its phases normally consist of calibration, repair or replacement of damaged or unserviceable parts, components, or assemblies; the emergency manufacture of non-available parts; and providing technical. assistance to using organizations. Intermediate maintenance is normally accomplished in fixed or mobile shops, tenders, or shore based repair facilities. The Department of Defense (DOD) term “Intermediate Maintenance” encompasses the Military Services’ maintenance terms of field, minor modification, upkeep, voyage repairs, restricted availability, shops C and D, third and fourth echelon, and direct and general support.

b. Depot maintenance is that maintenance which is the responsibility of and performed by designated maintenance activities, to augment stocks of serviceable material, and to support Organizational Maintenance and Intermediate Maintenance activities by the use of more extensive shop facilities, equipment, and personnel of higher technical skill than are available at the lower levels of maintenance. Its phases normally consist of repair, modification, alteration, modernization, overhaul, reclamation, or rebuilt parts, assemblies, subassemblies, components, and end items; the emergency manufacture of non-available parts; and providlng technical assistance to using activities and intermediate maintenance organizations. Depot maintenance is normally accomplished in fixed shops,

shipyards, and shore-based facilities. The DOD term "Depot Maintenance" encompasses the Military Services' maintenance terms of rehabilitation, depot, fifth echelon, NARF, regular overhaul, restricted availability, and shops A and B.

1-7. The technical manuals applicable to this equipment by the three services are:

Navy	- NAVAIR 16-30 APX72-2 and -3
	- NAVESHIPS 0967-217-4010, 4020, and 4030
Army	- TM 11-5895-490-20, -20P, -35, and -35P
Air Force	- T.O. 12P4-2APX72-2 and -4.

1-8. ARRANGEMENT AND HOW TO USE MANUAL .

1-9. This manual is divided into sections, each of which contains defined information related to the receiver-transmitter, MT-3809\ APX-72, and MT-39481APX-72.

a. The front matter contains the A page for recording manual changes and Table of Contents.

b. Section I contains an introduction to the publications prepared for and their relation to the receiver-transmitter MT-3809/ APX-72, and MT-39481APX-72.

c. Section II contains the physical and functional description of the receiver-transmitter, MT-3809/APX-72, and MT-3948/APX-72 and principles of operation relative to both system and equipment operation.

d. Section III provides maintenance information for Special Support Equipment (Aerospace Ground Equipment).

e. Section IV contains the intermediate maintenance procedures established for checkout, troubleshooting, repair, test, alignment, and adjustment of the receiver-transmitter.

f. Section V contains the depot maintenance procedures established for repair and overhaul of the receiver-transmitter. Procedures described in Section IV, applicable also to intermediate maintenance, are not repeated in this section except by reference.

g. Section VI contains the schematic and wiring diagrams.

h. An alphabetical index is provided at the back of this manual. This index will enable the user of this manual to locate — information more readily.

1-10. INDEX OF PUBLICATIONS.

1-11. Refer to List of Applicable Change Directives and the latest issue of NAVSUP-2002, section viii (Navy), DA PAM 310-1 (Army) , and T.O. 0-1-12 (Air Force) to determine where there are new editions, changes or additional publications pertaining to the equipment. The cited publications are a current index of technical bulletins, technical manuals, technical orders, illustrated parts breakdown, supply bulletins, supply manuals, lubrication orders, and modification work orders available through publication supply channels. The index lists the individual manual parts and the latest changes and revisions of each equipment publication.

1-12. FORMS AND RECORDS.

1-13. REPORTS OF MAINTENANCE AND UNSATISFACTORY EQUIPMENT. To prepare these reports, use equipment forms and records in accordance with instructions in NAVWEPS Form 13070/5 (Navy), TM38-750 (Army), and AFTO Form 29129A (Air Force).

1-14. REPORTS OF DAMAGED OR IMPROPER SHIPMENT. Fill out and forward DD Form 6 (Report of Damaged or Improper Shipment) as prescribed in NAVSANDA Publications 378 (Navy), AR 700-58 (Army) and AFR 71-4 (Air Force) .

1-15. DISCREPANCY IN SHIPMENT REPORT (DISREP) (SF361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF361) as prescribed in NAVSUP Pub. 459 (Navy), AR55-38 (Army), or AFM 75-34 (Air Force).

1-16. REPORTING OF EQUIPMENT MANUAL IMPROVEMENTS. Reports of errors, omissions, and recommendations for improving this manual by the individual user is encouraged. Reports should be submitted on OPNAV Form 4790/47, (Navy), DA Form 2028 (Army), and AFTO Form 22 (Air Force) . DA Form 2028 will be forwarded directly to Commanding General, U.S. Army Electronics Command, ATTN: DRSEL-MA-PSA, Fort Monmouth, New Jersey 07703.

LIST OF APPLICABLE CHANGE DIRECTIVES

(Avionic Change, Modification Work Order, Time Compliance Technical Order)

IDENTIFICATION NUMBER	DATE	TITLE	CHANGE/REV/ SUPPL DATE
AC 827	1 Jul 68	Receiver-Transmitter, Radio RT-859/APX-72, RF Section, modification of (ECP 020 R)	
AC 841 MWO 11-5895-490-40/1 T.O. 12P4-2APX72-503	1 Apr 70 21 Aug 70 8 Jul 70	Receiver-Transmitter, Radio RT-859/APX-72, RF Section, modification of (ECP 023 CCR2)	
AC 916 MWO 11-5895-490-40/1 T.O. 12P4-2APX72-502	28 Mar 69 21 Aug 70 8 July 70	Receiver-Transmitter, Radio RT-859/APx-72, Mode 4 Caution Light and Reply Light Improper Operation (ECP 022 CCR2)	
AC 917 MWO 11-5895-490-40/1 T.O. 12P4-2APX72-504	28 Mar 69 21 Aug 70 8 JULY 70	Receiver-Transmitter, Radio RT-8591APX-72, Wide Pulse Rejection Improvement (ECP 024 CCR2)	
AC 915 MWO 11-5895-490-40/1 T.O. 12P4-2APX72-501	15 Mar 69 21 Aug 70 8 July 70	Receiver-Transmitter, Radio RT-8591APX-72, Processor Assembly (ECP 021 CCR2)	
AC 992 MWO 11-5895-490-40/1 T.O. 12P4-2APX72-505	1 Apr 70 21 Aug 70 8 July 70	Receiver-Transmitter, Radio RT-8591APX-7.2, Modulator Trigger Modification (ECP 033 CCR)	
AC 993 MWO 11-5895-490-40/1 T.O. 12P4-2APX72-506	1 Apr 70 21 Aug 70 8 July 70	Receiver-Transmitter, Radio RT-8591APX-72, Encoder Clock Pulsing (ECP 049 CCR)	
AC 1143	16 Feb 70	Receiver-Transmitter, Radio RT-859/APX-72, Card Cage AOC Improvement (ECP 051 CCR)	15 Sep 70
AC 1144	16 Feb 70	Receiver-Transmitter, Radio RT-859/APX-72, Range Jitter Reduction (ECP 052 CC)	15 Sep 70
AC 1267 MWO 11-5845-490-40/2 T.O. 12P4-2APx72-507	13 July 72 14 June 72 30 Sep 72	Receiver-Transmitter, Radio RT-859AIAPX-72, Mode 4 Interface Compatibility Modification (ECP 055R1, ECP 056)	1 Apr 71
AC		Receiver-Transmitter, Radio RT-859A/APX-72, Compatibility with Mode 4 Computer.	

SECTION II

GENERAL DESCRIPTION

2-1. PHYSICAL DESCRIPTION.

NOTE

Unless specifically noted, all text applies to both the RT-859/APX-72 and the RT-859A/APX- 72

2-2. RECEIVER-TRANSMITTER, RADIO RT-859/APX-72, RT-859A/APX-72. The RT-859/APX-72 or RT-859A/APX-72 (figure 2-1) is encased in a two-section housing which may be pressurized. The only difference in the outward appearance between the two receiver-transmitters is the nameplate. A silicon rubber O-ring serves as a pressure seal between the two sections, which are joined together by an encircling flange coupler with clamp. The overall dimensions are 6 by 12.25 by 5.76 inches and the weight is 15 pounds. The upper section contains the digital circuitry printed circuit boards and a plug-in power supply. A front panel, containing three fuseholders, the mode 2 switch assembly, the power and control connector, an elapsed time meter, and a folding handle, is fastened to the upper section of the housing. The lower section of the housing contains the rf and video circuit components, the antenna connector, and the pressurization

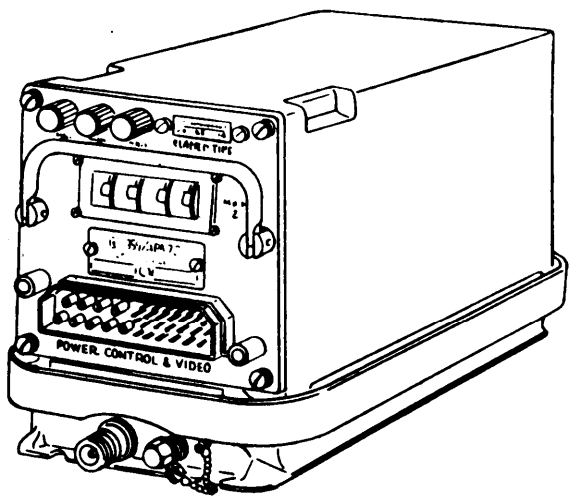


Figure 2-1. Receiver-Transmitter, Radio RT-859/APX-72 or RT-859A/APX-72.

valve. An rf electrical shield covers the subassemblies in the lower section to prevent interaction of stray electric fields between the components of the upper and lower sections. The lower section of the housing is provided with exterior protrusions which mate with cavities on the mounting frame. Table 2-1 lists the components and circuitboard assemblies comprising the receiver-transmitter.

2-3. MOUNTING MT-3809/APX-72. The MT-3809/APX-72 (figure 2-2) mount is constructed of cast aluminum measuring 0.81 by 12.4 by 5.06 inches and weighs 1.50 pounds. The MT-3809/APX-72 is a hard-type mount with a cavity in the rear frame into which the protruding lip of the receiver-transmitter is placed, and two self-locking screw fasteners at the front of the mount which fasten down on the front protrusions of the receiver-transmitter.

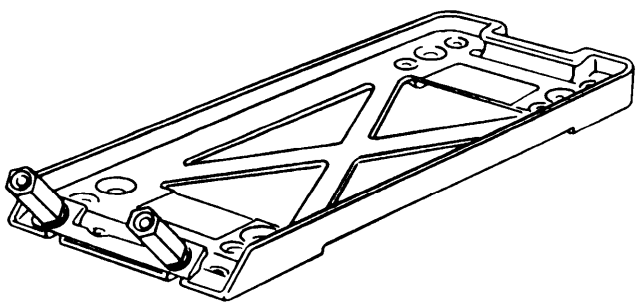


Figure 2-2. Mounting MT-3809/APX-72

2-4. MOUNTING MT-3948/APX-72. The MT-3948/APX-72 (figure 2-3) mount is physically the same as the MT-3809/APX-72, but provides for the addition of four isolator mounts and four ground straps positioned at the four corners of the MT-3948/APX-72 mount.

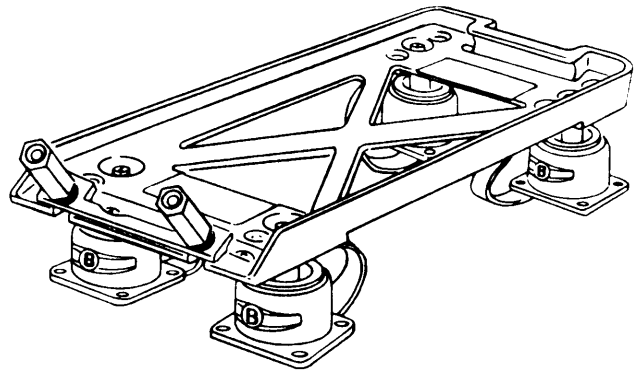


Figure 2-3. Mounting MT-3948/APX-72

2-5, AUXILIARY EQUIPMENT. The following equipment is not supplied as part of the RT-859/APX-72 or RT-859A/APX-72, but is required for partial or full operation of the transponder system. Refer to the Organizational Maintenance Manual for the RT-859/APX-72 (NAVSHIPS 0967-217-410, TM11-5895-490-20), and other manuals referenced therein for information about the auxiliary equipment.

a. Antenna AT-884/APX or equivalent.

b. Control, Transponder Set C-6280(P)/APX.

c. Computer KIT-1A/TSEC or equivalent.

d. Pressure Altitude Digitizer CPU-66\A or equivalent.

Test Set, Transponder Set TS-1843A/APX.

f. Primary Power 27.5 vdc or 27.5 vdc and 115 vac 400 Hertz.

g. Interconnecting cables.

Table 2-1. Components and Circuitboard Assemblies

QTY	NOMENCLATURE	REFERENCE DESIGNATOR	COLOR CODE	CHASSIS CONNECTOR
1	Receiver-Transmitter			
1	Diplexer			
1	Modulator	A7		
1	Sensitivity	A8		
1	Amplifier	AR1		
1	Power Amplifier	AR2		
1	Detector and Video Amplifier	AR3		
1	Preselector	Z1		
1	Oscillator	Z2		
1	Low Pass Filter	Z3		
1	Processor	A1	BRN	XA1P1
1	Decoder	A2	ORN	XA2P1
1	Mode 4	A3	YEL	XA3P1
1	Encoder Clock	A4	GRN	XA4P1
1	Encoder Control	A5	BLU	XA5P1
1	Encoder Gating	A6	VIO	XA6P1
1	Delay Line	DL1	RED	XDL1P1
1	Power Supply	PS1		XPS1P1, P2

2-6. FUNCTIONAL DESCRIPTION.

2-7. RECEIVER-TRANSMITTER, RADIO RT-859/APX-72, RT-859A/APX-72. The receiver-transmitter, when used with auxiliary equipment listed in paragraph 2-5, provides automatic radar identification, identification of position, emergency signals, and altitude reporting of the craft on which it is located to all suitably equipped interrogating facilities within the operational range of the system. The receiver-transmitter receives, decodes, and replies to the characteristic interrogations of operational modes 1, 2, 3/A, C, and 4. Specially coded identification of position (I/P) and emergency signals can be transmitted to interrogating stations

when conditions warrant. Slight modifications to the equipment will also provide a special position identification pulse (SPI) and a special (X-pulse) display in the reply signal train. The absence of auxiliary equipment, Computer KIT-1A/TSEC and Pressure Altitude Digitizer CPU-66/A, will not affect operation of the receiver-transmitter except in modes 4 and C.

2-8. INTERROGATION MODES AND CODES . The interrogation pulse characteristics for modes 1, 2, 3/A, C, test, and 4 are shown in figure 2-4. These pulses, transmitted at a frequency of 1030 MHz, are recognized by the receiver-transmitter through pulse width and spacing. Modes 1, 2, 3/A, C, and TEST each use two interrogation and one side lobe suppression pulse 0.8 ±0.1 us wide. Pulse spacings between the two interrogation pulses are:

Mode	Spacing
1	3 ±0.2 µs
2	5 ±0.2 µs
Test	6.5 ±0.2 µs
3/A	8 ±0.2 µs
C	21 ±0.2 µs

The side lobe suppression pulse for the above modes occurs 2 ±0.15 us after the leading edge of each initial pulse. Mode 4 interrogation pulse characteristics consist of four pulses 0.5 ±0.1 us wide, referenced from the first in multiples of 2 microseconds followed by as many as 33 additional pulses spaced in multiples of 1 microsecond. (A 1-microsecond spacing of pulses occurs only when the SLS pulse is present and is followed within 1 microsecond by another pulse (AII).) All others are spaced at least 2 microseconds leading edge to leading edge. The side lobe suppression pulse for mode 4 occupies the fifth. pulse position and is spaced 8 ±0.15 us from the leading edge of the first pulse.

2-9. NORMAL REPLY MODES AND CODES . The normal reply pulse characteristics for modes 1, 2, 3/A, TEST, and C are shown in figure 2-5. Mode 4 reply pulse characteristics are determined by an external computer. The reply information is transmitted by the receiver-transmitter at a frequency of 1091 MHz between two framing pulses spaced 20.3 ±0.05 us. The coded information between the two framing pulses is presented by the absence or presence of pulses at predetermined spacings. (In modes l, 2, and 3/A the absence or presence of information pulses at the predetermined spacings is determined by the mode code dial settings as shown in table 2-2. In mode C this information is determined by the Pressure Altitude Digitizer CPU-66/A and in mode 4 by the Computer KIT-1A/TSEC.) All reply pulses, framing, and information are 0.45 ±0.1 us wide.

a. Mode 1. For mode 1 a reply pulse train is transmitted containing from zero to a maximum of five information pulses plus two framing pulses. The information pulse spacing is in multiples of 2.9 ± 0.05 us from the initial framing pulse. The position where a sixth pulse would appear (17.4 ±0.05 us from the initial framing pulse) is not used. From the specified five information pulses, a total of 32 different codes are available.

b. Mode 2, 3/A, and Test. For modes 2, 3/A, and test, a reply pulse train is transmitted containing from zero to a maximum of 12 information pulses.

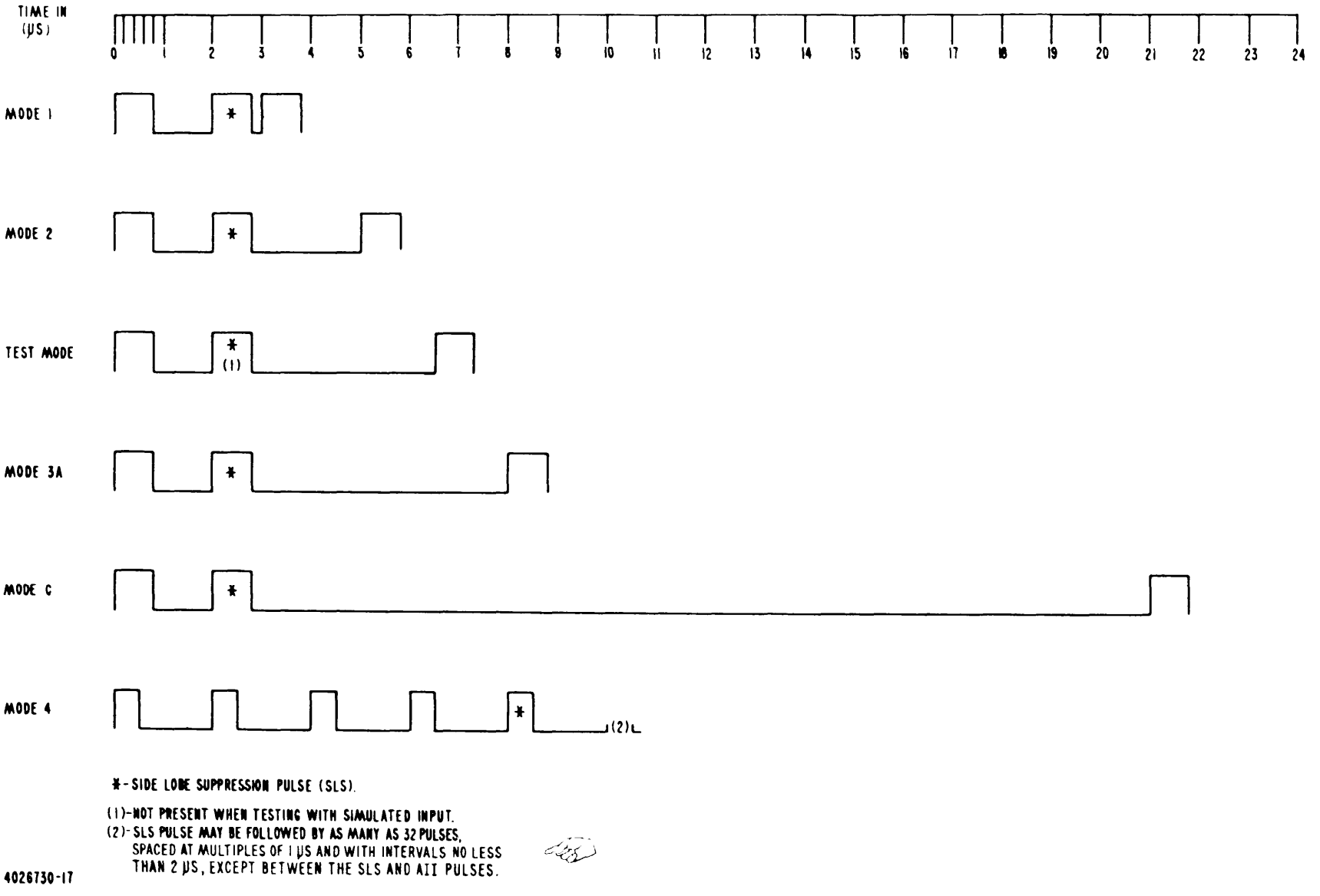
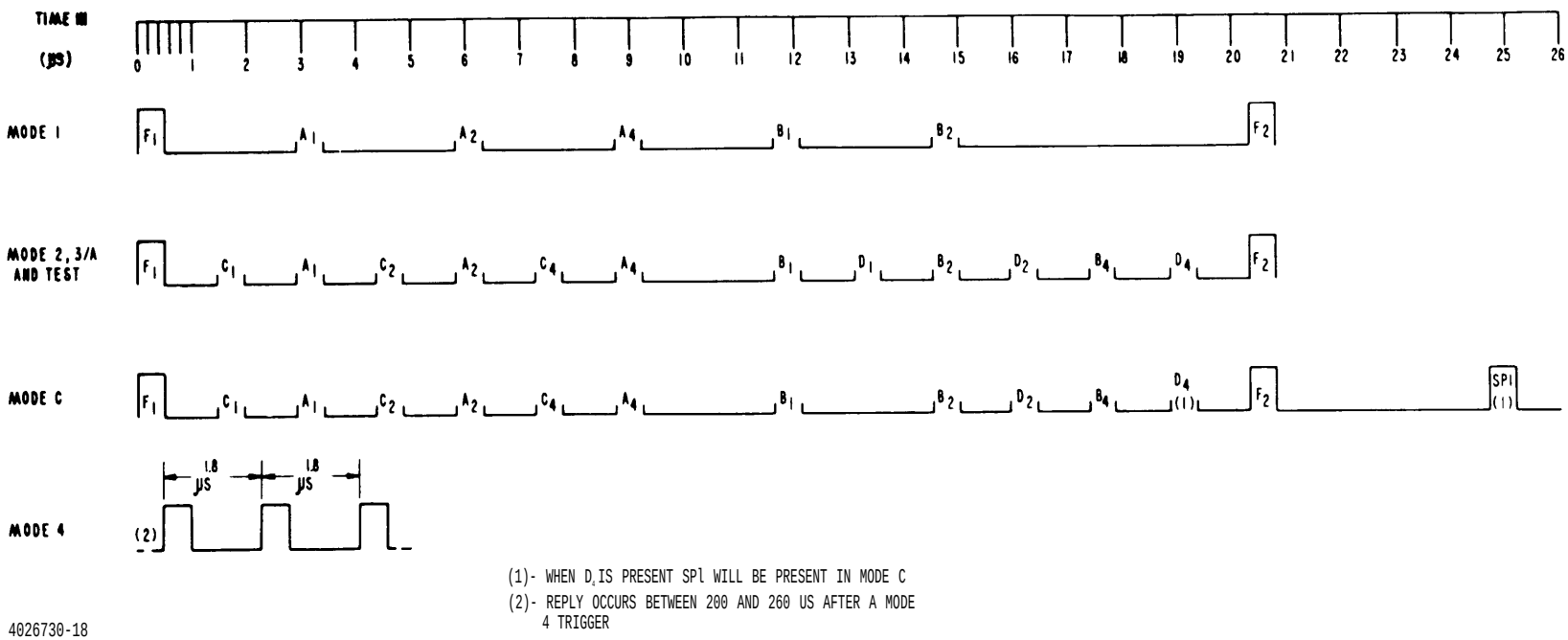


Figure. 2-4. Interrogation Pulse Characteristics



(1)- WHEN D_4 IS PRESENT SPI WILL BE PRESENT IN MODE C

(2)- REPLY OCCURS BETWEEN 200 AND 260 US AFTER A MODE 4 TRIGGER

Figure 2-5. Normal Reply Pulse Characteristics

Table 2-2. Correlation Dial Settings and Pulse Designations

DIAL NO.	PULSE DESIGNATIONS		
1	A_1	A_2	A_4
2	B_1	B_2	B_4
3	C_1	C_2	C_4
4	D_1	D_2	D_4
DIAL SETTING			
0	-	-	-
1	+	-	-
2	-	+	-
3	+	+	-
4	-	-	+
5	+	-	+
6	-	+	+
7	+	+	+

Note: + means presence of designated pulse
- means absence of designated pulse

The position of the above information in the reply pulse train are not in alphanumeric order except in mode 1. See figure 2-5.

plus two framing pulses. The information pulse spacing is in multiples of 1.45 ±0.05 us from the initial framing pulse. The position where a seventh pulse would appear (10.15 ±0.05 us from the initial framing pulse) is normally not used. Refer to paragraph 2-10d for information on use of the pulse position. From the specified 12 information pulses, a total of 4096 codes are available.

c. Mode C. For mode C, when an external pressure altitude digitizer is connected to the receiver-transmitter, a reply pulse train is transmitted containing from one to a maximum of 11 information pulses plus two framing pulses. The information pulse spacing is in multiples of 1.45 ±0.05 us from the initial framing pulse. The positions where a seventh pulse (10.15 ±0.05 ps from initial framing pulse) and a ninth pulse (13.05 ±0.05 us from initial framing pulse) would appear are not used. For RT-859/APX-72 only, whenever the thirteenth pulse position (18.85 ±0.05 us from initial framing pulse) is used, the Special Position Identification pulse (SPI) shall also be generated (24.65 ±0.05 us from initial framing pulse) at the output. Refer to paragraph 2-10C for information on the SPI pulse. The Mode C SPI pulse is not used in the RT-859A\APX-72. From the specified 11 information pulses, a total of 2048 codes are available. In the absence of a pressure altitude digitizer only framing pulses will be generated.

d. Mode 4. Mode 4 encoding is performed in an external computer.

2-10. SPECIAL REPLY FUNCTIONS.

NOTE

Any reference to the mode C SPI pulse applies for RT-859/APX-72 only.

The special reply pulse characteristics for modes 1, 2, 3/A, and C are shown in figure 2-6. Mode 4 is not affected by the special reply functions. The I/P function can be selected by the pilot for transmission for approximately 20-second intervals

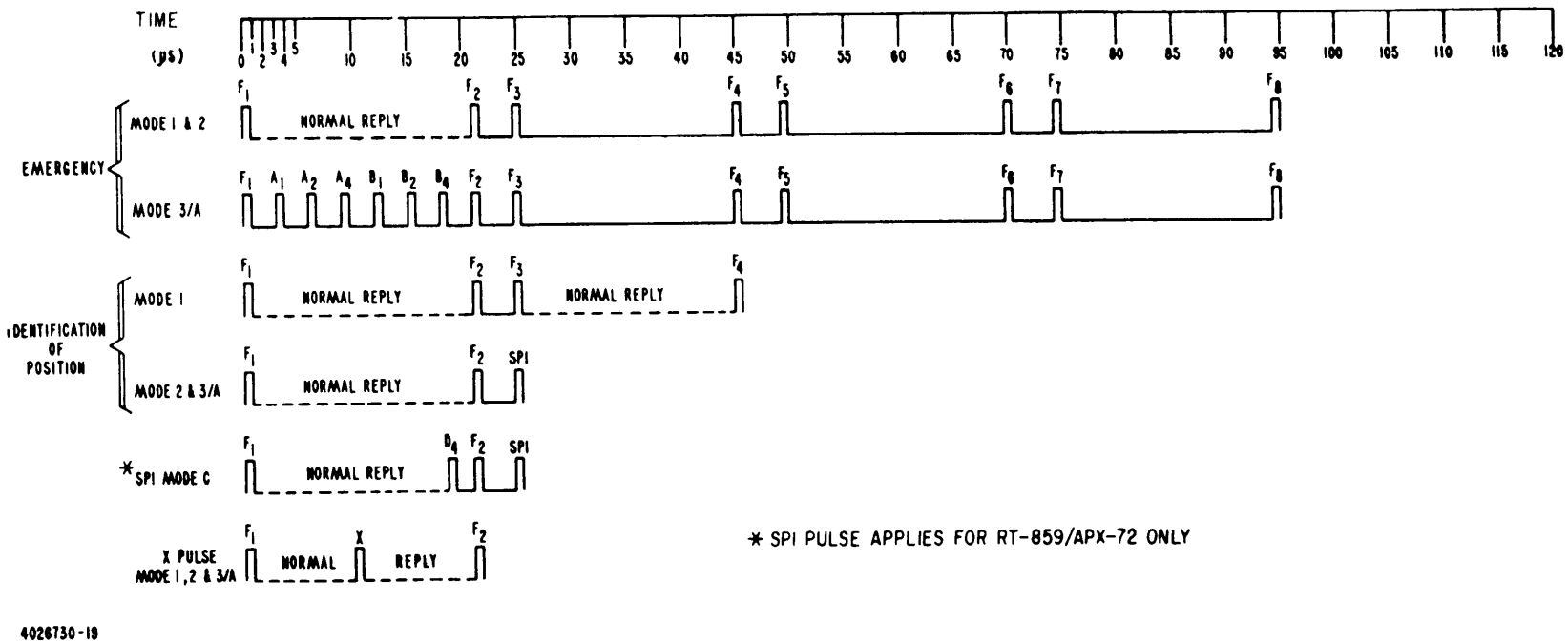


Figure 2-6. Special Reply Pulse Characteristics

and is used to distinguish between aircraft displaying identical coding. The emergency signal is selected by the pilot to indicate instance of an emergency condition in flight. The SPI pulse permits the air traffic controller to segregate aircraft above or below a given control altitude. The X-pulse permits identification of special aircraft such as drones.

Identification of Position (I/P). The I/P function affects operation in modes 1, 2, and 3/A. In mode 1, the reply pulse train containing the code in use is transmitted twice for each trigger pulse received. The second pulse train is spaced 24.65 ±0.05 us from the leading edge of the first framing pulse of the first train. In modes 2 and 3/A, the reply pulse train containing the code in use is transmitted once followed by a SPI pulse for each trigger pulse received. The SPI pulse is spaced 24.65 ±0.05 ps from the leading edge of the first framing pulse of the first train.

b. Emergency. The emergency function affects operation in modes 1, 2, and 3/A. In modes 1 and 2, the reply pulse train containing the code in use is transmitted once for each trigger pulse received followed by three sets of framing pulses, and no information pulses. The framing pulses will appear at 24.65 ±0.1, 44.95 ±0.15, 49.30 ±0.20, 69.60 ±0.25, 73.95 ±0.30, and 94.25 ±0.35 us. For each trigger pulse received in mode 3/A, one reply pulse train containing the code 7700 is transmitted followed by three sets of framing pulses, and no information pulses.

c. Special Position Idetification Pulse (SPI). The SPI or mode C caboose pulse (24.65 ±0.1 us from the initial framing pulse) is generted whenever a D4 pulse (18.85 ±0.05 us from the initial framing pulse) is used in a mode C reply. This pulse is actually the initial framing pulse of a second reply train, and is the same pulse used in the mode 2 and 3/A I/P function.

d. X-Pulse. The X-pulse (10.15 ±0.05 us from the initial framing pulse) appears in a. normally unused position. When the C-6280(P)\APX is modified by grounding a single external control lead, all replies in modes 1, 2, and 3/A will include this pulse in addition to the normal framing and information pulses.

2-11. BLOCK DIAGRAM ANALYSIS.

NOTE

Unless specifically noted, all text applies to both the RT-859/APX-72 and RT-859A/APX-72.

Figure 2-7 is a detailed block diagram of the RT-859/APX-72 and associated external equip ment and figure 2-8 is a detailed block diagram of the RT-859A/APX-72 and associated external equipment. The block diagram consists of the ten basic functional blocks; receiver-transmitter, processor (A1), delay line (DL1), decoder (A2), mode 4 (A3), encoder clock (A4), encoder control (A5), M-2 reply code switch, encoder gating (A6), and power supply (PS1); and four external auxiliary blocks; antenna AT-884AIAPX or equivalent, Control Transponder Set C-6280(P)/APX, Computer

KIT-1A/TSEC or equivalent, and Pressure Altitude Digitizer CPU-66/A or equivalent.

a. RF Section. The rf signal from the antenna is fed through a low pass filter (Z3), diplexer (CP1), preselector (Z1), three stage TRF amplifier (AR1), and detector and video amplifier (AR3). A sensitivity circuit (A8), controlled by the C-6280 (P)/APX, is applied to the TRF amplifier to control the amplifier gain. An output from the detector and video amplifier is also fed to the sensitivity circuit as an anti-jam signal. Under jamming conditions the anti-jam signal is rectified on the sensitivity circuit board automatically reducing the gain of the TRF amplifier. For RT-859/APX-72, operation of the anti-jam circuitry is inhibited by the blanking pulses developed, when the output of the processor (A1) is applied to the 1.45 us delay line (DL1); from the clock pulse; and from the mode 4 suppression pulse for modes 1, 2, 3\A, C, and test. For RT-859A\APX-72, operation of the anti-jam circuitry is inhibited by the blanking pulses developed when processor (Al) senses wide pulses; from the clock pulse; and from the mode 4 suppression pulse for modes 1, 2, 31A, C, and test. For both, normal inputs to the rf section are pulse pairs (figure 2-4) at 1030 MHz. The pulse pairs pass unattenuated through the low-pass filter and the diplexer to the preelector input. Pulses, at the correct interrogation frequency, pass comparatively unattenuated through the preselector to the TRF amplifier where they are amplified approximately 43 dB. The pulse output of the TRF amplifier is fed to the detector and video amplifier, where it is detected and further amplified in the log arithmetic type video amplifier stage, before being sent to the processor.

NOTE

For RT-859/APX-72, see subparagraph b below, and for RT-859A/APX-72, see subparagraph c below.

b. Processor (A1) (RT-859/APX-72). The log video output from the detector and video amplifier is fed to a times-seven amplifier in the processor. After amplification, the pulse is applied to threshold circuits which determine narrow pulse width for mode 4 operation. The -90- dBV input sensitivity, and anti-jam circuitry for providing 50% replies when jamming occurs. Operating in conjunction with the threshold circuits is a storage capacitor which remembers the input amplitude of the first pulse received for side lobe suppression (SLS). An input pulse of correct width (greater than 0.2 us) and with an amplitude greater than -90 dBV is passed through the threshold circuits to the delay, line driver. The delay line driver provides a video input to the 1.45 us delay line (DL1) and an AJ blanking pulse to detector and video amplifier (AR3). Output of the 1.45 us delay line is fed back to the processor for wide pulse discrimination and pulse position discrimination. Pulses with a width greater than 1.6 us or spaced less than 0.8 us apart will be rejected when fed back to the processor. Pulses with the correct width and spacing greater than 0.8 us between pulses, will be regenerated to normalized video with a width of

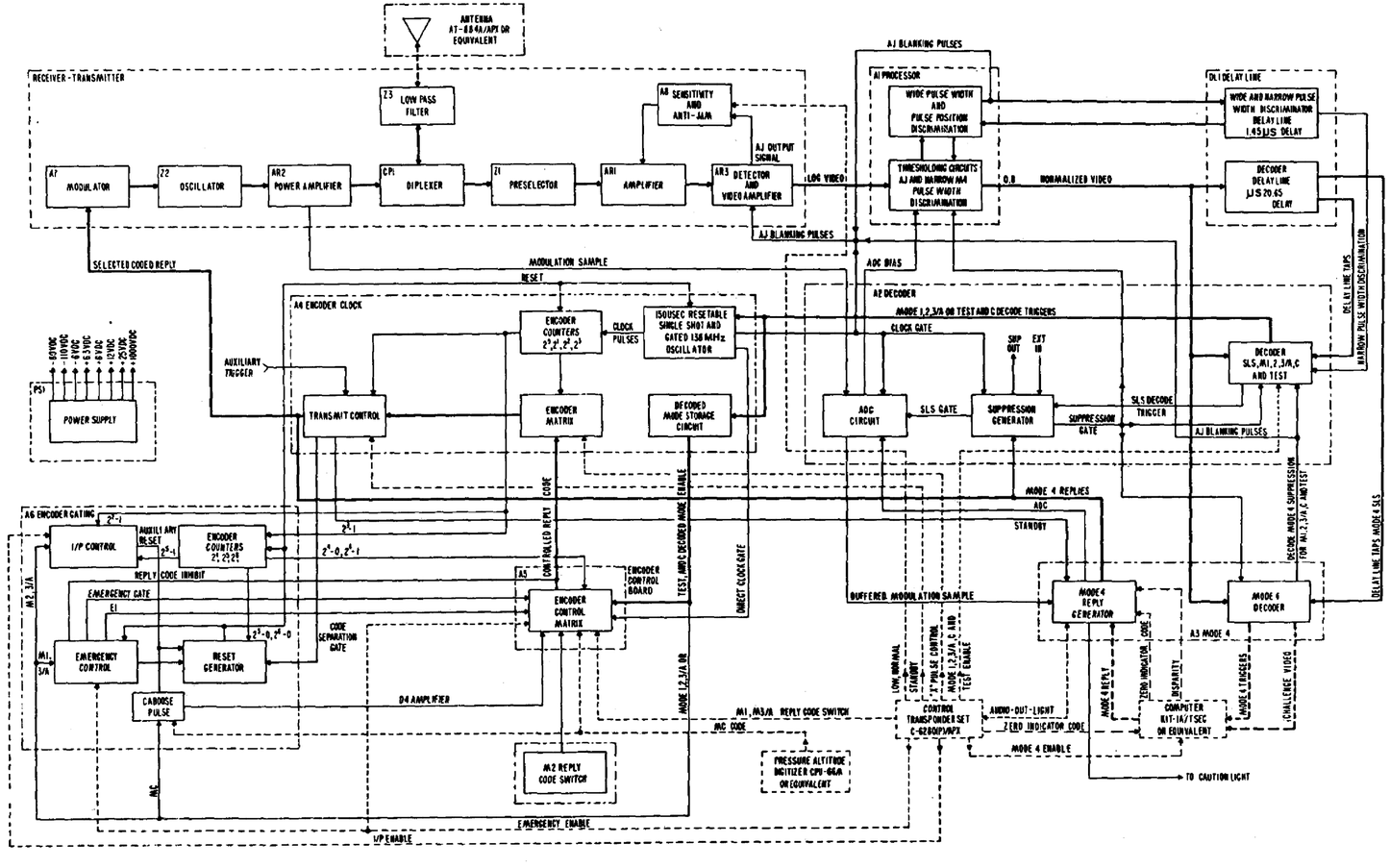


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Figure 2-7. Receiver-Transmitter, Radio RT-859/APX-72, Detailed Block Diagram

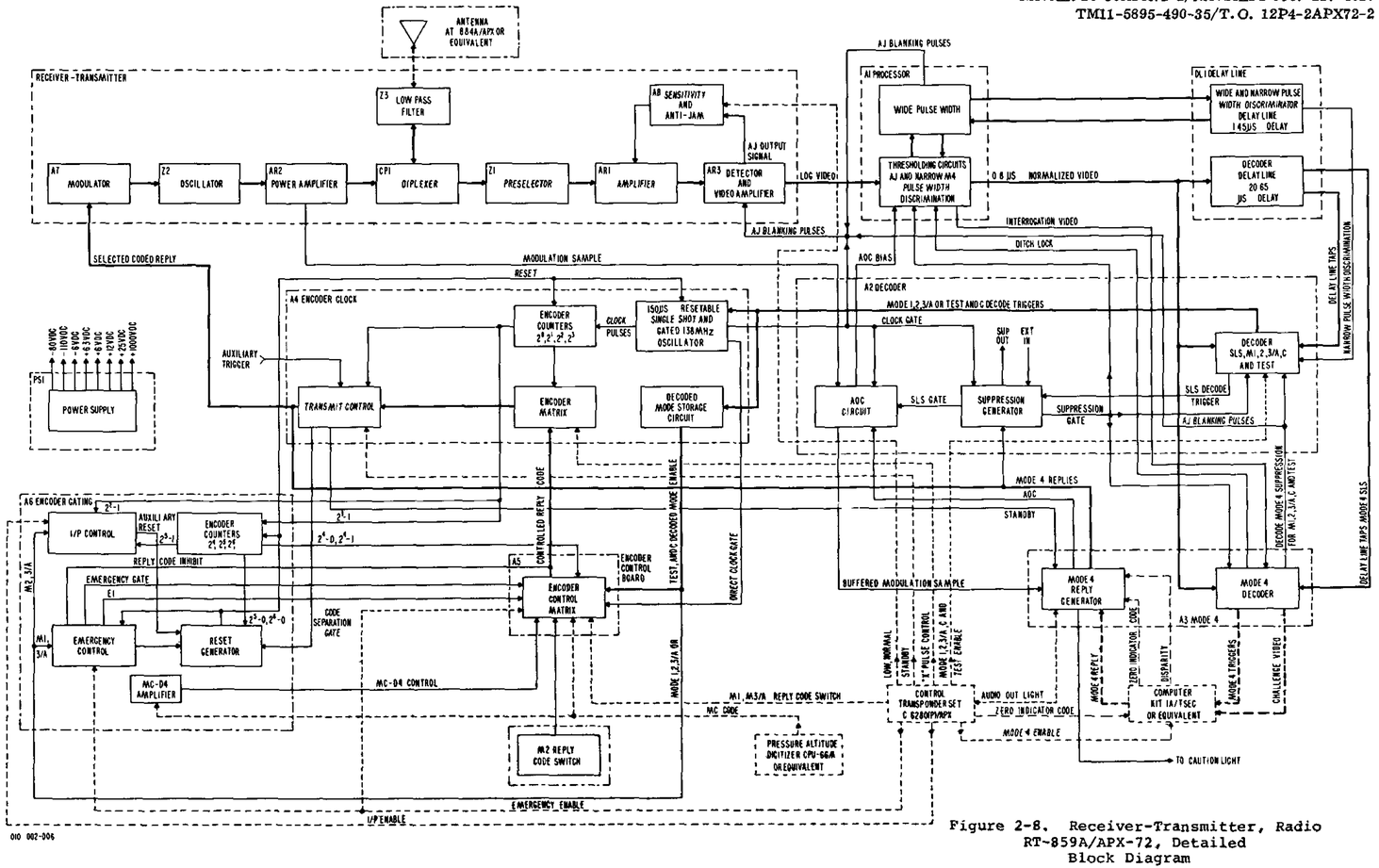


Figure 2-8. Receiver-Transmitter, Radio RT-859A/APX-72, Detailed Block Diagram

0.8 μs and applied to the 20.60 us delay line, decoder, and mode 4 circuits. The automatic overload control (AOC) bias input will reduce the sensitivity, and the suppression gate input to the processor will inhibit the normalized video output.

Processor (A1) (RT-859A/APX-72). The log video output from the detector and video amplifier is fed to an amplifier on the processor with an overall gain of eight. After amplification and buffering, the pulse is applied to various processing circuits which determine minimum allowable pulse widths and amplitudes, and compensate for pulse distortion in the presence of jamming. An analog memory, operating simultaneously with the amplitude thresholding circuits, preserves the amplitude of earlier pulses so that side lobe decisions may be rendered. An input pulse of correct width and sufficient amplitude is digitized and passed through the thresholding circuits to the first delay line driver, which provides a video input to the 1.45 us delay line. The output of this delay line is fed back to the processor, where wide pulse discrimination is performed. Pulses greater than 1.5 us wide will be prevented from entering the transponder decoding circuitry. Simultaneously, a blanking pulse will be developed, which will inhibit the anti-jam integrator located in the video amplifier assembly of the rf section. Pulses with correct width are regenerated as normalized video and given a pulse width of 0.8 us. Normalized video is applied to the 20.6-us decoding delay line, the decoder board, and mode 4 board. When enabled, the automatic overload control (AOC) input will reduce the sensitivity of the processor in a manner proportional to the analog input voltage. Both the internal suppression signal and the mode 4 ditch lock prevent normalized video from being sent to the decoding delay line. Neither these nor the wide pulse detection circuitry will disable the interrogation video drive circuit which provides the mode 4 board with processed video.

d. Delay Line (DL1). The delay line consists of the 1.45-us delay and the 20.60-us delay. For RT-859/APX-72, the 1.45-ps delay receives the output of the first delay line driver from the processor (A1) and provides delayed outputs, as a feedback to the processor, which determines wide pulse and pulse position discrimination, and a narrow pulse discrimination output to the decoder for modes 1, 2, 3/A, test, and C. For RT-859A/APX-72, the 1.45-us delay receives the output of the first delay line driver from the processor (A1) and provides delayed outputs to the processor and a narrow pulse discrimination output to the decoder for modes 1, 2, 3/A, test and C. For both, feedback pulses to the processor, having correct width and spacing, are processed through the second delay line driver and applied to the 20.60-us delay as normalized video. These inputs are applied through delay taps, spaced to coincide with the characteristic spacing of desired interrogation codes, to the decoder and mode 4 circuits as a first step in the mode decoding process.

e. Decoder (A2). The decoder provides three main functions: decoding, internal suppression, and automatic overload control.

NOTE

For RT-859/APX-72 see paragraphs 1, 3, and 4 below, and for RT-859A/APX-72 see paragraphs 2, 3, and 4 below.

1. For RT-859/APX-72, the inputs to the decoder stage are the normalized video from the processor, the 20.60-us delay outputs for decoding modes 1, 2, 3/A, test, C, and side lobe, the 1.45-us delay output for narrow width pulse discrimination, the C-6280(P)/APX mode 1, 2, 3/A, test, and C enable signals, the mode 4 (A3) and internal suppression signals. The decoding circuitry reacts to a valid interrogation by providing a decode trigger output to the encoder clock (A4) for the mode of interrogation recognized (except for the side lobe suppression decode which is applied to the internal suppression circuit). A valid interrogation occurs when coincident outputs of the 20.60-us delay are spaced according to the characteristic spacing of the interrogation codes (see figure 2-4). Narrow pulse discrimination occurs when the pulse entering the 1.45 us delay is narrower than 0.3 us, resulting in an output not in coincidence with the strobe generator. Enabling signals from the C-6280(P)/APX are required for the decoder to respond to any given mode. The presence of an internal suppression, mode 4 suppression, or SLS gate will inhibit the operation of the decoder for the duration of the suppression gate.

2. For RT-859A/APX-72, the inputs to the decoder stage are the normalized video from the processor (A1) and the mode 4 self-suppression signal. Coincident inputs of normalized video and normalized video delayed by 1.65, 3.65, and 5.65 us will generate enable triggers which are fed to an external computer. Simultaneous with the output of the enable trigger, an SIF suppression pulse is generated which, when applied to the decoder board (A2), prevents the decoding of modes 1, 2, 3/A, test and C interrogations. This signal is also fed to the detector and video amplifier (AR3) as an AJ blanking pulse. Coincident with the decoding of the first three mode 4 interrogation bits is the generation of a ditch lock signal which is sent to the processor (A1). This signal lasts for the duration of the SIF suppression signal, but is reset by disparity inputs. After the generation of the ditch lock signal, interrogation video inputs from the processor are sent to the external computer as challenge video.

3. The inputs to the internal suppression circuitry are the side lobe decode trigger, mode 4 replies, the clock gate, and an external suppression. The presence of any one or more of these inputs at the suppression amplifier input will inhibit the decoding operation for all modes of operation, the normalized video output of the processor, and provide an external suppression for the duration of the suppression gate. The side lobe decode trigger is applied through the side lobe gate generator to the suppression amplifier. The mode 4 suppression gate is at-coupled to the internal suppression circuitry when mode 4 replies are generated. The clock gate input is generated when a decode trigger is received at the encoder clock (A4), and is fed back to the suppression circuitry. When

the receiver-transmitter is so modified, the external suppression signal is applied during the operation of TACAN and other L-band equipment.

4. The inputs to the AOC circuit are the SLS gate, mode 4 AOC, modulation sample, and clock gate pulses. The automatic overload control functions as an amplifier of the processed signals from the SLS rate integrator, duty cycle integrator, and reply integrator and applies a bias to the processor (A1) increasing the -90-dB threshold and causing rejection of signals below that value. The SLS gate is applied to the SLS rate integrator, which will provide an output when the side lobe interrogation rate exceeds 5000 interrogations per second. The modulation sample pulses are processed through the duty cycle integrator which will provide an output when the transmitter exceeds a duty cycle greater than 1 percent. The mode 4 AOC is an output from an integrator on A3 which is present to limit the number of mode 4 replies. The clock gate is applied to the reply rate integrator which will produce an output, when the number of replies in modes 1, 2, 3/A, test, and C exceed a preset limit.

e. Mode 4 (A3). The mode 4 circuit board has two functions, decoding and reply generation. The inputs to the decoder stage are processed to provide enabling triggers and challenge video to a remote computer, and the outputs from the computer are processed by the reply generator for transmission. All other modes of operation are functional without the physical presence of the mode 4 board.

NOTE

For RT-859/APX-72 see paragraphs 1 and 3 below, for RT-859A/APX-72 see paragraphs 2 and 3 below.

1. For RT-859/APX-72, the inputs to the decoder stage are the normalized video, the mode 4 and side lobe suppression outputs of the 20.60-us delay line (DL1), and the suppression gate from the decoder (A2). Coincident inputs of normalized video and mode 4 delays of 1.65, 3.65, and 5.65 us recognized as a valid interrogation, will generate enabling triggers which are fed to an external computer. Simultaneous with the output of the enabling triggers, a suppression pulse is generated and applied to the decoder (A2) to prevent decoding of mode 1, 2, 3/A, test, and C interrogations and to the detector and video amplifier (AR3) as an AJ blanking pulse. After generation of the enabling triggers, additional inputs of normalized video are fed through the decoder stage to the external computer as challenge video.

2. For RT-859A/APX-72, the inputs to the decoder stage are the normalized video from the processor (A1) and the mode 4 self-suppression signal. Coincident inputs of normalized video and normalized video delayed by 1.65, 3.65, and 5.65 µs will generate enable triggers which are fed to an external computer. Simultaneous with the output of the enable trigger, an SIF suppression pulse is generated which, when applied to the decoder board (A2), prevents the decoding of modes 1, 2, 3/A, test and C interrogations. This signal is also fed to the

detector and video amplifier (AR3) as an AJ blanking pulse. Coincident with the decoding of the first three mode 4 interrogation bits is the generation of a ditch lock signal which is sent to the processor (A1). This signal lasts for the duration of the SIF suppression signal, but is reset by disparity inputs. After the generation of the ditch lock signal, interrogation video inputs from the processor are sent to the external computer as challenge video.

3. The inputs to the reply generator stage are the mode 4 replies, disparity signal, and zero indicator code from the external computer, the AUDIO-OUT-LIGHT control signal from the C-6280(P)/APX; the buffered modulation sample from the decoder (A2); and the standby inhibit from the encoder clock (A4). Replies from the external computer are processed through the reply generator, and applied through the transmit control stage of the encoder clock to the transmitter. Modulation samples of the transmitted pulse are fed back through the decoder (A2) to the reply generator stage, where a signal is generated to light the reply lamps on the C-6280(P)/APX when the AUDIO-OUT-LIGHT switch is in the AUDIO or LIGHT position. A disparity input from the computer will inhibit the operation of the reply generator stage. None receipt of replies, or disparity inputs from the computer, after enabling signals have been processed, will provide an output to the IFF CAUTION lamp on the pilot's instrument panel and an audio output if in AUDIO position on C-6280(P)/APX. If the computer fails, a ground is applied through the zero indicator code connection, which will also light the IFF CAUTION lamp. When the number of mode 4 interrogation signals exceed the rate established by the AOC threshold, an output is applied to the AOC circuit on the decoder (A2). When the C-6280(P)\APX MASTER switch is in STBY an inhibit signal is applied to the reply generator stage.

f. Encoder Clock (A4). The encoder clock circuitry consists of five stages: the decoded mode storage; 150-us single shot generator and gated oscillator; 2^0, 2^1, 2^2, and 2^4 encoder counters; encoder matrix; and transmit control.

1. The decoded mode storage stage receives mode 1, 2, 3/A or test, and C decode triggers from the decoder (A2). Receipt of a decoded mode trigger activates the decoded mode storage circuit and provides an enabling output to the encoder control matrix (A5). Replies in the decoded mode are enabled as long as the signal is present.

2. Inputs to the 150-us single-shot generator are the mode 1, 2, 3/A or test, and C decode triggers from decoder (A2) and the clear signals from the reset generator on the encoder gating circuit board (A6). The decoded mode trigger input starts the 150-us single-shot generator which provides the direct clock gate, a further amplified clock gate, and actuates the gated oscillator. The direct clock gate output to the encoder matrix (A5) permits passage of stored replies. The clock gate provides outputs to the AOC and suppression generators on the decoder (A2) and an AJ blanking pulse to the detector and video amplifier (AR3).

(a) For RT-859\APX-72 and early models of RT–859A, the gated oscillator operates at 1.38 MHz and develops clock pulses which feed the encoder counters. The input from the reset generator resets the clock gate and stops the oscillator.

(b) For later models of RT-859A\APX-72, the crystal controlled oscillator operates at 27.586 MHz which is counted down to a 1.379 MHz pulse train which is applied to the encoder counters. The input from the reset generator resets the clock gate and stops the clock.

3. Inputs to the 2°, 2^{1}, 2^{2}, and 2^{3} encoder counters are the clock pulses from the gated l.38–MHz oscillator stage, and the clear signals from the reset generator on the encoder gating circuit board (A6). The gated oscillator input to the 2° counter provides the hi-phase timing fox the entire digital system. The reset generator input clears and returns all counter stages to their original state. When the 21 through 24 counter 1 outputs are positive and the 20 counter O output goes positive, the code separation single shot is triggered.

4. Inputs to the encoder matrix stage are the controlled reply code from the encoder control matrix (A5) and timing pulses from the encoder counter stage. The presence of both these inputs, in proper timing phase, will provide a coded reply output to the transmit control stage. "X" pulse circuitry, which provides an output identifying the carrier as a drone aircraft, is part of the encoder matrix stage. The enabling input for the "X" pulse is obtained by grounding a pin on input connector J1.

5. The transmit control stage receives the controlled reply codes from the encoder matrix stage, an inhibit signal (when the C-6280 (P)/APX is in standby) , and an auxiliary trigger from external equipment. The controlled reply code and mode 4 triggers are applied as outputs to the modulator for transmission. The standby output is fed to the mode 4 circuit board (A3) to inhibit operation. The 2° through 2^{4} encoder counter outputs trigger the code separation single-shot generator providing an output to the reset generator on the encoder gating circuit board (A6) and a feedback to the 150-us single shot generator. Under normal conditions, the input to the reset generator generates a reset pulse which resets the clock gate, stops the gated l. 38-MHz oscillator, and clears all the encoder counters. During emergency and I\P operation the code separation gate feedback inhibits the triggers from the gated 1.38-MHZ oscillator, necessary to form the spacing between pulse groups.

9" Encoder Control (A5). The format of the encoder control is a matrix programmed by inputs from the mode 1 and 3/A code switches on the C-6280 (P)\APX, the mode 2 code switch on the front panel of the receiver-transmitter and the mode C pressure altitude digitizer. The decoded mode enable signal (modes 1, 2, 3\A, test or C) from the decoded mode storage stage and the direct clock gate from the 150-us resettable

single-shot generator, both on the encoder clock (A4), combine in the encoder control to release the programmed controlled reply code to the encoder matrix stage of the encoder clock (A4). Other inputs to the encoder control are: the emergency enable signal from the C-6280(P)/APX which enables the transmission of code 7700 in mode 3/A emergency reply; the emergency gate, E-1, 2^4-0, and 24-1 pulses from the encoder gating (A6) which eliminate the coded signals from the last three frames of the modes 1 and 2 emergency replies, and inhibit the normal coded reply of the mode 3/A emergency reply (first frame only); and the reply code inhibit pulse, which prevents the normal coded signal from being transmitted in the last three frames of the mode 1, 2, and 3/A test emergency replies.

h. M2 Reply Code Switch. The M2 reply code switch on the front panel supplies the mode 2 coded inputs for programming the encoder control matrix (A5).

NOTE

In paragraph i, below, reference to the mode C SPI pulse or caboose pulse circuit apply for RT-859/APX-72 only.

i. Encoder Gating (A6). The encoder gating circuitry consists of five stages: I/P control, emergency control, 2^4, 2^5, and 2^6 encoder counters, reset generator, and caboose pulse circuit.

1. Inputs to the I/P control stage are: the I/P enable signal from the C-6280(P)/APX, the mode 2 and 3/A decoded mode storage signals from the encoder clock (A4), and the 22-1 and 25-1 triggers from the encoder counters. The I/P enable signal activates the I/P circuitry for a period of 15 to 30 seconds in modes 1, 2, and 3/A only. The mode 2 or 3/A decoded mode enable input, in conjunction with the I/P enable and 2^2-1, and 25-1 inputs, provide an auxiliary reset pulse to the reset generator which activates the circuitry for generating the special indicator pulse (SPI), and eliminating the normal reply after the first reply has been transmitted in modes 2 and 3/A.

2. Inputs to the emergency control stage are: the emergency enable signal from the C-6280(P)/APX, the mode 1 and 3/A decoded mode enable pulse, from the encoder clock (A4), and the rest pulse from the reset generator. The emergency enable signal activates the emergency function in modes 1, 2, or 3/A only. The mode 1 decoded mode enable pulse is one of three inputs which activate the emergency gate signal to the encoder control (A5) eliminating the coded pulses from the reply train after the first frame. The mode 31A decoded mode enable pulse permits the code 7700, stored in encoder control (A5), to be transmitted during the first frame. pulses from the 25 counter activate the emergency gate, and provide the E-1 pulse to inhibit the X-pulse and the reply code inhibit pulse which prevents normal reply codes being transmitted in mode 3/A transmissions.

3. Inputs to the 24, 25, and 2^6 counters are the 2^3 triggers from the encoder clock (Ad) and the reset generator. The outputs are the 25-1 I/P inhibit to the I/P control, reset inhibits to the reset generator, and emergency flip-flop triggers.

4. Inputs to the reset generators are: the auxiliary reset trigger from the I/P control, the reset generator inhibits from the caboose pulse, the I/P control, the encoder counters, and the code separation gate from the encoder clock (A4). Except for the code separation gate, the other inputs inhibit the normal reset operation of the reset generator. The code separation gate triggers the reset generator to reset the encoder counters, and the 150-us resettable single-shot generator. It also generates the necessary spacing between framing pulses in emergency and I/P operation.

5. For RT-859/APX-72 only, inputs to the caboose pulse circuit are the mode C D4 pulse from the external pressure altitude digitizer, and the mode C decoded enable pulse from the encoder clock (A4). These inputs combine to provide a D4 pulse to the encoder control (A5), the SPI pulse, and a reset inhibit pulse to the reset generator which delays reset action until after the SPI pulse has been transmitted.

j. Transmitter. The transmitter consists of the modulator, oscillator, and power amplifier. The input to the modulator is the selected coded reply from the transmit control stage of the encoder clock (A4). In the modulator (A7) the coded reply is adjusted for pulse width, amplified, and coupled through a driver stage to the output. This output is applied to the grid of the power oscillator (22) which provides a 1090-MHZ pulsed rf output. In the power amplifier (AR2) the 1090-MHZ pulsed rf is amplified to a minimum power output of 250 Watts. A sample of the pulse is fed back to mode 4 (A3) through the decoder (A2) to operate the reply light when mode 4 signals are being transmitted. The amplified pulsed rf is fed to the tuned diplexer (CP1) which offers a low impedance path through (CP1) to the low-pass filter (23) and then to the antenna. The receiver input of the preselector (21) is tuned to 1030 MHZ, therefore little of the transmitted rf energy is transferred to the receiver. The low-pass filter removes spurious responses from the transmitted rf pulse.

k. Power Supply (PS1). The power supply provides all positive and negative voltages for operation, except for the 28 vdc which is supplied from an external power source. The source of power required for power supply operation in either 28 vdc, or 115 vat, 400 Hz.

1. External Auxiliary Equipment. The antenna, an AT-884A/APX or equivalent, receives the interrogating signal and radiates the coded reply signal. Control, Transponder Set C-6280(P)/APX provides the enabling signals for modes and categories of operation, and selects the mode code settings except for mode 2. Computer KIT-1A/TSEC, or equivalent, processes the mode 4 challenge video and prepares the coded reply for transmission. Pressure Altitude CPU-66/A, or equivalent, prepares the coded reply for mode C operation.

2-12. PRINCIPLES OF OPERATION.

NOTE

Unless specifically noted, all text applies for both the RT-859/APX-72 and RT-859A/APX-72.

2-13. The following paragraphs provide a detailed circuit analysis of the receiver-transmitter and the functional characteristics of operation. Applicable schematic and wiring diagrams referenced are in section VI of this manual. Logic diagrams follow immediately after first reference in text.

2-14. RECEIVER. The input to the receiver (see figure 2-7 for RT-859/APX-72 and figure 2-8 for RT-859A/APX-72) is through low-pass filter Z3 and diplexer CP1 to preselector Z1. Z3 is a coaxial-type filter having a bandpass of 1020-1100 MHZ, VSWR of 1.3 maximum, and insertion loss of 0.3 dB. The purpose of Z3 is to prevent radiation of spurious transmitter responses; CP1 enables the use of a single antenna for both reception and transmission. Burnout or overloading of the receiver during transmission and loss of receiver sensitivity, because of transmitter loading when receiving, is prevented by offering a high impedance to 1030 MHZ in the direction of the transmitter during reception, and a high impedance to 1090 MHZ in the direction of the receiver during transmission. The impedance of CP1 is determined by angle of phase shift which is directly related to cable length, making cable dimensions critical to diplexer operation. The receiver consists of preselector (21) and amplifier (AR1).

a. Preselector (Z1). Z1 is a tuned cavity preselector containing inductance-capacitance (LC) sections tunable to produce a good receiver bandpass characteristic in the region of 1030 MHz. The output of Z1 is applied to amplifier AR1.

b. Amplifier (AR1). AR1 is a three-stage tuned radio frequency (TRF) amplifier with a minimum bandwidth of 7 MHz at the 6 dB point. AR1 operates at the center frequency of 1030 MHz with a minimum gain of 43 dB. The output of AR1 is fed to the detector and video amplifier AR3.

2-15. DETECTOR AND VIDEO AMPLIFIER (AR3).

NOTE

Three versions of AR3 are covered in the following paragraph. a and b, below, cover AR3 (Part No. 4023409-0501) in RT-859/APX-72 and early models of AR3 (Part No. 4023409-0502) in RT-859A/APX-72. a and c, below, cover late models of AR3 (Part No. 4023409-0503) in RT-859A/APX-72.

The detector converts the rf signal from AR1 to a video pulse, and the video amplifier compresses the dynamic range of the input video to a level compatible with processor (A1) operation. The schematic diagram for the detector and video amplifier is figure 6-1.

a. Detector. The load on AR3 is determined by the detector and its associated cable, which are computed for loading and cable length to provide a VSWR not to exceed 1.45:1. Physically, the detector assembly is mounted on the front of the video amplifier chassis. The rf input from AR1 is applied through connector P9 (see figure 6-1) to loading or shunting resistors R46 and R47 and a hot-carrier diode CR1. Diode CR1 rectifies the rf input

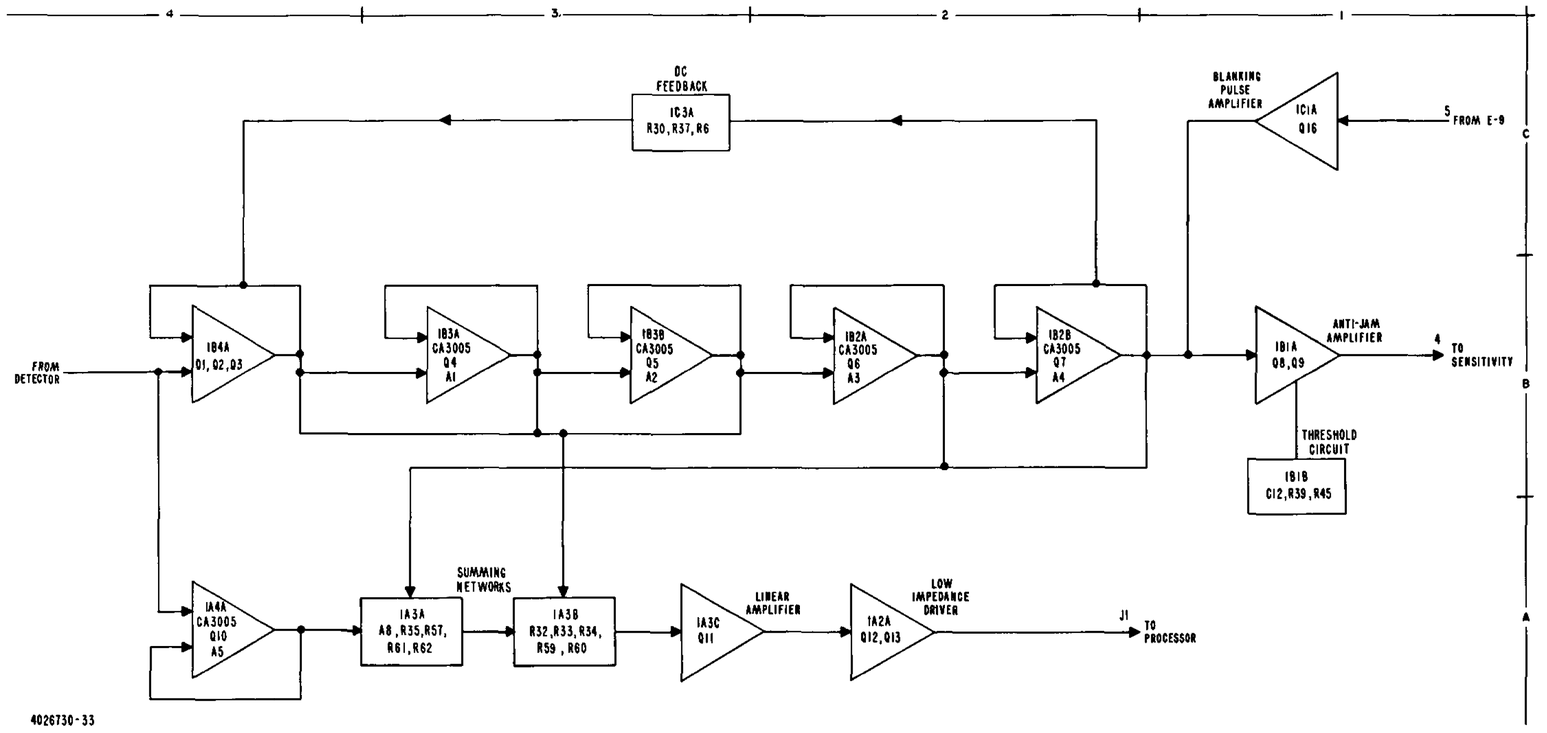


Figure 2-9. Video Amplifier (AR3), Block Diagram

to a video output which is applied to a feed-through capacitor (an integral part of the detector assembly) to eliminate rf currents from the video as it passes to the video amplifier.

b. Video Amplifier. The video amplifier has the twofold function of compressing the dynamic range of the video input to approximately 20 dB while maintaining a constant voltage difference between the side lobe pulse and the first interrogation pulse. An additional function is to generate an anti-jamming output to automatically reduce the gain of the receiver amplifier (AR1).

1. The amplitudes of the input pulses from the detector are compressed logarithmically from a range of approximately 50 dB to 18 dB in a six-stage video amplifier circuit, parallel-summed in two summing networks; amplified by a linear amplifier with a gain of 4.7; and applied through a cascade emitter-follower to the processor (Al). Refer to figure 2-9. The output of the video amplifier yields approximately 140 millivolts for every nine dB change in input signal, as shown in the transfer characteristic curve of figure 2-10. The video output of the detector is fed through resistor R3 to the base of transistor Q1 in the first (1B4A) of six stages of video amplifiers. Transistors Q1 and Q2 form a low noise input differential amplifier; the output of which is applied through emitter follower transistor Q3 to the summing network (1A3B), the input of the next stage (1B3A), and as ac-dc feedback to the source amplifiers. Stages two through six (1B3A, 1B3B, 1B2A, 1F32B, 1A4A) of the video amplifier consist of linear integrated circuits (Al through A5 in figure 6-1) RCA type CA3005 and emitter-follower transistors QA, Q5, Q6, QT, and Q10. Stages one through five are series-connected and have a dc feedback from emitter of transistor Q7 through resistors R30, R37, and R6 (1C3A) to the base of transistor Q2 (1B41A). Capacitor C10 filters the ac component of the feedback to ground. Stage six (1A4A) is parallel fed from the emitter of transistor Q1 through capacitor C15 and resistor R51. Resistors R5, R16, R21, R26, R31, and R53 are load resistors; R7, R13, R18, R23, R28, R5A, R8, R15, R20, R25, R30, and R56 provide individual stage ac-dc feedback; and R14, R19, R24, R29, R38, and R55 form individual stage biasing networks. Capacitors C5, C6, and C7 provide bandwidth limiting to their applicable stages. Resistors R32, R33, R34, R35, R57, R59, R60, R61, R62, and module A8 form the summation network (1A3A, 1A3B) for the video amplifier. (In RT-859A/APX-72, module A8 is replaced with resistor R100.) Module A8 or resistor R100 is inserted in the summing network to compensate for system temperature drift. As the input signal from the detector increases, the signal at the output of (1B2B) rises linearly until limiting occurs. This limited output is coupled through the summing network (module A8 or resistor R100) to the sum point (junction of resistors R57, R58, R61, and R62) and produces the first element of the composite log output. As the detector input signal continues to increase, stage limiting will occur in succession from stage four (1B2A) back to stage one (1B4A). When stages one (1B4A) through five (lB2B) are saturated, parallel-connected stage six (1A4A) will then operate to provide the

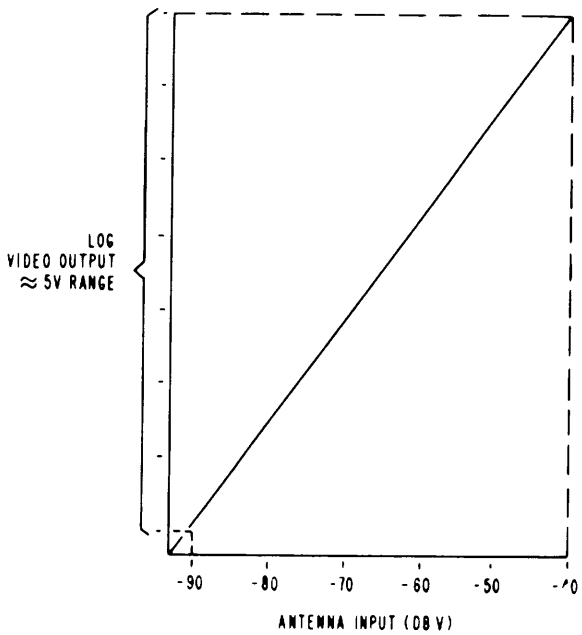


Figure 2-10. Video Amplifier Log Gain Characteristics

high level element to the composite log output. The summed voltages are added at two separate summing points (1A3A, 1A3B) to prevent oscillation, and applied through capacitor C17 to the emitter of linear amplifier (1A3C). A low-impedance driver (1A2A) applies the composite log output to the processor.

2. A shunt-voltage regulator (figure 6-1) for +4.5 and -4.5 vdc is included in the video amplifier circuitry to provide voltage stability, and filter the voltage applied from the power supply (Psi). One input voltage for the regulator is the +12 vdc applied at terminal 1 from filter FL6. The +12 vdc is applied to a voltage divider consisting of resistor R79 and Zener diode VR2, from which +8.4 vdc is applied as inputs to both the +4.5-and -4.5-vdc regulators. The (8.4-vdc input to the +4.5-vdc regulator is divided down across a voltage divider consisting of resistors R72, R73, and R74. Resistor R73 is variable and is adjusted to obtain a +4.5-vdc output at test point TP2. A6, a PA710 micrologic circuit, is a differential voltage comparator which compares the threshold voltage established at pin 3 by resistor R73, and the feedback voltage at pin 2 from the collector output of NPN transistor Q14. The output of A6 is applied through resistor R67 to the base of shunt regulator transistor Q14. An input to transistor Q14, of approximately +0.6 volt, is required to provide the +4.S vdc output at the collector. The output of the +4.5 vdc regulator is applied to the video amplifier stages. The +8.4 vdc input to the -4.5 vdc regulator is dropped to +3.9 vdc at pin 2 of PA710 micrologic unit A7 through a voltage divider consisting of resistor R70 and Zener diode VR1, and to +3.9 vdc at pin 3 of A7 by a voltage divider consisting of resistors R75, R76, and R77. Resistor R76 is variable and is adjusted to obtain a -4.5-vdc output at test point TP3. The output of A7 is applied through the negative bias network of resistors R68, R69, and capacitor C21 resulting in an input of approximately -0,6 volt, to the base of PNP transistor Q15. The -4.5-vdc output at the collector of transistor Q15 provides the basis for the video amplifier. Capacitors C22 and C23 in the regulator circuits prevent A6 and A7 from oscillating. Capacitors Cl, C2, C8, C9, C18, and C19 filter ac component of bias network to ground.

3. The anti-jamming circuit consists of amplifier (1B1A), threshold circuit (1B1B), and blanking pulse circuit (1CIA), diode CR2, and resistors R80 and R81. When jamming occurs, the base line noise on the video pulse will rise as a result of square law detector action. The threshold voltage is set so that the normal noise presently fed through capacitor C11 and resistor R40 to the base of transistor Q8, will not trigger (1B1A). When (1B1A) is triggered, the noise signal is am lified and the output of the collector of Q9 is applied through pin 4 to the sensitivity circuit (A8). Diode CR3 provides protection for the anti-jam amplifier against feedback voltages caused by failure of the sensitivity circuit. For RT-859/APX-72 the blanking pulse amplifier (1C1A) biases the anti-jam amplifier (1B1A) off for each output of the 1.45 us delay line driver of the processor (Al); for each mode 4 supression pulse for modes 1, 2, 3/A, C, and test; and for each clock pulse generated by the encoder clock (A4). For RT-859A/APX-72, the blanking pulse amplifier (1C1A) biases the anti-jam amplifier (1B1A) off for each output of the wide pulse detector of the processor (Al); for each mode 4 suppression pulse for modes 1, 2, 3/A, C, and test; and for each clock pulse generated by the encoder clock (A4) .

c. Video Amplifier. The video amplifier has the twofold function of compressing the dynamic range of the video input to approximately 20 dB while maintaining a constant voltage difference between the side lobe pulse and the first interrogation pulse. an additional function is to generate the anti-jam output to automatically reduce the gain of the receiver amplifier (AR1).

1. The amplitudes of the input pulses from the detector are compressed logarithmically from a range of 50 dB to 18 dB in a linear logarithmic microcircuit amplifier (AR3U1) whose inputs are derived from limiting and differential amplifier circuits. The output of the log amplifier is applied to a low impedance input transistor whose high impedance output is amplified for delivery to the processor (A1). Refer to figure 6-2. The output of the video is approximately 140 millivolts for every 9 dB change in input signal, as shown on the transfer characteristic curve of figure 2-10. The video output of the detector is applied to the base of emitter follower transistors Q1 and Q2 and through limiting resistor R2 to pin 4 of log amplifier U1. The signal at Ul-4, which is determined by resistors R2, R3 and R4, ranges between *zero* and 0.4 volts. From transistor Q1 the signal, which ranges between 0.4 and 1.7 volts, is coupled through capacitor Cl to pin 7 of log amplifier U1. Transistor Q2 and diode CR1 limits the signal to 1 volt at the input to pin 1 of differential amplifi*er* U2. Reference voltage at pin 2 of differential amplifiers U2 and U3 is determined by resistors R11 and R12 and filtered through capacitors C16 and C2. The output signal from amplifier U2, which ranges between 2.9 and 4.5 volts, is applied through resistor R9 and capacitor C3 to pin 9 of log amplifier U1. This same signal is applied through resistor R7 and the one-volt limiting circuit of transistor Q3 and diode CRZ to pin 1 of differential amplifier U3. The signal output of amplifier U3, which ranges between 3 and 4 volts, is applied through resistor R14 and capacitor C4 to pin 12 of log amplifier

U1 and to pin 1 of voltage comparator U4 of the anti-jam circuit. The inputs to log amplifier U1 on pins 4 and 7 are summed together to provide an output at pin 5, and the inputs at pins 9 and 12 are summed together to provide an output at pin 11. The outputs at pins 5 and 11 are summed together through resistors R18 and R19. The resultant output signal is coupled through capacitor C7 to the emitter of transistor U5Q1. Transistor U5Q1 is connected in a common base configuration to provide a low impedance for the log amplifier output signal and a high output impedance for application of the signal to transistor U5Q2. Transistors U5Q2 and U5Q3 are both connected as emitter followers to provide an output signal to connector J1. The output signal at connector J1 ranges between 2.1 and 3 volts and is applied to the processor (A1).

2. Voltages for the video amplifier are +12V, +6V, -6V and -4.4V. The +12V is applied at pin 1 for distribution to the board circuits and through resistor R29 to voltage regulator VR1 where it is Zenered down to +6V. The -6V is applied at pin for distribution to the board circuits and through resistor R28 to voltage regulator VR1 and to the base of current limiting transistor Q4 to provide -4.4V.

3. The anti-jamming circuit consists of voltage comparator U4 and blanking pulse amplifier transistor U5Q4. When jamming occurs in the input signal the base line noise on the video pulse will rise as a result of the pulse limiting action of limiter circuits Q2 and CR1, and Q3 and CR2. The reference or threshold voltage, determined by R16 and R17 at pin 1 of voltage comparator U4 is set so that normal noise will not cause an output at U4-7. When the noise level exceeds the threshold voltage, an output at U4-7 will be applied through pin 4 to the sensitivity circuit (A8). Diode CR3 provides protection for amplifier U4 against feedback voltages caused by failure of the sensitivity circuit. Blanking pulse amplifier U5Q4 applies an inhibit signal to pin 5 of operational amplifier U4 for each output of the wide pulse detector in the processor (A1); for each mode 4 suppression pulse for modes 1, 2, 31A, C and test; and for each clock pulse generated by the encoder clock (A4).

2-16. SENSITIVITY (A8). The sensitivity circuit (see figure 6-3) controls the gain of receiver amplifier (AR1) automatically under jamming conditions, and by operator selection in areas of high signal density. Signal inputs to the sensitivity circuit are from the anti-jamming circuit on the detector and video amplifier (AR3) and the C-6280 (P)/APX. The anti-jamming input signal, consisting of noise spikes from AR3, is applied to a peak-to-peak detector consisting of coupling capacitor C1, resistor R7, and dc reference restorer diode CR1. The restored dc signal is then rectified by diode CR2 and a negative bias voltage developed at the output of the filter circuit consisting of capacitors C2, C3, and resistors R10 and R9. The resultant negative bias is applied through pin 5 to the grids of AR1 reducing the receiver gain. Resistor R24 provides grid current so that there will be no voltage dropped across R10 and R9. Figure 6-3 shows the sensitivity circuit with the

C-6280(P)/APX set in the LOW position. The negative 110-volt input at pin 4 is applied through contacts A2, A3 of relay K1 through adjustable resistor R5, in series with resistors Rl, R2, and R3 to the cathode of AR1. When C-6280(P)/APX is placed in the NORM position, a ground is applied through pin 3 energizing relay K1 and causing contact to break at A3 and make at A1. The new path for the negative 110 vdc is through adjustable resistor R6. Resistor R6 is smaller in value than R5 and will increase the negative voltage to the cathodes of AR1 increasing the receiver gain. Capacitor C4 provides a bypass to ground for ac component of -110 vdc and diode CR3 suppresses induced voltage spikes caused by relay operation.

2-17. PROCESSOR (A1).

NOTE

This paragraph applies for RT-859/APX-72 only. For RT-859A/APX-72, see paragraph 2-18.

The processor (see figure 6-4) converts the log video (analog signals) from the detector and video amplifier (AR3) into digital signals which can interrogate the digital decoder circuitry. The input video signal must be more positive than -90 dB, be of proper width, adhere to minimum spacing between pulses, and have side lobe pulses at least 9 dB below adjacent main pulses in order to transit the processor and provide outputs to the 20.60-us delay line (DL1) and to the detector video amplifier (AR3). See figure 2-11 for the following discussion.

a. Signal Flow. The log video input is applied to a times-seven amplifier (1C5A) the output of which is processed through three separate paths which screen the signal for width, amplitude, jamming, and side lobe rejection. Simultaneous outputs from each of the three paths will result in a signal pulse at the output of logical AND (1B3C) in the absence of suppression or pulse discrimination inputs.

1. Path A for the output of (1C5A) is through the O.28-us delay (1C4B) to differential amplifier (1C4C) and by a parallel path through subtracter (1C5B) and charging and storage circuit (1C4D) to (1C4C). The purpose of delay line (1CQB) is to allow time for (1CQD) to charge and to provide narrow pulse discrimination by delaying the output of (1C4C) to logical AND (1B3C). Subtracter (1C5B) is a constant current sink clamping the input signal level to (1C4C) 3 dB more negative than output of (1C5A). Charging and storage circuit (1CQD) is charged for each input pulse and held charged until discharged through ditch constant current sink (1B4A). The output of (1CQD) is applied as the second input to the delayed -93-dBV threshold circuit, differential amplifier (1C4C). The threshold level for (1C4C) is provided by -93-dBV adjust R22 and amplifier (1B5A). With simultaneous inputs from (1C4D) and (1C4B) the delayed input from (1C4B) being more positive than -93 dBV, (1C4C) is activated providing a 0.28-µs delayed output to logical AND (1B3C). Additionally, (1C4C) provides a feedback through logical OR (1B3B) to ditch disable (1B3A); a feedback through detector (1C3B), differential amplifier (1C3A), and emitter follower (1C4A) to

subtracter (1C5B); and a feedback to subtracter (1A5A).

2. Path B is a parallel output from amplifier (1C5A) through logical OR (1B4B) to -93-dBV differential amplifier (1B4C). The threshold voltage level for (1B4C) is obtained from resistor R22 and amplifier (1B5A). A signal input more positive than -93 dBV activates (1B4C) providing outputs to logical AND circuit (1B3C) and through logical OR (1B3B) to ditch disable (1B3A). A signal input more negative than -93 dBV will fail to activate differential amplifier (1B4C).

3. Path C is from the output of (1C5A) through subtracter (1A5A) and charging' and storage circuit (1A4A) to the -90-dBV threshold differential amplifier (1A4C). The threshold voltage level for (1A4C) is obtained from -90-dBV adjust R25 (1A5B) and the automatic overload bias, developed in the decoder (A2), through logical OR circuit (1A5C). The output of (1A4C) is applied to logical AND (1B3C); to detector suppressor (1C3C); and fed back to its input to hold (1A4C) on for the duration of output pulse. The threshold level of (1A4C) is adjusted for minimum triggering level (MTL) defined as 90-percent replies for a signal level of -90 dBV. An input signal more negative than -90 dBV will fail to energize (1A4C).

4. Logical AND circuit (1B3C) consists of transistors Q15, Q16, and Q17 connected for a common emitter output, and a positive input from pulse position discriminator (1A3A) developed when transistor Q9 is off. The bases of transistors Q15, Q16, and Q17 are connected to (1C4C), (1B4C), and (1A4C), respectively, and all three bases must go positive simultaneously with (1A3A) turned off in order to obtain an output from (1B3C). The output of (1B3C), which is basically determined by the output of (1C4C), is applied to inverter (1B2B) and also fed back through (1B4B) to hold (1B4C) on for the duration of output pulse. The output of (1B2B) is applied to delay line driver (1B2C) and also to logical INHIBIT AND (1A2B). The output of (1B2C) is applied: through terminal 11 to the 1.45 us delay line (DL1); through terminal K as the anti-jam blanking pulse to video amplifier (AR3); to 2 us single-shot (1B2A); to the output of wide pulse discriminator (1BIC); and fed back through (1B4B) to hold 1B4C) on for the duration of the output pulse. The input from the 1.45 us tap on the delay line through terminal B is applied through the wide pulse discriminator (1B2C) to the 0.8-us pulse generator (1B1A). The generator (1B1A) regenerates the input pulse to a width of 0.8 us and applies this pulse through delay line driver (1B1B) and terminal 5 to the 20.60 us delay line (DL1).

b. Anti-Jam Control. The anti-jam control circuitry consists of detector suppressor (1C3C), detector (1C3B), differential amplifier (1C3A), and emitter follower (1C4A). With a normal input, no -jamming, detector suppressor (1C3C) receives simultaneous inputs at the base and collector of transistor Q28 from (1A4C) and (1C4C), respectively. When the signal on the collector is present concurrently with the signal on the base, there is no output. When jamming is present in the input signal such that the noise level exceeds the threshold level of

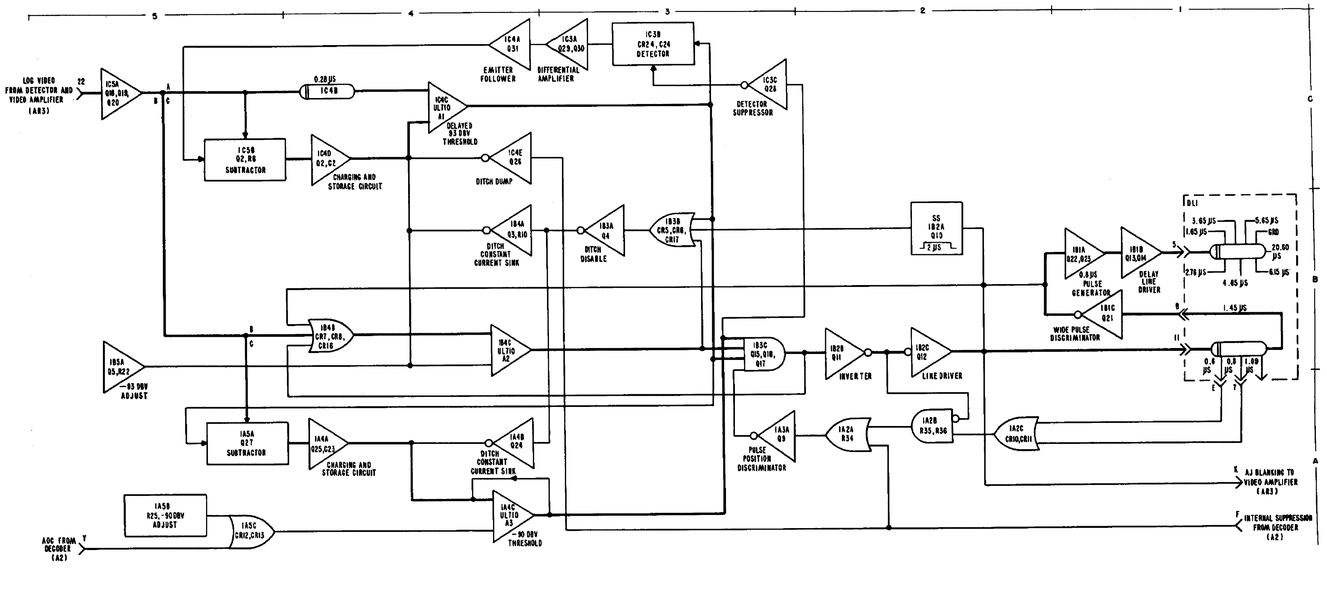


Figure 2-11. Processor (A1) Used with RT-859/APX-72, Logic Diagram

1C4C), the positive output of (1C4C) extending beyond cut-off of (1A4C) until cut-off of (1C4C) will provide a positive input through detector (1C3B) to differential amplifier (1C3A). A positive voltage developed in (1C3A) is applied through emitter follower (1C4A) causing subtracter (1C5B) to conduct harder and clamp the input signal level to (1C4D) 6 to 9 dBV down, effectively eliminating the jamming or noise from the input pulse.

c. Discrimination Circuits. The processor contains circuits for rejecting video input pulses which are less than 0.2 µs wide (narrow pulse), wider than 1.60 µs (wide pulse), and succeeding pulses spaced less than pulse width plus 0.8 µs apart (pulse position).

1. Narrow pulse discrimination is primarily the function of differential amplifiers (1C4C) and (1B4C). The delayed pulse, which energizes (1C4C), arrives 0.28 µs after the direct pulse has energized (1B4C). A pulse, less than 0.2 µs wide, will cause (1C4C) to provide an output after the direct pulse at (1B4C) has passed, and there will be no coincidence of outputs needed to operate logical AND circuit (1B3C). A pulse of 0.28 µs or wider will provide an overlap of outputs from (1C4C) and (1B4C) since (1B4C) will be operating when (1C4C) is energized. These coincident outputs, coupled with the output of differential amplifier (1A4C) and the quiescent state of pulse position discriminator (1A3A), will cause logical AND (1B3C) to operate. The width of the pulse at the output of (1B3C) will be determined by the width of the input pulse to (1C4C) since (1B4C) is held on by the feedback action of (1B3C) and delay line driver (1B2C); (1B3C) will operate until the output of (1C4C) drops to zero.

2. Wide pulse discrimination is made by wide pulse discriminator (1B1C) and the pulse rejected, when the input from the 1.45 µs delay line (DL1) and a parallel output from the 1.45 µs delay line driver (1B2C), are simultaneously present at the base and collector, respectively, of transistor Q1 (1B1C). This condition exists for pulses greater in width than 1.45 µs. Pulses 1.45 µs wide or less will appear at input of (1B1C) when (1B2C) is down, and the output will be applied to the 0.8 µs pulse generator (1B1A).

3. The purpose of pulse position discrimination is to prevent succeeding pulses, closer than the pulse width plus 0.8 µs, from being recognized as a single wide pulse and thus being rejected in the wide pulse discrimination circuit (1B1C). Pulse position discrimination is a function of the output of the 0.6 and 0.8 µs taps of the 1.45 µs delay line (DL1) and the low output of inverter (1B2B). Pulses are applied to logical OR circuit (1A2C) through terminals E and 7 when the 0.6 and 0.8 µs delay line taps are covered. The output of (1A2C) is applied to logical INHIBIT AND (1A2B) which is enabled only when the input from (1B2B) is low indicating the continued presence of the pulse at that point. When activated, (1A2B) provides an output through logical OR (1A2A) causing (1A3A) to turn on and provide a low input to (1B3C) inhibiting the processing of additional pulses while (1A3A) is on. When the pulse in the delay line (DL1)

has passed, the 0.8 µs tap (1A3A) will turn off and normal signal processing will be resumed.

d. Ditch Circuits. Ditch constant current sinks (1B4A) and (1A4B) regulate the discharge rate of charging and storage circuits (1C4C) and (1A4A), respectively. Adjustable resistor R10, connected to base of Q3 (1B4A), varies the linear discharge rate Of (1B4A). Ditch disable (1B3A), when activated, holds (1B4A) and (1A4B) off allowing (1C4D) and (1A4A) to remain charged. Feedbacks from outputs of (1C4C), (1B4C), and from (1B2C) through 2 µs single shot (1B2A) are applied through logical OR (1B3B) to activate (1B3A). These feedbacks combine to hold (1B3A) on and (1B4A) and (1A4B) off for width of pulse plus 2 µs. Ditch dump circuit (1C4E) is activated by the internal suppression input from the decoder (A2) through terminal F. When activated, (1C4E) causes (1C4D) to discharge nonlinearly, reducing discharge time from 13.5 µs to 3 µs.

e. Suppression Circuits. The processor functions to reject second pulses occurring 2 µs after the first pulse and 9 dB or more below (side lobe rejection), to gradually reduce the minimum triggering level (MTL). upon receipt of an automatic overload control (AOC) signal, and to inhibit processing upon receipt of an internal suppression signal.

1. Pulses occurring 2 µs after a first pulse and 9 dB or more below the level of the first pulse, are rejected in the combined circuitry of delayed differential amplifier (1C4C) and charging circuit (1C4D). Capacitor C2 (1C4D) retains the peak voltage of the first pulse less 3 dB. A second pulse of 9 dB or more below will remain below the threshold established on (1C4D) and will be rejected. A second pulse equal to or greater, will penetrate the threshold of (1C4D) causing (1C4C) to operate and be processed as a separate pulse, later identified as the side lobe pulse.

2. The automatic overload control (AOC) signal from decoder (A2) is applied through terminal Y to logical OR circuit (1A5C) to the -90 dBV threshold differential amplifier (1A4C). This positive AOC input will gradually increase the MTL threshold in a positive direction, and thereby reduce the number of pulses processed by the processor.

3. The internal suppression signal from decoder (A2) is applied through terminal F in parallel paths to logical OR circuit (1A2A) and ditch dump circuit (1C4E). The path through (1A2A) energizes (1A3A) which inhibits (1B3C) and prevents processing of input pulses for the duration of the internal suppression signal. The input to ditch dump circuit (1C4E) is explained in paragraph 2-17, d.

2-18. PROCESSOR (A1).

NOTE

The following paragraph applies for RT-859A/APX-72 only. For RT-859/APX-72, see paragraph 2-17.

The processor (see figure 6-5) converts the log video (analog signals) from the detector and video amplifier (AR3) into digital signals which can activate the digital decoder circuitry. The input video signal must

exceed an amplitude threshold, have the proper width, and contain a side lobe pulse (P2) whose amplitude is greater than 9 dB below the amplitude of the first interrogation pulse (Pi) in order to transit the processor and provide outputs to the 20.60-µs delay line (DL1). See figure 2-12 for the following discussion.

a. Signal Flow. The log video input is applied to an amplifier-buffer (1E8A and 1E7A) with an overall gain of eight, the output of which is processed through three separate paths which screen the signal for width, amplitude and presence of jamming noise. In addition, echo rejection and side lobe rejection is effected in these paths. Simultaneous outputs from each of the three paths will result in a signal pulse at the output of logical AND (1C4B).

1. Path A for the output of (1E7A) is through the 0.28-µs delay (1E6B) to differential amplifier (1E6C) and, by a parallel path, to the other input of amplifier (1E6C) through the subtracter (1D7A), charging and storage circuit (1D6A), and buffer (1D6B). The purpose of delay line (1E6B) is to provide the time necessary for the storage circuit to charge properly, and to delay the input from the differential amplifier (1E6C) to logical NAND (1C4B). The length of this delay determines narrow pulse rejection, as the delayed signal is AND'ed with the undelayed signal from path B in logical NAND (1C4B). Subtracter (1D7A) is a constant current sink which pulls a steady current through a fixed resistor. When the input video is applied to this fixed resistor, the subtracter output voltage is less than the input voltage by an amount equal to the product of the constant current and fixed resistance. This product is adjusted by potentiometer R6 so that the output voltage of the subtracter (1D7A) is 3 dB below the level of the input, and this level is used to determine the level to which the output of the charging and storage circuit (1D6A) is raised. This memory is charged for each input pulse and held constant until discharged through the ditch constant current sink (1D6E). The output of (1D6A) is buffered by (1D6B) and applied as the second input to the delayed -93-dBV threshold circuit, differential amplifier (1E6C). The quiescent threshold level for (1E6C) is provided by -93-dBV threshold adjust R22 and amplifier Q13 (1C6A). With simultaneous inputs from (1E6B) and (1D6B), the differential amplifier (1E6C) uses the buffered output of the charging and storage circuit (1D6B) as a threshold for the delayed input video. The stored level is 3 dB below the peak level of the video input, thus the output of (1E6C) represents the width of the unlogged rf signal at the 50–percent point delayed in time by 280 ns. This output is also fed to logical NAND (1C4B); provides an enable to logical NAND (1D4B), which is used in mode 4 operation; enables charge inhibit circuit (1A6A); and serves as an input to detector-integrator (1E5A), which is activated in the presence of jamming.

2. Path B is from amplifier (1E7A) through differential amplifier (1C6A), inverter (1C5A), and logical NOR (1C5B) to logical NAND circuits (1C4B) and (1D4B). The inverting input of

amplifier (1C6A) is connected directly to the threshold circuits of amplifier (1E6C). Signals of greater amplitude than the level set by adjustment of R22 provide outputs which are inverted by (1C5A), and fed to logical NOR (1C5B). The output of (1C5B) is fed directly to logical NAND circuits (1C4B) and (1D4B). If all inputs to (1C4B) are satisfied, its output is fed back to the remaining input of logical NOR (1C5B), whose output remains enabled for as long as (1C4B) has an active output. The output of (1C5B) is also inverted by (1D4A), and fed to logical NOR (1D5B). Inverted by (1D5C), the resulting output inhibits the constant current sinks (1D6E) and (1B5A) which normally act to lower the thresholds of storage circuits (1D6A) and (1A6A) linearly until they reach predetermined minimums.

3. Path C is from the output of (1E7A) through attenuator (1A7A) and charging and storage circuit (1A6A) to differential amplifier (1A6B), the -90-dBV threshold circuit which determines minimum triggering level (MTL). The threshold voltage level for (1A6B) is obtained through adjustment of R25, the -90-dBV adjustment, or through the automatic overload control (AOC) bias developed on the decoder board when the transponder is exposed to overly demanding environments. These two thresholds are OR'd in analog OR circuit (1A7B), and the higher level determines the threshold for (1A6B). When the threshold is exceeded, an enable is supplied to logical NAND (1C4B), detector suppressor (1D5A) is activated, and the amplifier output is fed back to its input so that the enable to (1C4B) is solid at low signal levels. Quiescently, the threshold level for (1A6B) is adjusted so that an rf interrogation to the transponder with an amplitude of -90 dBV will evoke 90-percent replies.

4. In the presence of simultaneous enables from differential amplifiers (1E6C), (1C6A), and (1A6B), logical NAND (1C4B) will be energized. The output duration is determined only by the width of the input from differential amplifier (1E6C), which is equal to the 50-percent pulse width of the rf signal input. The output from amplifier (1C6A) maintains the enable from (1A6B) through (1C5B), (1D4A), (1D5B), (1D5C), and (1B5A), while direct feedback from (1C4B) keeps amplifier (1C6A) enabled for the duration of the output from logical NAND (1C4B). This output is also channeled to the wide pulse integrator (1B3A), and through logical NOR (1C4A) and inverter (1C3A) to the 1.45-μs delay line driver (1C3B). Single shot (1D3B) is activated by the trailing edge of the pulse input to the 1.45-μs delay line. Its purpose is to maintain the memory of the input pulse amplitudes in the charging and storage circuits (1D6A) and (1A6A) for two μs following the trailing edge of an rf input. The output of line driver (1C3B) is delayed by 1.45 μs, and applied to inverter (1A3B), which enables delay line driver (1A3A) and single shot (1B3C). The delay line driver (1A3A) provides true width interrogation video to the mode 4 (A3) board. If the wide pulse threshold has not been exceeded, (1B3C) generates a 0.8-μs pulse, and, through inverter (1B3D) and delay line driver (1B2D), applies this pulse to the 20.60-μs decoding delay line (DL1).

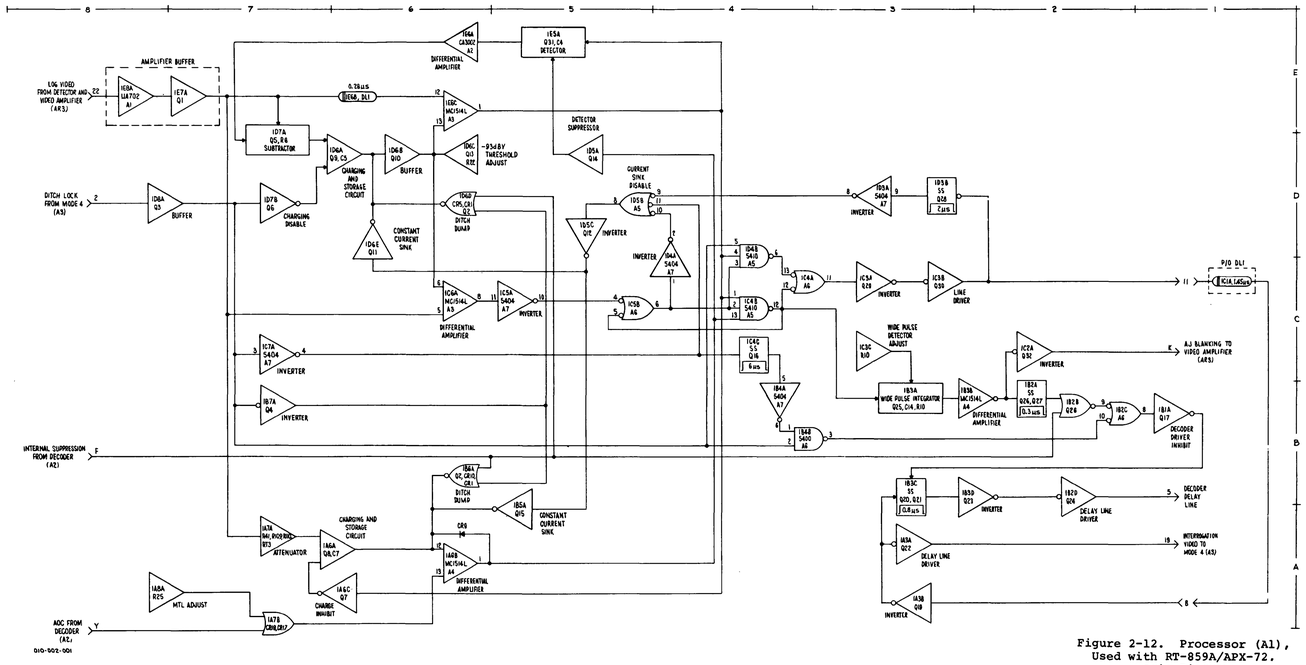


Figure 2-12. Processor (A1), Used with RT-859A/APX-72. Logic Diagram

b. Anti-Jam Control. The anti-jam control circuitry consists of detector suppressor (1D5A), detector (1E5A), and differential amplifier (1E6A). In normal environments, during the absence of jamming signals, the detector (1E5A) receives simultaneous inputs from differential amplifier (1E6C) and differential amplifier (1A6B) through detector suppressor (1D5A). The suppressor prevents the detector from charging to a level which would exceed the threshold level of differential amplifier (1E6A). When jamming interference is present in the input signal, the quiescent noise level at the output of amplifier (1E7A) may be sufficient to exceed the minimum threshold of differential amplifier (1E6C) which is set by -93-dBV threshold adjustment R22. In this case, amplifiers (1E6C) and (1C6A) will pass the noise signal, but the -90-dBV threshold of differential amplifier (1A6B) will not be exceeded. Only two inputs to logical NAND (1C4B) are present, so no pulse will be processed at this time. As (1A6B) provides no output, the detector suppressor (1D5A) is disabled, and the noise from (1E6C) is detected and integrated in detector (1E5A). If this noise is of sufficient density, the threshold of differential amplifier (1E6A) will be exceeded, the output goes positive, and causes the subtracter (1D7A) to set a threshold lower than it would under zero interference conditions. The lowering of the threshold to differential amplifier (1E6C) causes the amplifier to threshold at a lower amplitude on an input pulse, eliminating breakup of the amplifier's output due to hetrodyning of the jamming signal with the rf pulse input. In other words, the sum and difference effect caused by the jamming signal is circumvented by lowering the threshold level of the differential amplifier (1E6C) to a level which is below the minimum of distortion caused by interference.

c. Discrimination Circuits. The processor contains circuits for rejecting video input pulses which are less than 0.2 µs wide (narrow pulse rejection), greater than 1.50 µs wide (wide pulse rejection), and pulses which are lower in amplitude than preceding pulses (echo rejection and side lobe rejection).

1. Narrow pulse discrimination is primarily the function of differential amplifiers (1E6C) and (1C6A) and the 0.28 µs delay line (1E6B). The delayed pulse which energizes amplifier (1E6C) arrives 0.28 µs after the input to amplifier (1C6A) has been enabled. A pulse of sufficient amplitude and with a duration less than 200 ns will thus enable one input to logical NAND (1C4B), and enable the other input 280 ns later. As the pulse itself is narrower than 200 ns, these enables are not present simultaneously, and logical NAND (1C4B) is never satisfied. If the input pulse is 0.28 µs or wider, however, all inputs to the NAND (1C4B) gate are momentarily enabled, and an output is generated and fed back to logical NOR (1C.5B). This feedback maintains enables to (1C4B) from both path B and path C, and the output width is determined by path A.

2. Wide pulse discrimination is accomplished in the wide pulse integrator (1B3A) and differential amplifier (1B3B). The pulse present at the output of logical NAND (1C4B) has been shown to be equal in duration to an rf input

pulse, and is used to enable a ramp generator-integrator (1B3A). Whenever the pulse exceeds a width of 1.50 µs, the integrator voltage will exceed the threshold of differential amplifier (1B3B) and an output will be produced. As a result of this action, inverter (1C2A) produces an anti-jamming blanking pulse which is directed to the video amplifier (AR3). As a second response, single shot (1B2A) is triggered, and regenerates the trigger as a 0.8 µs pulse. This pulse is fed through logical NOR circuits (1B2B) and (1B2C) to the decoder driver inhibit circuit (1B1A), which prevents single shot (1B3C) from being activated. In this manner, pulses judged wider than 1.50 µs are inhibited from the decoding circuits. The precise width at which differential amplifier (1B3B) triggers is determined by R10, the wide pulse integrator adjustment. Adjusting this control changes the slope of the integration ramp, and thus the time at which the threshold of (1B3B) is exceeded.

3. Echo rejection and side lobe rejection are the functions of subtracter (1D7A), charge and storage circuit (1D6A), buffer (1D6B), differential amplifier (1E6C), and constant current sink (1D6E). As described in subparagraph a.1., above, an input signal is reduced in amplitude by 3 dB, stored, buffered, and applied as a reference level to amplifier (1E6C). Constant current sink (1D6E) has previously been disabled by the output of amplifier (1C6A) through (1C5A), (1C5B), (1D4A), (1D5B), and (1D5C), and the level stored in (1D6A) is maintained for the duration of the input pulse. At the trailing edge of the input pulse, the output of the 1.45 µs delay line driver returns to a low state, and this transition enables 3 µs single shot (1D3B). The gate produced provides another enable to logical NOR (1D5B) through inverter (1D3A). This path provides an additional three µs during which the constant current sink is held inoperative. In this period, if a second pulse appears at the input to the processor, it will be rejected by differential amplifier (1E6C) if its amplitude does not exceed the level of first pulse, less 3 dB. This is the process by which side lobe rejection operates. If an ISLS pulse is present in an SIF interrogation, and is equal in amplitude to the interrogation level, it will be passed by amplifier (1E6C); however, if it is nine or more dB below the interrogation, it will not exceed the -3 dB standard and consequently will not be processed. When single shot (1D3B) times out, constant current disable (1D5C) will be released via (1D3A) and (1D5B). Current generators (1D6E) and (1B5A) will now drain a constant current from storage circuits (1D6A) and (1A6A), causing the references to amplifiers (1E6C) and (1C6A) and the input-feedback signal to amplifier (1A6B) to decrease at a linear rate of approximately 4.5 dB per µs. Any echoes originating from valid interrogations will be rejected in the same manner as a side lobe pulse. Sensitivity is thus returned to the transponder at a linear rate of 4.5 dB per µs.

d. Suppression Circuits. The processor functions to gradually reduce the minimum triggering level (MTL) upon receipt of an automatic overload control (AOC) signal, to inhibit processing upon receipt of an internal suppression signal, and to alter

processing upon receipt of a mode 4 ditch lock signal.

1. The automatic overload control (AOC) signal from decoder (A2) is applied through terminal Y to logical OR circuit (1A7B) to the -90 dBV threshold differential amplifier (1A6B). This positive AOC input will gradually increase the MTL threshold in a positive direction, and thereby reduce the number of pulses processed by the processor.

2. The internal suppression signal from decoder (A2) is applied through terminal F through parallel paths to logical NOR circuits (1B6A) , (1D6D), and (1B2B). The first two NOR circuits dump the charge stored in the charge and storage circuits (1A6A) and (1D6A) respectively. This action prevents transmitted rf from being detected and reducing MTL for subsequent interrogations. Logical NOR (1B2B) disables the second delay line driver single shot (1B3C) via path (1B2C) and (1B1A). In this manner, extraneous pulses detected during the time of transmission are kept from the transponder decoding circuits.

3. The mode 4 ditch lock serves many functions. Primarily, this circuit prevents the charging and storage circuit (1D6A) from either increasing or decreasing in amplitude after the decoding of the first three pulses of a mode 4 interrogation. After the ditch lock signal is buffered by (1D8A), it enables inhibit circuit (1D7B) which prevents further inputs to (1D6A). Simultaneously, the output of (1D8A) is inverted by (1C7A) and fed to logical NOR (1D5B), where it prevents reduction in ditch amplitude through inverter (1D5C). The positive output of inverter (1C7A) is delayed four µs by single shot (1C4C) whose output, inverted by (1B4A), is fed to logical NAND (1B4B). This delayed enable is NAND'ed with the buffered ditch lock from (1D8A), and the output of (1B4P) prevents any further normalized video from being applied to the decoder delay line (DLI) through (1B2C) and (1B1A). The four-µs delay is present to allow the fourth mode 4 sync pulse to be sent to the mode 4 decode circuitry. The undelayed output of buffer (1D8A) also enables logical NAND (1D4B) which allows further interrogation pulses to be processed without exceeding the minimum amplitude set by inputs to differential amplifier (1A6B). Thus , a rising AOC level will not interfere with the reception of a mode 4 word once the initial sync pattern has been decoded. On the trailing edge of the ditch lock signal, inverter (1B7A) enables ditch dump circuits (1B6A) and (1D6D) to assure recovery of the processing circuits to within 3 dB of MTL.

2-19. DELAY LINE (DL1). The delay line is divided into two sections connected to a common ground. One section is designated the 1.45-µs delay line and the other the 20.60-µs delay line . All pulses entering the delay line are delayed by the amount of time designated at each tap.

NOTE

Two 1.45-µs delay lines are discussed in this paragraph. For RT-859/APX-72, see a and c below. For RT-859A/APX-72, see b and c below.

a. For RT-859/APX-72, the 1.45-

µs delay line (figure 6-6) has five active terminals: input, 0.6, 0.8, 1.09, and 1.45-µs delays. The input pulse is the 0.2-µs narrow width discriminated pulse from the 1.45-µs delay line driver in the processor (A1). Delayed outputs: the 0.6 and 0.8-µs taps are fed back to the processor for pulse position discrimination, the 1.09–µs tap is fed to the decoder (A2) for narrow pulse discrimination, and the 1.45 µs tap is fed to the processor for wide pulse discrimination.

b. For RT-859A/APX-72, the 1.45 µs delay line (figure 6-7) has three active terminals: input, 1.09, and 1.45-µs delays. The input pulse is the 0.2-µs narrow width discriminated pulse from the l.45-µs delay line driver in the processor (Al). Delayed outputs: the 1.09-µs tap is fed to the decoder (A2) for narrow pulse discrimination, and the 1.45-µs output is fed to the processor for wide pulse discrimination.

c. The 20.60–µs delay line has nine terminals: input and 1.65, 2.76, 3.65, 4.65, 5.65, 6.15, 7.65, and 20.60-µs delays. The input pulse is the regenerated 0.8-µs pulse from the 20.60-µs delay line driver in the processor. The delay line taps are spaced to provide outputs identifying the characteristic spacing of the interrogation codes for decoding purposes. outputs are the zero delayed input to the decoder and mode 4 (A3); the 1.65 µs delay side lobe decode to the decoder and the mode 4; the 2.76-µs delay identifying mode 1, the 4.65-µs delay identifying mode 2, the 6.15-µs delay identifying the test mode, the 7.65-µs delay identifying mode 3/A, and the 20.60-µs delay identifying mode C are applied to the decoder; and the 3.65 and 5.65-µs delays are applied to mode 4.

2-20. DECODER (A2). The decoder circuitry (see figure 6-8 (RT-859/APX-72) or figure 6-9 (RT-859A/APX-72)) provides three general functions: decoding, suppression, and automatic overload control (AOC) bias development. Decoding consists of identifying and processing interrogation codes in modes 1, 2, 3/A, test, and C (mode 4 interrogations are decoded on mode 4 circuit board (A3)). Suppression outputs are generated when: width of interrogation pulse is less than 0.3 µs, a side lobe pulse is decoded, mode 1, 2, 3/A, test, or C have been decoded and replies generated; and when external L band equipment is operating. An AOC bias is generated whenever the rate of interrogation exceeds the internally adjusted limits. Refer to figure 2-13 (RT-859/APX-72) or to figure 2-14 (RT-859A/APX-72) for the following discussion.

a. Decoding Circuits. The decoder input stage consists of seven separate circuits; one each for modes 1, 2, 3/A, test, and C, a side lobe decode, and a strobe generator. The output circuitry consists of four logical AND circuits which apply mode decode triggers to the mode storage circuit on the encoder clock circuit board (A4).

1. The five logical AND circuits , representing the five interrogation modes, operate in the same manner. They are (1B4A), (1B4C), (1B4E), (1B4G), and (1A4A). These logical AND circuits provide a low output when simultaneous inputs,

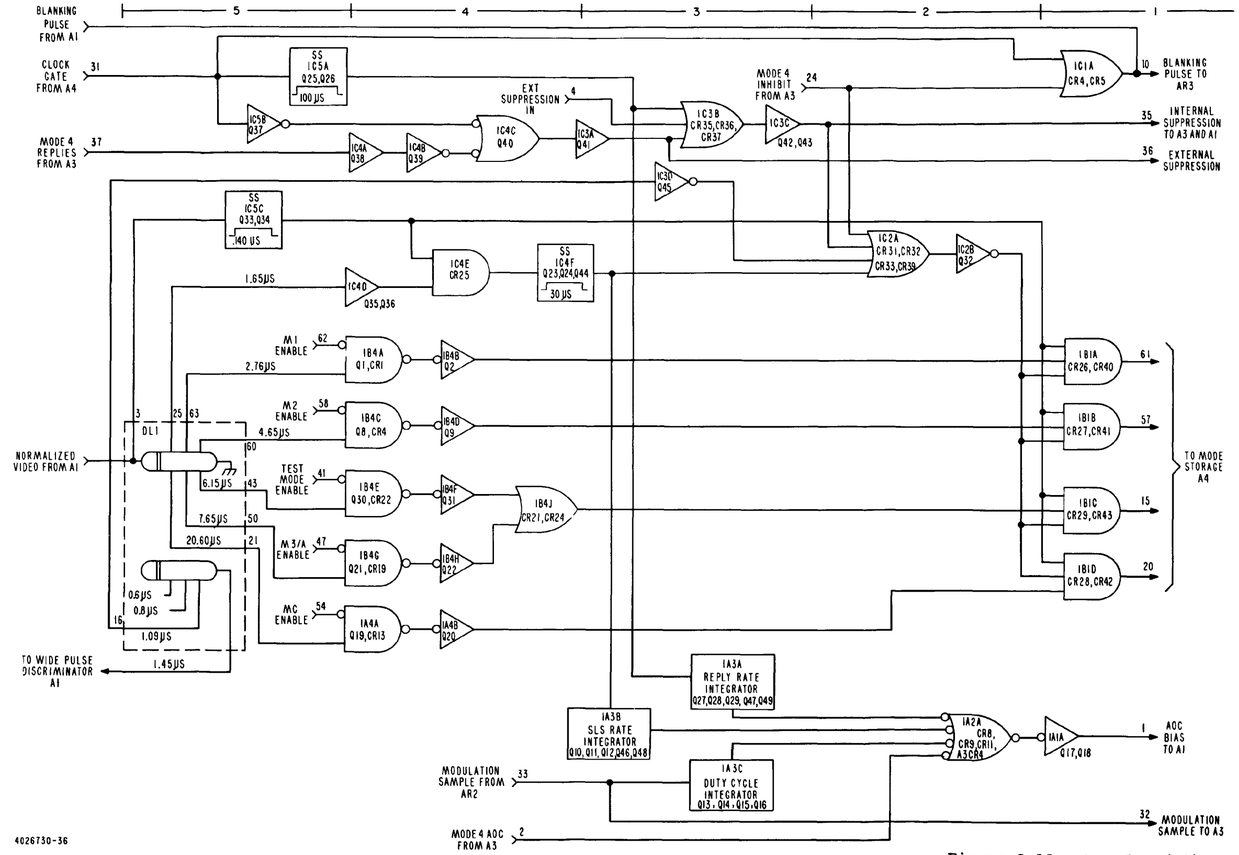


Figure 2-13. Decoder (A2), Used with RT-859/APX-72 Logic Diagram

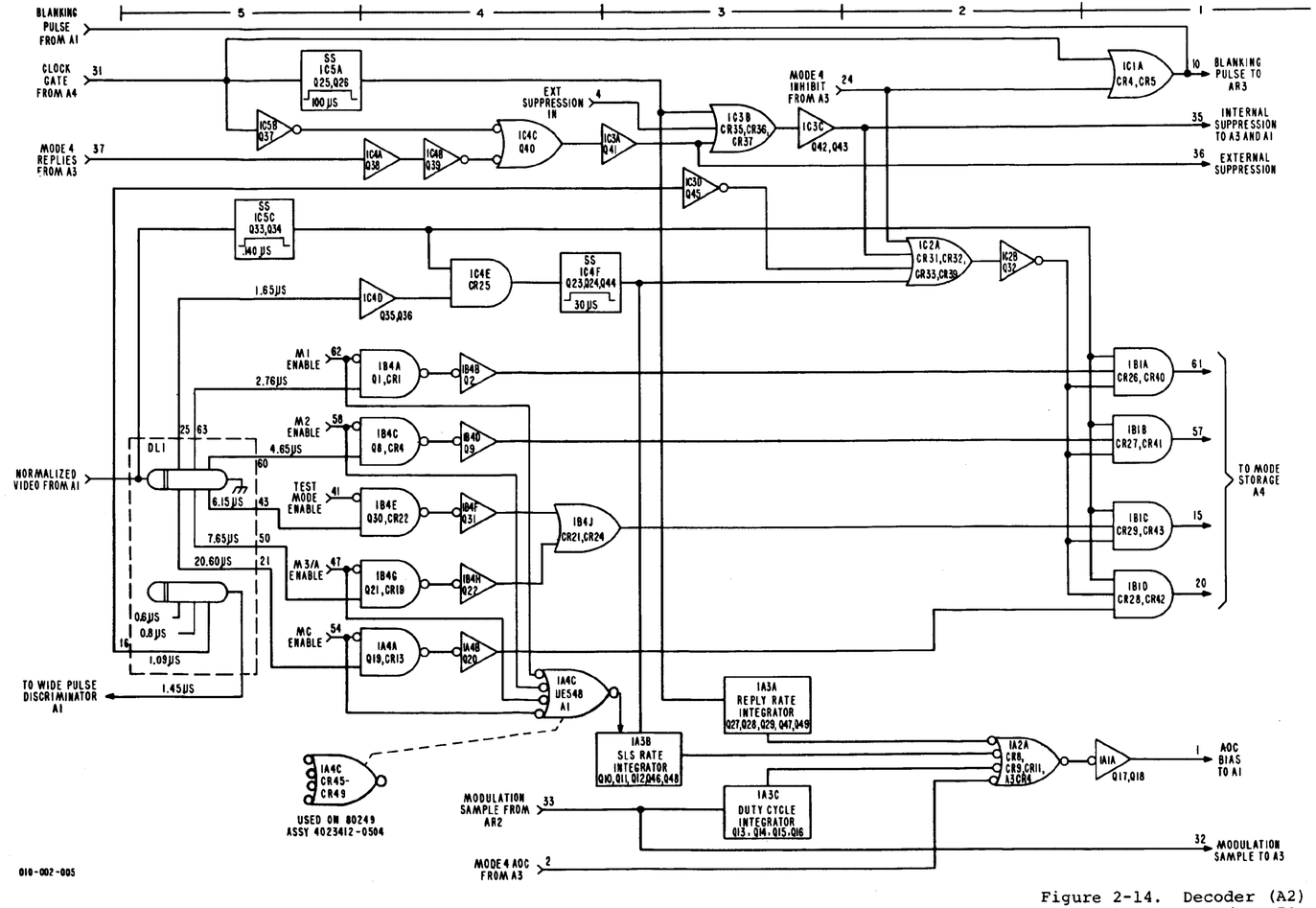


Figure 2-14. Decoder (A2) Used with RT-859A/APX-72 Logic Diagram

consisting of a low or ground input and a high or positive input, are received. The low input is obtained when the applicable MODE IN-OUT switches on the C-6280(P)/APX are in the IN position, and the high input is obtained when the corresponding delay line tap on (DL1) is covered. The low outputs of logical AND circuits are inverted in their associated five inverter amplifiers (1B4B), (1B4D), (1B4F), (1B4H), and (1A4B). The high outputs of (1B4F) test mode and (1B4H) mode 3/A are applied to logical OR circuit (1B4J) which provides a high output whenever activated by either mode. The outputs of the three remaining inverter amplifiers and (1B4J) are applied to logical AND circuits (1B1A) through (1B1D) , respectively. Logical AND circuits (1B1A), (1B1B), (1B1C), and (1B1D) require two additional high inputs, appearing coincidently with the first interrogation code pulse, to provide a decoded mode output. one of these inputs is from the strobe generator (1C5C) and the other from the suppression inverter amplifier (1C2B) when it is in the off condition indicating the absence of any suppression inputs. Outputs developed in (1B1A) through (1B1D) are fed to the mode storage circuit on the encoder clock circuit board (A4) as mode decode triggers.

2. Side lobe decoding is a function of the side lobe decoder (1C4D) and logical AND circuit (1C4E). The input to (1C4D) is the l.65-µs tap output from the 20.60-µs delay line (DLI). This input signal causes transistor Q35 (1C4D) to conduct and its collector output to go to ground. When this happens, the base of transistor Q36 (1C4D) is placed at ground potential turning it off for duration of pulse width and applying a positive 6-volt output across diode CR25 (1C4E). If this input coincides with the receipt of a positive input from (1C5C), a side lobe decode is obtained, and the output of (1C4E) is applied to side lobe gate generator (1C4F) and SLS rate integrator (1A3B).

3. Strobe generator (1C5C) is a single-shot, the input to which is the normalized video output of the processor (Al) applied from the input of the 20.60-µs delay (DL1) through terminal 3. This positive input to (1C5C) causes transistor Q34 to conduct and drive transistor Q33 to cutoff, through capacitor C36. Transistor Q33 remains off for the charging time of capacitor C36 and resistor R106, approximately 0.140 µs. With transistor Q33 off, its collector voltage is positive providing a back bias on diodes CR26 through CR29, (1B1A) through (1B1D), enabling development of mode decode triggers for the 0.140-µs width of output pulse.

b. Suppression Circuits. suppression of modes 1, 2, 3/A or test, and C are accomplished by the output of logical OR circuit (1C2A). A positive input from any one of four suppressions sources will produce an output at (1C2A). This output is inverted by inverter amplifier (1C2B) and applied to logical AND circuits (1B1A) through (1B1D) providing a path to ground through diodes CR40 to CR43, and (1C2B) for any other inputs present for the duration of the suppression pulse. The four sources of suppression input to (1C2B) are: narrow pulse width discrimination, side lobe decode, internal suppression, and mode 4 inhibit.

Suppression outputs developed to inhibit circuits and equipment external to the decoder are the blanking pulses, internal suppression, and external suppression.

1. Narrow pulse width discrimination occurs when there is no coincidence, between the output of the 1.09-µs tap of the 1.45 µs delay line (DL1) and the output of strobe generator (1C5C). The 1.09 µs delay input to narrow pulse discriminator (1C3D) causes transistor Q45 to conduct, dropping its collector output to ground. This ground potential reverse biases transistor Q32 (1C2B) through diode CR39 (1C2A) holding it off for the width of the pulses obtained from the 1.09-µs delay tap. For pulse width greater than 0.3 µs (1C5C) will remain positive coincident with (1C2B), and logical AND circuits (1B1A) through (1B1D) will be enabled to provide mode decode triggers. For pulses less than 0.3 µs wide the collector of transistor Q33 (1C5C) will be at ground and inputs to logical AND circuits (1B1A) through (1B1D) will be shorted to ground.

2. When a side lobe pulse is decoded, an output is applied from logical AND (1C4E) to the side lobe gate generator (1C4F). A positive input from (1C4E) causes transistor Q23 to conduct and its collector to go to ground. Transistor Q24 is reverse-biased through capacitor C25, turned off, and remains off through the time constant of capacitor C25 and resistors R68 and R72. The positive output of the collector of transistor Q24 is applied to SLS rate integrator (1A3B) and (1C2A) for 30 µs. The positive output of (1C2A) is inverted by (1C2B) and fed to (1B1A) through (1B1D) suppressing their outputs for 30 µs. Transistor Q44 (1C4F) turns on at the end of 30 µs, and acts as a fast recovery single-shot returning the circuit to its original state within 2 µs.

3. The internal suppression function is concentrated at logical OR circuit (1C3B). A positive input to (1C3E3) from either an external suppression source, the reply gate generator (1C5A), or the external suppression generator (1C4C) through (1C3A), will provide a positive output which is fed to internal suppression generator (1C3C) and then to (1C2A). The positive input to (1C3C) causes transistor Q42 to conduct and its collector voltage to go to ground turning off transistor Q43. The positive collector voltage output of transistor Q43, when it is off, is fed to (1C2A) as the internal suppression input. This positive voltage output is also applied through terminal 35 to suppress operation of the processor (Al) and mode 4 (A3).

(a) The external suppression source applied to (1C3B) is applied from external L band equipment to provide protection for the receiver when the L band equipment is transmitting.

(b) The reply gate generator (1C5A) develops the internal suppression input to (1C3B). When a decoded mode trigger is fed to the mode storage on encoder clock circuit board (A4), a clock gate signal is fed back to terminal 31 of the encoder. This positive clock gate signal applied to single-shot (1C5A) causes transistor Q25 to conduct and its collector voltage to go to ground turning off transistor

Q26. The time constant of capacitor C27 and resistor R80 hold transistor Q26 off the 100 µs during which time the positive output voltage from the collector of transistor Q26 is applied to (1C3B). Diode CR16 compensates for temperature changes.

(c) The external suppression generator input to (1C3B) is developed from the clock gate signal and from the generation of mode 4 replies. The positive clock gate signal is applied through terminal 39 to clock gate inverter amplifier (1C5B), causing transistor Q37 to conduct and its collector voltage output to go to ground. This collector output is applied to logical OR (1C4C). The generated mode 4 replies are ac coupled through terminal 37 to emitter follower (1C4A) causing it to conduct. The positive emitter output of transistor Q38 causes transistor Q39 (1C4B) to conduct and its collector voltage to go to grounds When the low inputs of either (1C5B) or (1C4B) are applied to (1C4C), transistor Q40 will conduct , raising its collector voltage output to +24 volts. The high output of (1C4C) is applied to emitter follower (1C3A) causing it to conduct and provide a positive output at its emitter. This positive output pulse, approximately 23 µs wide, is applied as external suppression to (1C3B) and through terminal 36 to external equipment to protect against jamming by receiver-transmitter transmission of replies.

4. When mode 4 interrogations are decoded a 100-µs suppression signal is developed on mode 4 circuit board (A3) and applied to decoder terminal 24. This input is applied to logical OR (1C2A) and will function to inhibit decode of modes 1, 2, 3/A, test, and C for a period of 100 µs. A parallel path for this inhibit signal is to logical OR (1C1A) consisting of diodes CR4 and CR5 (physically connected to XA2P1 on card cage). This circuit is activated whenever a mode 4 suppression or a clock gate signal is received. The output of (1C1A) is a blanking pulse which is applied through terminal 10 to detector and video amplifier (AR3) to prevent jamming of the receiver by transmitted replies.

Automatic Overload Control (AOC). The AOC functions whenever the interrogation rate is faster than the internally adjusted rate. The AOC circuitry consists of four integrators whose outputs are applied to logical OR (1A2A), which consists of diodes CR4 (on A3) , CR8, CR9, and CR11. The four integrators are the reply rate integrator (1A3A), SLS rate integrator (1A3B), duty cycle integrator (1A3C), and the mode 4 reply rate limiter which is on the mode 4 circuit board (A3). A low input to (1A2A) from either of these integrators provides a low output to amplifier (1A1A). The low input to (1A1A) causes transistor Q17 to conduct and provide a positive output at its collector. This output is applied through terminal 1 to the processor (Al) increasing the MTL threshold in a positive direction and thereby reducing the number of interrogation pulses processed.

1. The input to reply rate integrator (1A3A), is the positive output of reply gate generator (1C5A). This input causes transistor Q47 to conduct, dropping its collector voltage output to

ground, and causing transistor Q27 to conduct charging capacitor C28 through resistor R83 for 100 µs. When the voltage on capacitor C28 exceeds the voltage set by reply rate adjust resistor R89, transistor Q28 conducts and provides low input to (1A2A) generating an AOC bias output for as long as the rate is above the rate set by R89.

2. The input to SLS rate integrator (1A3B) is the 30-µs SLS gate generator (1C4F) pulse developed from the decoded side lobe pulse. This input causes transistor Q46 to conduct, dropping its collector voltage output to ground and causing transistor Q10 to conduct, charging capacitor C15 through resistor R35 for 30 µs. When the voltage on capacitor C15 exceeds the voltage on the base of transistor Q12, transistor Q11 conducts and provides a low input to (1A2A), generating an AOC bias output for as long as the SLS rate is above threshold.

NOTE

In the RT-859A/APX-72 (figure 2-14), logical OR circuit A1 (1A4C) inhibits (1A3B) when all SIF modes (1, 2, 3A, and C) are disabled.

3. The input to duty cycle integrator (1A3C) is sample negative pulses from the transmitter power amplifier (AR2) applied through terminal 33. A buffered sample of these input pulses is fed directly to mode 4 circuit board (A3) through terminal 32. The negative input to (1A3C) is amplified by transistor Q13 which also charges capacitor C18 through resistor R44. When the voltage input to transistor Q14 exceeds the voltage set by duty cycle, adjust resistor R51, transistor Q15 conducts and provides a low input to (1A2A) generating an AOC bias output.

NOTE

The following paragraph applies for RT-859/APX-72, for RT-859A/APX-72, see paragraphs 2-22 and 2-22A.

2-21. MODE 4 (A3). The mode 4 circuit board (see figure 6-10) provides six general functions: decoding, suppression, AOC bias development, processing challenge video, amplification of computer replies, and generation of audio and visual monitors for mode 4 operation. Decoding consists of identifying and processing mode 4 interrogations to provide an enabling trigger output to activate the computer. Suppressions are generated to inhibit decoding in all modes: as a result of decoding mode 4 interrogations; and when an external suppression, generated in decoder (A2), is received. An AOC bias is generated when the rate of interrogation exceeds the limits established in the reply rate integrator. Normalized video is processed and applied to the computer as challenge video. Computer replies are amplified and applied to the modulator through the encoder clock (A4) and power supply (Psi). Visual and audio monitors for mode 4 circuit operations are generated. Micrologic units, used extensively in this circuit, are described on logic drawings by type number. Refer to figure 2-15 for the following discussion.

a. Decoding Circuits. The mode 4 decode inputs consists of the normalized video input to delay line (DL1) and the 1.65-µs, 3.65-µs, and 5.65-µs outputs from the delay line taps. The

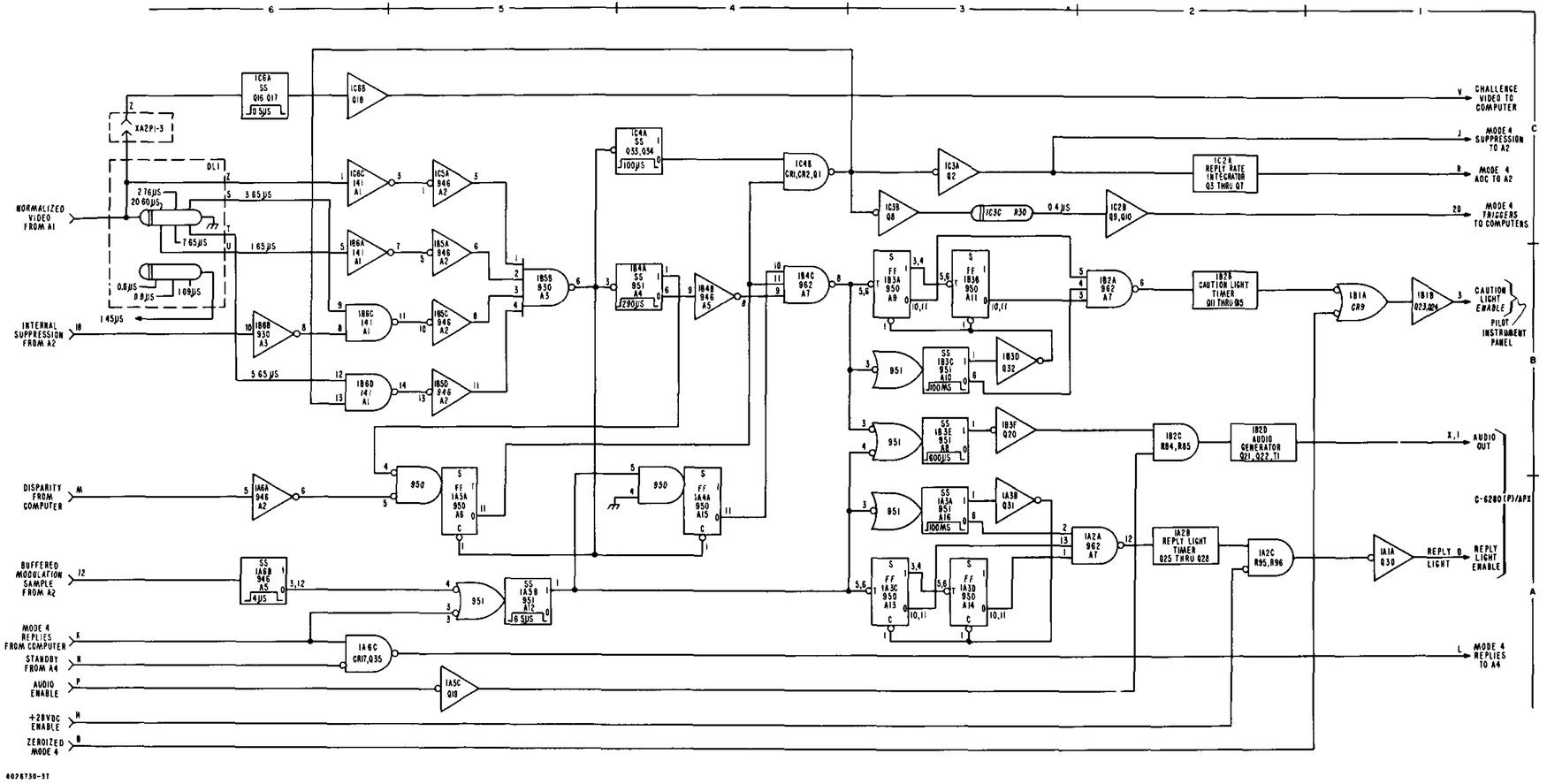


Figure 2-15. Mode 4 (A3), Used with RT-859/APX-72, Logic Diagram

normalized video input is amplified in two inverter stages (1C6C) and (1C6A), the 1.65-µs input in two inverter stages (1B6A) and (1C5A), the 3.65-µs input in logical NAND (1B6C) and inverter (1C5C), and the 5.65-µs input in logical NAND (1B6C) and inverter (1C5D). Logical NAND (1B6C) is also fed by inverter amplifier (1B6B), which is normally off, providing a positive input to (1B6C) except when a suppression signal is received from the decoder (A2). Logical NAND (1B6C) is also fed by logical NAND (1C4B) providing a positive input to (1B6D) until a decode strobe is generated causing transistor Q1 (1C4B) to conduct and disable (1B6D). To obtain a mode 4 decode, all four inputs to logical NAND (1B5B) must appear as positive voltages in coincidence. The low decode output of (1B5B) is applied through four parallel paths to single shots (1C4A) and (1B4A), and flip-flops (1A4A) and (1A5A). The low input to (1C4A) causes transistor Q34 to turn off, driving its collector voltage positive causing transistor Q33 to conduct charging capacitor C6 through resistor R104. After 100 µs, capacitor C6 is charged sufficiently to cause transistor Q34 to again conduct and terminate the output pulse. The positive voltage output of transistor Q34 is applied to logical NAND (1C4B) for 100 µs. The second input to (1C4B) is a positive voltage from the O output of flip-flop (1A5A) reset positive by the parallel decode Output Of (1B5B). The combining of the two positive inputs to (1C4B) causes transistor Q1 to conduct and provide a low voltage on its collector. This low voltage output is applied through parallel paths to inverter amplifiers (1C3A), (1C3B), and logical NAND (1B6D). The input to (1C3B), which is transistor Q8, causes it to turn off and remain off until its base is again driven positive through (1C3C), which requires approximately 0.4 µs. When (1C3B) again conducts, a low input is provided to (1C2B). Transistor Q9 of (1C2B) turns off causing transistor Q10 to conduct and provide a positive output at its emitter. This positive output is applied through terminal 20 to the computer as the mode 4 enable trigger.

b. Suppression Circuits. Internal suppression is generated from the output strobe of logical NAND (1C4B) which feeds an input to (1B6D) suppressing mode 4 decoding for 100 µs. At the same time, a parallel output of (1C4B) is applied to inverter amplifier (1C3A) turning transistor Q2 off. The positive output of (1C3A) is applied to the decoder (A2) to suppress modes 1, 2, 3/A, test, and C for 100 µs. When a disparity signal is returned from the computer, it is applied through inverter amplifier (1A6A) to flip-flop (1A5A). The negative-going input triggers (1A5A) to its set position with ground being supplied at the O output. This ground is applied to (1C4B) and terminates the suppression of decoding.

Automatic Overload Control Bias (AOC). An AOC bias is developed from the mode 4 external suppression output when the rate of interrogation in mode 4 exceeds the limits established in the circuit. The third path for the positive voltage output from the collector of transistor Q2 (1C3A) is applied to reply rate integrator (1C2A), which causes transistor Q3 to conduct, driving its collector voltage to ground

which causes transistor Q4 to turn off and charge capacitor C12 through resistor R22 and diode CR3 for 100 µs. When the voltage on capacitor C12 exceeds the voltage on the anode of CR5 set by the reply rate adjust resistor R29, transistor Q6 conducts and provides a negative output through terminal R to AOC bias circuit on decoder (A2).

d. Challenge Video. Pulses following immediately after a mode 4 interrogation code are designated challenge video and are used to interrogate the computer after it has been enabled by the mode 4 enable trigger. These normalized video pulses are applied through terminal Z to single shot (1C6A). The positive input causes transistor Q16 to conduct, discharging capacitor C23 through resistor R58 for approximately 0.5 µs. Transistor Q17 is biased off for the duration of the charging cycle supplying a positive output from its collector which causes emitter follower (1C6B) to conduct providing 0.5 µs challenge video pulses from the emitter through terminal V to the computer.

e. Mode 4 Replies. Mode 4 replies from the computer are applied through terminal K to logical NAND (1A6C). With the MASTER switch, on the C-6280(P)/APX, in any position but OFF or STBY, the low enabling input to (1A6C) through terminal N is at ground potential. Mode 4 reply inputs to the enabled (1A6C) are amplified by transistor Q35 and applied to modulator (A7) through encoder clock (A4) and power supply (Psi).

f. Visual and Audio Monitors. Three external indications of mode 4 circuit operations are available to the operator, namely a reply light, indicating four or more replies are transmitted within a 0.033-second interval or replies are transmitted at a rate of 50 or more per second for 0.25 seconds; a caution light, indieating grounding of control lead by computer or failure to reply to a valid mode 4 interrogation; and an audio output when enabled, indicating that the reply light or caution light counters are activated.

1. The source for reply light operation is the mode 4 replies and the buffered modulation sample of the transmitted mode 4 replies. Mode 4 replies are applied through terminal K to logical OR (1A5B). The buffered modulation sample applied through terminal 12 to single shot (1A6B), generates a 4-µs positive pulse which is also applied to (1A5B). These inputs, the 4-µs positive pulse and the positive-going mode 4 replies, trigger (1A5B) and provide a negative 6.5-µs output at terminal 1. This output is the counter start pulse which is applied to trigger (1A4A), (1A3A), (1A3C), and (1B3E). When single shot (1A3A) is triggered, a positive 100-µs pulse is applied to enable logical NAND (1A2A). During the 100-µs period that (1A2A) is enabled, additional mode 4 replies trigger (1A3C), and if four or more replies are received within a 0.033-second interval, (1A2A) will be activated and provide a low input to the reply light timer (1A2B). This input turns transistor Q25 off, which causes transistor Q26 to conduct and discharge capacitor C31. As capacitor C31 discharges, the base of transistor Q27 is pulled to ground, turning off transistor Q28. The positive output

from the collector of transistor Q28 causes transistor Q29 to conduct and its collector voltage to go to ground providing an output to logical INHIBIT AND (1A2C). The low input from (1A2B), combined with the positive 28 vdc enable, will provide a low output to inverter amplifier (1A1A) and enable the reply light. When the 100-ms pulse to (1A2A) is removed, (1A2B) operation reverses providing a positive output which disables (1A2C) and the reply light. The reply light is enabled for approximately 3 seconds.

2. The caution light enable is controlled by three inputs to logical NAND (1B4C) and the zeroized mode 4 input from the computer, through terminal B, to logical OR (1B1A). To activate (1B4C) and provide a counter start pulse for the caution light enable, three simultaneous positive inputs are required. These three inputs are developed from the decode strobe, absence of disparity signal, and absence of valid mode 4 replies. When the decode strobe is developed at the output of logical NAND (1B5B), it is also applied to clear or reset flip-flops (1A5A) and (1A4A) and to trigger (1B4A). The positive outputs of (1A5A) and (1A4A) in the reset position are applied to (1B4C) awaiting a third input to activate it. A positive 290-µs pulse developed in (1B4A) is fed through the O output and ac coupled to inverter amplifier (1B4B). The 1 output of (1B4A) is at ground potential and applies an enabling input to (1A5A) which will activate if a disparity pulse is received. The inverted output of (1B4B) is applied as a negative input to (1B4C) disabling it for 290 µs. At the end of 290 µs (1B4A) changes state and the inverted input to (1B4C) becomes positive. Lacking any change of state of (1A5A) and (1A4A), due to the absence of either disparity or valid mode 4 replies, (1B4C) is activated and the output pulse applied to trigger caution light counter (1B3A) and single shot (1B3C). When single shot (1B3C) is triggered, a positive 100-µs pulse is applied to enable logical NAND (1B2A). Flip-flops (1B3A) and (1B3B) provide positive inputs to logical NAND (1B2A) through their O outputs activating (1B2A) and providing a low input to caution light timer (1B2B). This input turns transistor Q11 off which causes transistor Q12 to conduct and discharge capacitor C21. As capacitor C21 discharges, the base of transistor Q13 is pulled to ground, turning off transistor Q14. The positive output from the collector of transistor Q14 causes transistor Q15 to conduct and its collector voltage to go to ground applying a low input to logical OR (1B1A). The second input to (1B1A) is the zeroized mode 4 input from the computer through terminal B. When either of these two inputs appear at (1B1A), a low output is applied to inverter amplifier (1B1B). The base and emitter of Q23 go positive and turn Q24 on. Q24 supplies a caution light enable signal (2 to 5 seconds) through terminal 3. When the 100-µs pulse to (1B2A) is removed, (1B2B) operation reverses providing a positive output, which in the absence of a zeroized mode 4, disables (1B1B) and the caution light. The caution light is enabled for approximately 3 seconds.

3. An audio output, when enabled, is generated to start either a caution light counter

(1B3A) or a reply light counter (1A3C). The outputs of logical NAND (1B4C) which feeds (1B3A) and the output of (1A5B) which feeds (1A3C) are applied to logical OR (1B3E). The presence of a low input from either of the above sources will trigger single shot (1B3E) generating a 600-µs pulse. This pulse is applied in the negative direction through (1B3E) to inverter amplifier (1B3F) turning it off for 600 µs providing a positive output to logical AND (1B2C). The enabling input for (1B2C) is the AUDIO-OUT-LIGHT switch on the C–6280(P)/APX which, when in the AUDIO position, provides a ground to inverter amplifier (1A5C). This input is inverted and applied to (1B2C) activating it when a positive output from (1B3F) is present. The positive output of (1B2C) is applied to audio generator (1B2D) which consists of transistors Q21, Q22, and transformer T1. Transister Q21 and Q22 operate in push–pull, charging and discharging capacitor C32 through transformer T1. The resulting audio signal is applied to control C-6280(P)/APX through terminals X and 1.

NOTE

The following paragraph applies for A3 (Part No. 4028683-0502) in RT-859A/APX-72. For A3 (Part No. 116104-1) in RT-859A/APX-72, refer to paragraph 2-22A. For RT-859/APX-72, refer to paragraph 2-21.

2-22. MODE 4 (A3). The mode 4 circuit board (see figure 6-11) provides six general functions: decoding, suppression, AOC bias development, processing of interrogation video, amplification of computer replies, and generation of audio and visual monitors of mode 4 operation. Decoding consists of identifying and processing mode 4 interrogations to provide enable triggers to activate an external computer, and to provide a ditch lock for the processor board (A1) . Suppressions are generated to inhibit decoding in all modes as a result of recognizing a mode 4 interrogation. An AOC bias is generated when the rate of interrogation exceeds the limit established in the reply rate limiter-integrator. Interrogation video is processed and sent to an external computer as challenge video, while computer replies are amplified and applied to the modulator through the encoder clock board (A4). Visual and audio indicators of mode 4 circuit performance are provided. Refer to figure 2-16 for the following discussion.

a. Decoding Circuits. The mode 4 decode inputs consist of the normalized video input to, and the delayed outputs from the decoder delay line (DL1). The normalized video input is differentiated and reduced in amplitude by input network (1F7B). Inputs from the (DL1) delay taps are buffered and normalized in amplitude by input networks (1E7A), (1E7B), and (1D7A), respectively, which are applied to NAND gates (1F6D) and (1E6A). Whenever simultaneous signals appear at the three inputs to NAND (1F6D), A negative level is produced which triggers single-shot (1F6E). The 5-µs output of this circuit is sent through NOR (1F4C) to the processor board (A1) as the ditch lock. In order to obtain a mode 4 decode, all four inputs to NAND (1E6A) must appear as positive levels coincidently. The decode strobe produced at the output of (1E6A) is applied

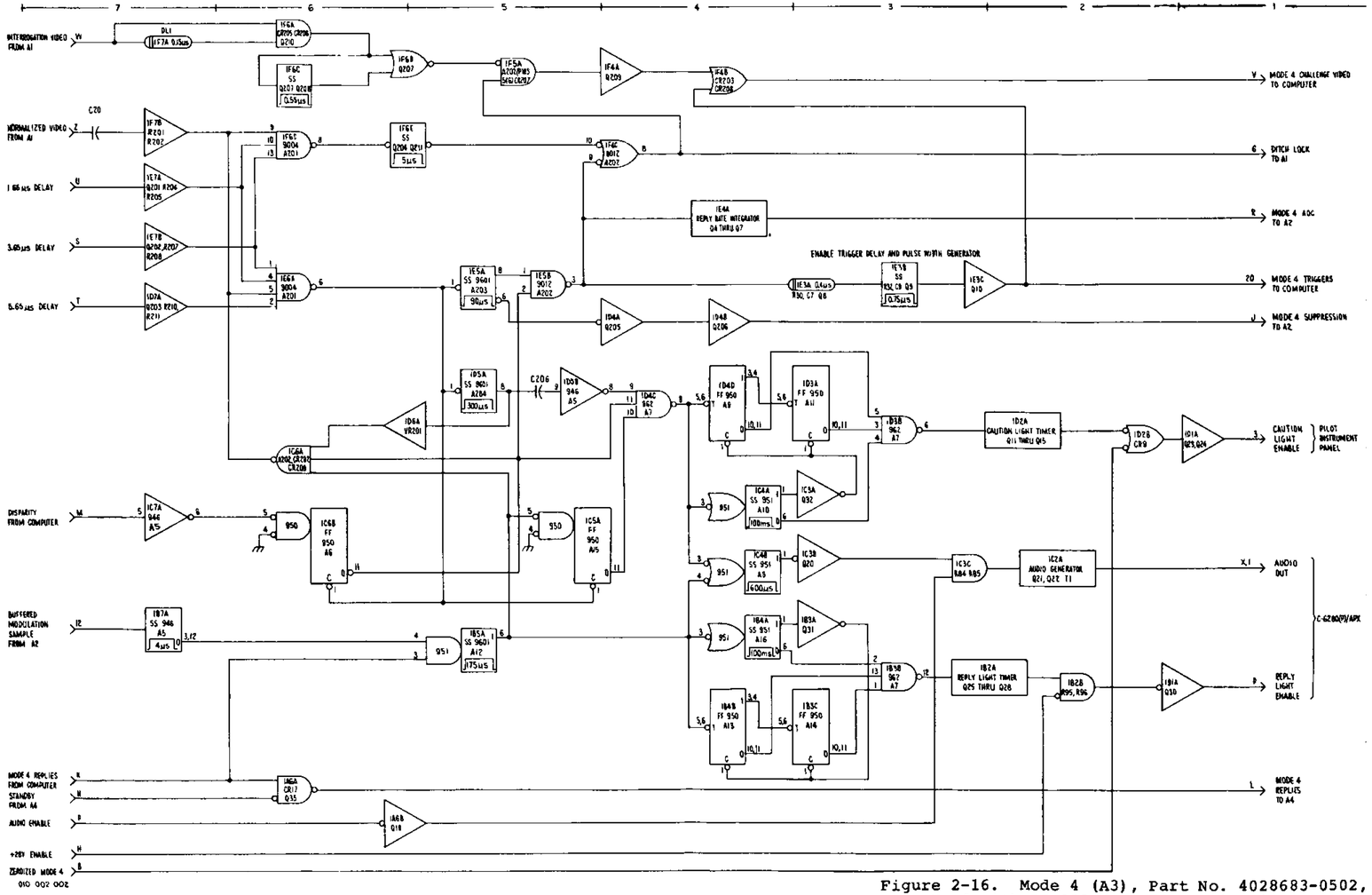


Figure 2-16. Mode 4 (A3), Part No. 4028683-0502, Used with RT-859A/APX-72, Logic Diagram

through four parallel paths to single shots (1E5A) and (1D5A), and flip-flops (1C5A) and (1C6B). This signal resets both flip-flops; that is, causes their zero outputs to assume a high level; and causes both monostables to trigger. The positive-going output of (1E5A) and the just reset positive output of bistable (1C6B) are applied to logical NAND (1E5B), causing its output to switch to a low level. This output is delayed 0.4 µs by half single shot (1E3A), shaped to 0.75-µs duration by half single shot (1E3B), amplified by (1E3C), and sent to an external computer as the mode 4 enable trigger. Additionally, the output of logical NAND (1E5B) enables logical NOR (1F4C) for the duration of the enable from single shot (1E5A). The ditch lock is thus sent to the processor (A1) for approximately 92 µs through the path consisting of (1E6A), (1E5A), (1E5B), and (1F4C). Upon receipt of a disparity signal from the external mode 4 computer, flip-flop (1C6B) toggles due to the amplified disparity pulse from (1C7A), and the second enable to gate (1E5B) is removed. The termination of this enable removes the ditch lock signal from the processor (Al).

b. Suppression Circuits. Mode 4 self-suppression is generated by logical NAND (1C6A). As mentioned previously, a mode 4 decode strobe resets flip-flop (1C6B) and causes single shot (1D5A) to go into the active state. The positive output from flip-flop (1C6B) is fed directly to logical NAND (lC6A), while zener diode (1D6A) reduces the positive output of single shot (1D5A) to the proper level to activate (1C6A). The quiescently high output of single shot (1B5A) is also applied to logical NAND (1C6A). In the presence of all three enables, (1C6A) prevents the strobe inputs to decoding gates (1F6D) and (1E6A) from going positive. No more mode 4 interrogations are recognized until either a disparity or a reply is received from the external mode 4 computer, or until the 300-µs single shot (1D5A) times out. At the time of the mode 4 decode strobe, single shot (1E5A) is also energized. The negative-going output is inverted by (1D4A), buffered by (1D4B), and sent to the decoder board (A2) as an SIF suppression signal. Thus, for 90 µs after the recognition of a mode 4 interrogation, the SIF modes are inhibited from decoding. If a disparity interrupts normal mode 4 operation, the suppression of SIF decoding is not terminated at the time of the disparity.

Automatic Overload Control Bias; (AOC). An AOC bias is developed from the output of logical NAND circuit (1E5B). Each time the output of this gate goes to ground, an integrating capacitor in the reply rate integrator (1E4A) is allowed to charge. As the number of interrogations increases, the charge on the integrator increases until a predetermined threshold is exceeded. At this point an output is produced by (1E4A) which is fed to the decoder board (A2).

d. Challenge Video. Pulses following immediately after a mode 4 interrogation are designated challenge video and are used to interrogate an external computer after it has been enabled by a mode 4 enable trigger. Interrogation video from the processor board (A1) is applied to a 0.15-µs delay line (1F7A) and

simultaneously to logical AND circuit (1F6A). The overall effect of this delay line is to delay the output of AND circuit (1F6A) and to shorten by 150-ns any pulse fed into it. The positive output of (1F6A) enables logical NOR (1F6B) and triggers single shot (1F6C) , whose output is also fed to logical NOR (1F6B). In this manner, the output of (1F6B) is guaranteed to be no narrower than the width of the single shot (1F6C). When the input is very wide, the output will be 150 ns less than the duration of the input. The negative-going output of (1F6B) is AND'ed with the ditch lock signal by (1F5A) and fed to buffer stage (1F4A). This interlocking eliminates challenge video from the computer until the first three pulses of a mode 4 interrogation have been decoded. SIF challenge video is thus kept from the computer. The enable trigger from buffer (1E3C) is also OR'ed with the output of (1F4A) by logical OR (1F4B) to produce challenge video.

e. Mode 4 Replies. Mode 4 replies from the computer are applied through terminal K to logical NAND (1A6A). With the MASTER switch, on the C-6280(P)/APX, in any position but OFF or STBY, the low enabling input to (1A6A) through terminal N is at ground potential. Mode 4 reply inputs to the enabled (1A6A) are amplified by transistor Q35 and applied to modulator (A7) through encoder clock (A4) and power supply (Psi).

f. Visual and Audio Monitors. Three external indications of mode 4 circuit operations are available to the operator, namely: a reply light, indicating four or more replies are transmitted within a 0.033-second interval or replies are transmitted at a rate of 50 or more per second for 0.25 second; a caution light, indicating grounding of control lead by computer or failure to reply to a valid mode 4 interrogation; and an audio output when enabled, indicating that the reply light or caution light counters are activated.

1. The source for reply light operation is the mode 4 replies and the buffered modulation sample of the transmitted mode 4 replies. Mode 4 replies are applied through terminal K to logical OR (1B5A). The buffered modulation sample applied through terminal 12 to single shot (1B7A), generates a 4-µs positive pulse which is also applied to (1B5A). These inputs, the 4-µs positive pulse and the positive-going mode 4 replies, trigger (1B5A) and provide a negative 6.5-µs output. This output is the counter start pulse which is applied to trigger (1C5A), (1B4A), (1B4B), and (1C4B). When single shot (1B4A) is triggered, a positive 100-ms pulse is applied to enable logical NAND (1B3B). During the 100-ms period that (1B3B) is enabled, additional mode 4 replies trigger (1B4B), and if four or more replies are received within a 0.033-second interval, (1B3B) will be activated and provide a low input to the reply light timer (1B2A). This input turns transistor Q25 off, which causes transistor Q26 to conduct and discharge capacitor C31. As capacitor C31 discharges, the base of transistor Q27 is pulled to ground, turning off transistor Q28. The positive output from the collector of transistor Q28 causes transistor Q29 to conduct and its collector voltage to go to ground providing an output to

logical INHIBIT AND (1B2B). The low input from (1B2A), combined with the positive 28-vdc enable, will provide a low output to inverter amplifier (1B1A) and enable the reply light. When the 100-ms pulse to (1B3B) is removed, (1B2A) operation reverses providing a positive output which disables (1B2B) and the reply light. The reply light is enabled for approximately three seconds.

2. The caution light enable is controlled by the three inputs to logical NAND (1D4C) and the zeroized mode 4 input from the computer, through terminal B, to logical OR (1D2B). To activate (1D4C) and provide a counter start pulse for the caution light enable, three simultaneous positive inputs are required. These three inputs are developed from the decode strobe, absence of disparity signal, and absence of valid mode 4 replies. When the decode strobe is deveoped at the output of logical NAND (1E6A), it is also applied to clear or reset flip flops (1C6B) and (1C5A) and to trigger (1D5A). The positive outputs of (1C6B) and (1C5A) in the reset position are applied to (1D4C), which requires still a third input to activate it. The positive 300-µs pulse from (1D5A) is capacitive coupled to inverter (1D5B) and applied as a negative input to (1D4C) to disable (1D4C) for 300 µs. After 300 µs, (1D5A) changes state and the inverted input from (1D5B) to (1D4C) becomes positive. Lacking any change of state of (1C6B) and (1C5A), due to the absence of either disparity or valid mode 4 replies, (1D4C) is activated and the output pulse applied to trigger caution light counter (1D4D) and single shot (1C4A). When single shot (1C4A) is triggered, a positive 100-ms pulse is applied to enable logical NAND (1D3B). Flip-flops (1D4D) and (1D3A) provide positive inputs to logical NAND (1D3B) through their O outputs activating (1D3B) and providing a low input to caution light timer (1D2A). This input turns transistor Q11 off which causes transistor Q12 to conduct and discharge capacitor C21. As capacitor C21 discharges, the base of transistor Q13 is pulled to ground, turning off transistor Q14. The positive output from the collector of transistor Q14 causes transistor Q15 to conduct and its collector voltage to go to ground applying a low input to logical OR (1D2B). The second input to (1D2B) is the zeroized mode 4 input from the computer through terminal B. When either of these two inputs appears at (1D2B), a low output is applied to inverter amplifier (1D1A). Transistor Q23 turns off and, through its emitter, also turns off transistor Q24 supplying a caution light enable pulse through terminal 3. When the 100-ms pulse to (1D3B) is removed, (1D2A) operation reverses providing a positive output, which, in the absence of a zeroized mode 4, disables (1D1A) and the caution light. The caution light is enabled for approximately three seconds.

3. An audio output, when enabled, is generated to start either a caution light counter (1D4D) or a reply light counter (1B4B). The outputs of logical NAND (1D4C) which feeds (1D4D) and the output of (1B5A) which feeds (1B4B) are applied to single-shot (1C4B). The presence of a low input from either of the above sources will trigger single shot (1C4B) generating a 600-µs

pulse. This pulse is applied in the negative direction through (1C4B) to inverter amplifier (1C3B) turning it off for 600 µs providing a positive output to logical AND (1C3C). The enabling input for (1C3C) is the AUDIO-OUT-LIGHT switch on the C-6280 (P)/APX which, when in the AUDIO position, provides a ground to inverter amplifier (1A6B). This input is inverted and applied to (1C3C) activating it when a positive output from (1C3B) is present. The positive output of (1C3C) is applied to audio generator (1C2A) which consists of transistors Q21, Q22, and transformer T1. Transistor Q21 and Q22 operate in push-pull, charging and discharging capacitor C32 through transformer T1. The resulting audio signal is applied to control C-6280(P)/APX through terminals X and 1.

NOTE

The following paragraph applies for A3 (Part No. 116104-1) in RT-859A/APX-72 . For A3 (Part No. 4028683-0502) in RT-859A/APX-72 refer to paragraph 2-22. For RT-859/APX-72 refer to paragraph 2-21.

2-22A. MODE 4 (A3). The mode 4 board (figure 6-11A) provides six general functions: decoding, suppression, processing of interrogation video, amplification of computer replies, AOC bias development, and generation of audio and visual monitors of mode 4 operation. Decoding consists of identifying mode 4 sync patterns. As a result of decoding a mode 4 sync pattern, internal and external suppression signals are generated, the mode 4 computer is triggered, and processor (A1) is provided with a ditch lock signal. Interrogation video is processed and routed to the mode 4 computer as challenge video. The replies of the computer are amplified and routed to modulator (A7) through encoder clock (A4). An AOC bias is generated when the rate of interrogation causes the reply rate integrator to exceed an established limit. The mode 4 board also provides outputs to enable audio and visual indications of mode 4 operation.

a. Status Indicator and Suppression circuits. The mode 4 status indicator and suppression Circuits consist of a 222.222-kHz square wave oscillator (1H9A), a seven–stage ripple counter (1H9B) and three discrete-gate flip-flops (1G6A, 1G6B), (1F6A, 1F6B), and (1E6A, 1E6B) , which provide the timing and monitoring of mode 4 operation. Suppression signals are derived from the outputs of the status indicator flip-flops.

1. Counter (1H9B) is clocked at 4.5-µs intervals by each negative-going edge of the square wave output from oscillator (1H9A). When a mode 4 sync pattern is decoded, the reset input to the counter goes low and the clock pulses are allowed to increment the count. NAND gate (1G8A) senses the third- and fifth-bit outputs of the counter and produces a low output when the counter reaches a count of 20, thereby indicating the end of the 90-µs interrogation video receive period. The counter continues to count until either a disparity condition occurs or a mode 4 reply is transmitted. If neither of these conditions occur, the counter continues to the maximum count of 64 and the seventh-bit output is produced. This output indicates that a reply has not been made within the 288-µs mode 4 operational cycle.

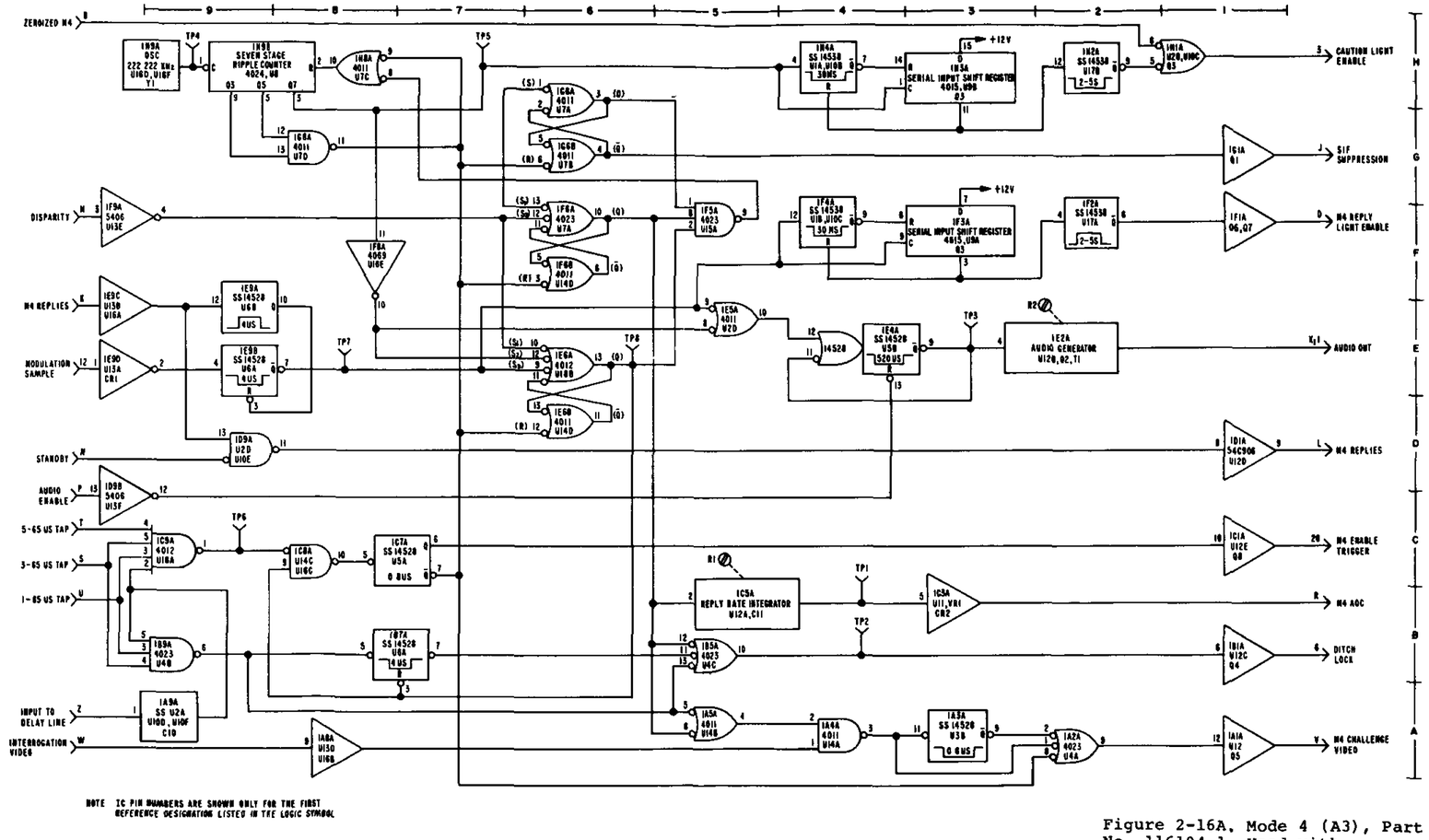


Figure 2-16A. Mode 4 (A3), Part No. 116104-1, Used with RT-859A/APX-72, Logic Diagram

2. Status indicator flip-flops (1G6A, 1G6B), (1F6A, 1F6B), and (1E6A, 1E6B) are reset at the beginning of a mode 4 operational cycle, and are set when specific events occur during the cycle. The states of these flip-flops indicate the status of mode 4 operation.

(a) Flip-flop (1G6A, 1G6B) is in the reset state during the 90-µs interrogation video receive period. While this flip-flop is in the reset state, the (Q) output from (1G6B) is high, transistor Q1 in (1G1A) is on, and an SIF suppression signal is generated. As a result, the SIF mode decoder on decoder board (A2) and the anti-jamming circuitry on detector and video amplifier board (AR3) are disabled. At the end of the interrogation video receive period, the flip-flop is set by NAND gate (1G8A) and the SIF suppression signal is terminated.

(b) Flip-flop (1F6A, 1F6B) is in the reset state when interrogation video is being received and accepted by the mode 4 computer as a valid interrogation. If the mode 4 computer detects a disparity condition in the incoming challenge video, a disparity signal is generated, which is amplified to the required 12-volt level by buffer (1F9A) and then applied to the set input of the flip-flop. When no disparity is detected the flip-flop is set by the output of NAND gate (1G8A).

(c) Flip-flop (1E6A, 1E6B) is in the reset state from the beginning of the mode 4 operational cycle until one of the three set inputs indicate that the cycle is terminated. During normal operation, this indication is provided by the active low output of single-shot (1E9B) when a mode 4 reply has been transmitted (Refer to paragraph 2-22A.e.) If the cycle is terminated by a disparity condition, or when counter (1H9B) reaches the maximum count of 64, the flip-flop is set by buffer (1F9A) or inverter (1F8A), repsectively. Internal suppression is effected by the (Q) output from (1E6A), which prevents the decoding of mode 4 interrogations while the flip-flop is in the reset state.

(d) During the period when the mode 4 board is not processing interrogations, all the status indicator flip-flops are in the set state. This condition is indicated by NAND gate (1F5A) which senses the (Q) outputs of the flip-flops and provides a low output, which, via OR gate (1H8A) holds counter (1H9B) in the reset state.

b. Decoding Circuit. The mode 4 decoding circuit consists of NAND gates (1B9A), (1C9A), and (1C8A) and single-shots (1A9A), (1B7A), and (1C7A). NAND gate (1B9A) generates a three-pulse decode trigger, which is used in the generation of the ditch lock signal, and the first pulse of challenge video. The mode 4 (four-pulse) decode trigger is generated by NAND gate (1C9A) and is used to reset the status indicator circuits, generate the mode 4 enable trigger, and the second pulse of challenge video.

1. The inputs to the mode 4 decoding circuit are the normalized video output from processor (Al), the delayed video outputs from the taps of delay line (DL1) and the internal suppression signal from the (Q) output of flip-flop (1E6A, 1E6B). The normalized video is applied to single-shot (1A9A). Each input pulse to this single-shot enables NAND gate U2A

and causes the output voltage of inverter U10D to be inverted at a rate determined by the discharging of capacitor C10. The output of inverter U10F is high from the time an input pulse is applied to the single–shot until the capacitor discharges below the threshold of NAND gate U2A.

2. The inputs to NAND gate (1C9A) are the output of single-shot (1A9A) and the 1.65-, 3.65-, and 5.65-µs delay line taps. When the first, second, and third delayed pulses of a mode 4 interrogation coincide with the just-received fourth pulse, NAND gate (1C9A) produces the mode 4 decode trigger. If NAND gate (1C8A) is not inhibited by internal suppression, this trigger activates single-shot (1C7A). The mode 4 enable trigger is derived from the (Q) output of the single-shot by buffer (1C1A), where the signal is translated to the 5-volt level required by the mode 4 computer. The (Q) output of the single-shot resets the status indicator flip-flops (paragraph 2-22A.a) on the leading edge and is applied to the interrogation video gating circuit (paragraph 2-22A.d). When the single-shot returns to the quiescent state, the (6) output allows counter (1H9B) to begin counting.

3. NAND gate (1B9A) receives the same inputs as NAND gate (1C9A), except for the 5.65-µs delay line tap. When the first three pulses of a mode 4 interrogation coincide at the inputs of NAND gate (1B9A), a three-pulse decode trigger is generated. This trigger precedes the mode 4 decode trigger by 2 µs, and it is applied to the ditch lock generator circuit (paragraph 2-22A.c), the interrogation video gating circuit (paragraph 2-22A.d), and the trigger input to single-shot (1B7A). This single-shot is only triggered when the internal suppression signal is not present. The output of this single-shot is also applied to the ditch lock generator circuit.

c. Ditch Lock Generator Circuit. The ditch lock signal to processor (A1) is derived from the output of OR gate (1B5A), and is translated to the required 5–volt level by buffer (1B1A). The ditch lock signal is initiated by the three-pulse decode trigger from NAND gate (1B9A), and is maintained by the output of single-shot (1B7A) for 4 µs or until the single-shot is reset as a result of a mode 4 decode trigger. If the later occurs, the low input to the OR gate is provided by the (Q) output of flip-flop (1F6A, 1F6B).

d. Interrogation Video Gating Circuit. Interrogation video from the processor (A1) is amplified to the required 12-volt level by buffer (1A8A). The output of this buffer is gated by NAND gate (1A4A), which is enabled through OR gate (1A5A). The OR gate provides an enabling input when NAND gate (1B9A) provides a three-pulse decode trigger or when flip-flop (1F6A, 1F6B) is reset. The interrogation pulses that pass through NAND gate (1A4A) are shaped by single-shot (1A3A) and OR gate (1A2A) for a minimum pulse width of 0.6 µS. The pulses from OR gate (1A2A) are routed to the mode 4 computer via buffer (1A1A), which translates the signals to the required 5-volt level. This circuit configuration applies a pulse to the mode 4 computer at the third- and fourth-pulse positions of an interrogation. If an SLS pulse appears at the fifth-pulse position, the pulse is also applied to the mode 4 computer, which responds by

generating a disparity signal. The pulse train that follows the fifth-pulse position is designated challenge video, and is applied to the mode 4 computer unless a disparity condition occurs.

e. Mode 4 Replies. Replies from the mode 4 computer are amplified to a 12-volt level by buffer (1E9C). If the standby input from the control transponder set does not inhibit NAND gate (1D9A), replies pass through buffer (1D1A) and are routed to modulator (A7) via encoder clock board (A4). These replies also trigger single-shot (1E9A), which, in turn, enables single–shot (1E9B). In this manner, false triggering of single-shot (1E9B) by erroneous modulation samples fed back from decoder board (A2) via buffer (1E9D) is prevented.

f. Mode 4 AOC. When a valid interrogation is being received, flip-flop (1F6A, 1F6B) is in the reset state and the input to the reply rate integrator (1C5A) is low. As a result, capacitor C11 discharges through buffer U12A as determined by the values of the capacitor, resistors R12 and R13, and potentiometer R1. As the rate of interrogation increases, the mean voltage across the capacitor decreases, which causes a decrease in the output of non-inverting amplifier U11. When the output of this amplifier drops below 7 volts, zener diode VR1 begins to conduct, and the output to decoder board (A2) begins to decrease in a manner that, is proportional to the interrogation rate.

g. Visual and Audio Monitors. The mode 4 board generates a caution light enable, a reply light enable, and an audio output to provide indication of mode 4 performance. The caution light is enabled whenever a minimum of four interrogations remain unanswered at intervals of 30 ms or less, or if the mode 4 reply code is zeroized. The mode 4 reply light is enabled if a minimum of four replies are made at intervals of 30 ms or less. An audio signal, if enabled, is generated whenever a mode 4 reply is transmitted or when an interrogation is not replied to.

1. If counter (1H9B) is not reset before the seventh bit is clocked high, a failure to reply is detected, single-shot (1H4A) is activated and shift register (1H3A) is enabled for at least 30 ms. The serial input to the shift register is always high, so that if another trigger is obtained from the counter while the shift register is still enabled, a logic one is latched in the first stage. The fourth trigger pulse shifts a logic one to the third stage of the shift register. The third–stage output resets single-shot (1H4A) and activates single-shot (1H2A). The caution light is enabled by either the low output of single-shot (1H2A) or the zeroized mode 4 signal, which are applied to OR gate (1H1A). Within (1H1A), the output of OR gate U2B is inverted by U10C, transistor Q3 is turned off, and the caution light enabling line is disconnected from ground.

2. The mode 4 reply light enabling circuit consists of single–shots (1F4A) and (1F2A), and shift register (1F3A), which function in a manner similar to the caution light enabling circuit. The trigger source for this circuit is the output of single-shot (1E9B), which indicates that a reply has been made. The output of single-shot (1F2A)

is applied to lamp driver (1F1A). When the base of transistor Q6 is high, transistor Q7 is on, and the reply light enabling line is raised to a potential of 28 volts.

3. The audio enable signal is applied to single-shot (1E4A) via buffer (1D9B), which inverts and amplifies the signal to a 12-volt level. If enabled, single-shot (1E4A) is activated through OR gate (1E5A), either by the trigger to the reply light enabling circuit or the trigger to the caution light enabling circuit via inverter (1F8A). The (Q) output of single shot (1E4A) is applied to audio generator (1E2A) and is fed back to the trigger disable input of the single-shot to prevent retriggering. The pulses entering the audio generator are applied to isolating transformer T1 via buffer-driver U12B and Q2. Pulse trains resulting from repeated interrogations cause the generator to produce an audio signal.

2-23. ENCODER CLOCK (A4). The encoder clock circuitry (see figure 6-12, sheet 1) provides five general functions: decoded mode storage, generation of clock and direct clock gates, time division and pulse train spacing, phasing of counter outputs and reply codes, and control of modulation triggers for modes 1, 2, 3/A or test, and C. Mode storage is provided by an eight-transistor circuit which stores the decoded mode until another mode is decoded. The clock gates are generated by the clock gate single shot which activates the reply transmission cycle each time a valid interrogation has been decoded. Time division is a function of the encoder counter circuits which provide the intervals for reply code insertion. Phasing of the reply code with the time intervals is accomplished in the encoder matrix circuit. Enabling of coded reply triggers for transmission by the modulator is the function of the transmit control circuitry. See figure 2-17 for the following discussion.

a. Decoded Mode Storage. The mode 1, 2, 3\A or test, and C mode decode trigger inputs to the encoder clock circuit board are applied through terminals B, D, F, and A to inverter amplifiers (1B7B), (1B7D), (1A7A), and (1A7C), respectively. Each mode storage circuit is represented by three logical circuits, namely: a logical NAND, amplifier, and OR. The logical circuits for modes 1, 2, 31A or test, and C, respectively, are as follows: logical NAND (1B6A), (1B6C), (1A6A), and (1A6C); emitter followers (1B6B), (1B6D), (1A6B), and (1A6D); logical OR (1B7A), (1B7C), (1B7E), and (1A7B). A1l four mode storage circuits operate in the same manner; only mode 1 is described. The mode 1 decode trigger input is inverted in (1B7B) and the low output is fed to logical NAND (1B6A) turning transistor Q30 off. The positive output of (1B6A) is fed to emitter follower amplifier (1B6B) which conducts and provides a positive output at its emitter which biases (1B6C), (1A6A), and (1A6C) on, through (1B7C), (1B7E), and (1A7B), respectively. Each of amplifiers (1B6C), (1A6A), and (1A6C) feed back a low input through (1B7A) which holds (1B6A) off. The positive output of (1B6A) is applied through terminal 3 to the encoder control (A5) as the mode 1 enable signal. Replies in mode 1 will be enabled as long as (1B6A) is biased off.

b. Clock Gate Generation. The output of inverter amplifiers (1B7B), (1B7D), (1A7A), and

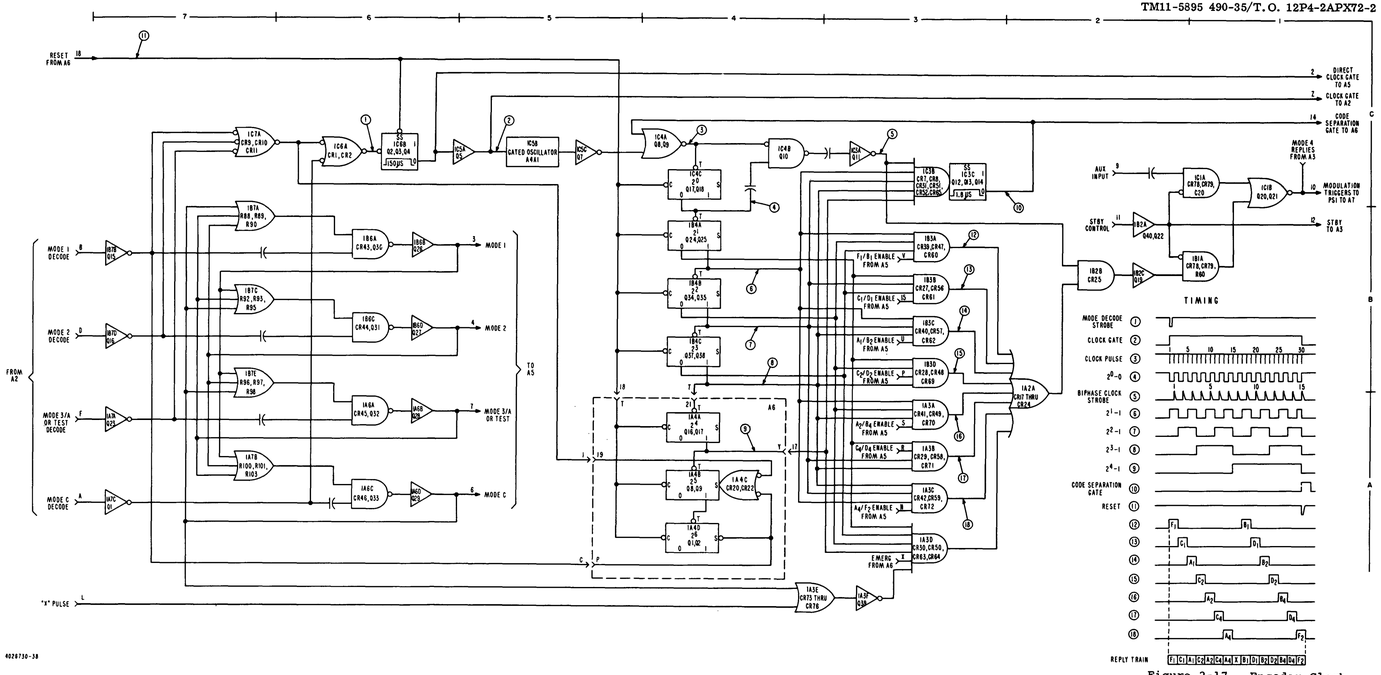


Figure 2-17. Encoder Clock (A4), Logic Diagram

(1A7C), the mode decode strobes, is also applied through logical NOR (1C7A) and logical NOR (1C6A) to 150-µs single shot (1C6B). The input to (1C6B) causes the collector of transistor Q2 to go to ground momentarily, turning off transistor Q4 through capacitor C5. Transistor Q4 will remain off for 150 µs, unless reset, providing a positive pulse which is applied through terminal 2 to the encoder control (A5) as the direct clock gate and to emitter follower (1C5A). The positive output of (1C5A) is the clock gate which is applied to the gated oscillator (1C5B) and through terminal Z to the decoder (A2). The duration of the clock gate is normally 21 µs and is determined by the encoder counters which enable the code separation single shot which activates the reset generator on the encoder gating circuit board (A6). The reset generator applies a clear or reset pulse through terminal 18 to (1C6B) turning transistor Q2 off and allowing transistor Q3 to charge capacitor C5 rapidly. When capacitor C5 is charged, transistor Q4 will turn on ending the single shot operation.

NOTE

TWO gated oscillators are described in this paragraph. For RT-8591APX-72 and early versions of RT-859A/APX-72 see paragraphs 1 and 3 below. For later versions see paragraphs 2 and 3 below.

1. The gated oscillator is a temperature compensated L-C oscillator which establishes the 1.45-µs spacing of the reply pulses. When Q5 (1C5A) turns on, the positive emitter output to (1C5B) causes input transistor A1Q1 to turn off, permitting oscillator (1C5B) to provide a pulse train to pulse shaper Q7 (1C5C) via capacitor C7. The square wave output of (1C5C) is coupled through transistor Q8 of logical NOR (1C4A) to the trigger input of encoder counter 2° (1C4C) providing an input is not present on the base of transistor Q9 of (1C4A).

2. The gated oscillator (figure 6-12, sheet 2) makes use of a 27.586-MHz crystal oscillator, an integrated circuit divide-by-four counter, an an integrated circuit divide-by-five counter. The positive 21-µs output of Q5 (1C5A), after clipping by A1VR1 and double inversion by A1A1C and A1A1B, is used to remove the preset from pins 10 and 13 of divide-by-four counter A1A2. The two flip-flops of A1A2 start counting, clocked by the crystal oscillator. The 6.8965-MHz output of A1A2 clocks divide-by-five counter A1A3, which provides a 1.3793-MHz pulse train to inverter A1A1F. The 0.725-µs pulse train output of A1A1F is applied to pulse shaper Q7 via capacitor C7.

3. As described below, (1C4C) provides a negative-going output at its 0 terminal on every other 0.725-µs pulse input at its trigger terminal. This results in the 1.45-µs spacing of reply pulses.

Encoder Counter Circuits (figure 2-17). The encoder counting circuit consists of seven flip-flops (1C4C), (1B4A), (1B4B), (1B4C), (1A4A), (1A4B) and (1A4D), which operate as 2^0 through 2^6 counters. The 2^4 through 26 (1A4A), (1A4B), and (1A4D) counters are on the encoder gating circuit board (A6). The 0 outputs of

(1C4C), (1B4A), (1B4B), and (1B4D) are, respectively, the collectors of transistors Q18, Q24, Q34, and Q37, and the 1 outputs the collectors of transistors Q17, Q25, Q35, and Q38. On the encoder gating circuit board (A6) the 0 outputs of (1A4A), (1A4B), and (1A4D) are, respectively, the collectors of transistors Q16, Q8, and Q1 and the 1 outputs the collectors of transistors Q17, Q9, and Q2, Initially (1C4C) is triggered by the negative clock pulse of logical NOR (1C4A) and, in turn, (1C4C) triggers (1B4A) through its 0 output when it goes to ground potential. The 1 outputs of the remaining counters are used to trigger the following stages when the 1 outputs are negative going. Connected in this manner, (1C4C) will change state on every negative-going pulse from (1C5B) providing a negative-going output at the 0 terminal on every other trigger input. (1B4A) will then trigger on every second pulse from (1C5B), (1B4B) on every fourth clock pulse, (1B4C) on every eigth clock pulse, (1A4A) on every sixteenth clock pulse, (1A4B) on every thirty-second clock pulse, and (1A4D) on every sixty-fourth clock pulse as shown in the timing diagram. The counter outputs are applied to the encoder matrix where they combine with the outputs of the encoder control (A5) to provide the coded reply pulse positions. The 0 output of (1C4C) is also applied to logical NAND (1C4B) enabling it so that when a negative input from (1C4A) coincides with a positive input from (1C4C) a low output will be ac coupled to invert amplifier (1C3A). The low input to (1C3A) is inverted providing a positive output to logical AND (1C3B) and logical AND (1B2B). On the 30th count of the binary counters, (1B4A), (1B4B), (1B4C), and (1A4A) will provide a positive level at the 1 outputs enabling (1C3B) which will activate and trigger 1.81-µs single shot (1C3C) when the next positive output is received from (1C3A). This positive input feeds through diode CR8 causing (1C3C) to operate. The positive input causes transistor Q12 to conduct, coupling a negative-going signal to the base of transistor Q14, shutting it off. The collector of transistor Q14 goes positive causing transistor Q13 to conduct. At the end of the strobe pulse from (1C3A) transistor Q12 will turn off but transistor Q13 will continue to conduct until the charge on capacitor C11 has reduced to the level at which transistor Q14 will again conduct. The output of (1C3C) is the code separation gate, which is fed back to logical NOR (1C4A) inhibiting clock pulses from triggering the encoder counter and applied through terminal 14 to trigger the reset generator on encoder gating circuit board (A6).

d. Encoder Matrix Circuit. The encoder matrix is shown as a series of logical AND circuits in which outputs of the encoder counters and inputs from the encoder control circuit board (A5) are combined to provide the reply code timing. These logical AND circuits consist of the following: (1B3A), (1B3B), (1B3C), (1B3D), (1A3A), (1A3B), (1A3C), (1A3D). Logical AND (1B3A) provides an output when diode CR17 (1A2A) becomes forward biased. To activate (1B3A), counter (1B4A) must provide a positive pulse from its 1 output, (1B4B) and (1B4C) a positive pulse from their 0 outputs, and terminal V a positive input from encoder

control (A5). When (1B3A) is activated, a positive output is applied through logical OR (1A2A) to enable logical AND (1B2B) the other input of which is diode CR25. With (1B2B) enabled, a positive input from (1C3A) will reverse bias diode CR25 causing transistor amplifier Q19 (1B2C) to conduct and provide a positive output from its emitter to the transmit control circuit. All other encoder matrix circuits function in the same manner. The X pulse control, which is associated with the encoder matrix, consists of logical OR (1A3E) and inverter amplifier (1A3F). Transistor Q39 (1A3F) is normally conducting providing a low input to logical AND (1A3D) and disabling it. When a mode C code is stored, a positive input is applied to (1A3E) causing a high output to (1A3F) which will cause transistor Q39 to conduct preventing X pulse operation. When mode C is not stored, a low input is applied to (1A3E) and an X pulse enabling input through terminal L will bias (1A3F) off enabling (1A3D) and provide an X pulse in the proper time slot.

e. Transmit Control Circuit. The operation of the transmit control circuit is centered in logical NOR (1C1B). When the MASTER switch on the C-6280 (P)/APX is in STBY, an open appears at the input of inverter amplifier (1B2A). Transistor Q40 will conduct turning off transistor Q22, disabling (1B1A) and (1C1A), and provide an inhibit to mode 4 operation through terminal 12. When the MASTER switch is in LOW or NORM, a ground is applied to (1B2A) turning off transistor Q40 and causing transistor Q22 to conduct enabling (1B1A) and (1C1A). A positive auxiliary input to the enabled (1C1A) will cause a positive output to logical NOR (1C1B) and transistor Q21 will conduct providing negative trigger pulses through the power supply (PS1) connection to the modulator (A7). Likewise, a positive output from (1B2C) activates the enabled (1B1A) providing a positive input to (1C1B) causing similar action.

2-24. ENCODER CONTROL (A5). The primary function of the encoder control circuitry (see figure 6-13) is to store the programmed coded mode inputs for modes 1, 2, 3\A, and C until a decoded mode enable trigger releases it for transmission. The preset coded mode inputs for modes 1, 3\A, and 2 are the thumb-wheel switches on the C-6280(P)\APX and the front panel of the RT-859/APX-72, respectively. Refer to table 2-2 for correlation of dial settings and pulse designations. The mode C inputs are received from the pressure altitude digitizer. Each coded mode input to the encoder control furnishes a ground for the selected pulse which will inhibit operation of the outputs (1B1A) through (1B1G) for the selected mode when in normal operation. (See figure 2-18). When (1B1A) through (1B1G) are inhibited, a positive pulse is applied to the encoder matrix of the encoder clock (A4) for transmission in its proper time slot. To obtain a positive output from any one of these circuits, all inputs must be low. A high input to any given circuit will cause a low output from that circuit. During each transmission each of these circuits is sampled twice. When the 2^4 - 0 counter output is positive, the output circuits are sampled for F_1, C_1, A_1, C_2, A_2, C_4, and A_4 pulses; when the 2^4 - 1 counter-output is positive, the circuits are sampled for B1, D1, B2, D2, B4, D4, and F2 pulses. The F1 and F2 pulses will always

be generated, and the El input from the encoder gating circuit board (A6) through terminal 65 and logical AND circuits (1B4A) and (1B4B) , will inhibit B1 and A4 pulses during the last three frames of an emergency reply.

Mode 1 Circuitry. The mode 1 code set in the thumbwheel switches on the C-6280(P)\APX applies a ground through terminals 28, 61, 27, 60, and 26 to logical AND circuits (1A4A) through (1A4E). Whenever a ground is applied to either of these logical AND circuits, their outputs remain low or at ground and will function to bias off associated output logical NOR circuits (1B1A) through (1B1G) and provide a positive output to encoder matrix on encoder clock (A4). To understand mode 1 operation, assume a mode 1 dial setting of 52 on the C-6280 (P)\APX with Ml IN. From table 2-2, we find that inputs A1, A4, and B2 on figure 2-18 will be at ground potential. When a decoded Ml storage signal is received at terminal 2, a positive input is applied to logical AND circuits (1A4F) and (1A4H). At the same time, a positive direct clock gate and a positive 2^4 - 0 pulse activates (1A4F) applying a positive input to (1A4A) through (1A4C) for the first half of the clock gate. Since 2^4 - 1 is negative at this time, (1A4H) will be disabled. With (1A4A) and (1A4C) disabled by the ground potential, applied through A1 and A4, their outputs will be causing (1B1C) and (1B1G) to provide a positive output. The open at the A2 input appears as a positive input to enabled (1A4B) providing a positive output which disables (1B1G) providing a low output for the first half of the clock gate. The output at this time will be F_1, A_1, and A_4 (1B1A), (1B1C), and (1B1G), respectively. After a count of 15, 2^4 - 0 goes to ground, 24 - 1 goes positive, (1A4F) is disabled, and (1A4H) provides a positive input to (1A4D), (1A4E), and (1B1E). The open at B1 activates (1A4D) which disables (1B1A) providing a low output. The ground potential at B2 disables (1A4E) which disables (1B1C) providing a high output. The output for the second half of the clock gate will be B2 and F2 (1B1C) and (1B1G), respectively. There is no B4 pulse present in a mode 1 reply code. This pulse is inhibited by feeding the output of (1A4H) which is positive during the second half of the clock gate into (1B1E) by CR18. In mode 1, operation C and D pulses are not used. Output circuits (1B1B), (1B1D), and (1B1F) are disabled by the emergency gates which applies a positive 12-volt input through terminal 5, when in mode 1 or emergency position. The composite reply code, applied to the encoder matrix of encoder clock (A4), will be F1, A1, A4, B2, and F2, representing a mode 1 dial setting of 52.

b. Mode 2 Circuitry. The mode 2 code set in the thumbwheel switches on the front panel applies a ground through terminals 59, 58, 25, 24, 57, 23, 22, 21, 55, 54, 20, and 53 to logical AND circuits (1A3A) through (1A3M). The enabling inputs for mode 2 are logical AND circuits (1A4G) and (1A4J). The operation of mode 2 is identical to mode 1 with the exception that all outputs (1B1A) through (1B1G) are used in normal operation since the emergency gate will be disabled in modes 2, 3\A, and C during the first frame. Refer to paragraph 2-24, step a for detailed description of circuit operation.

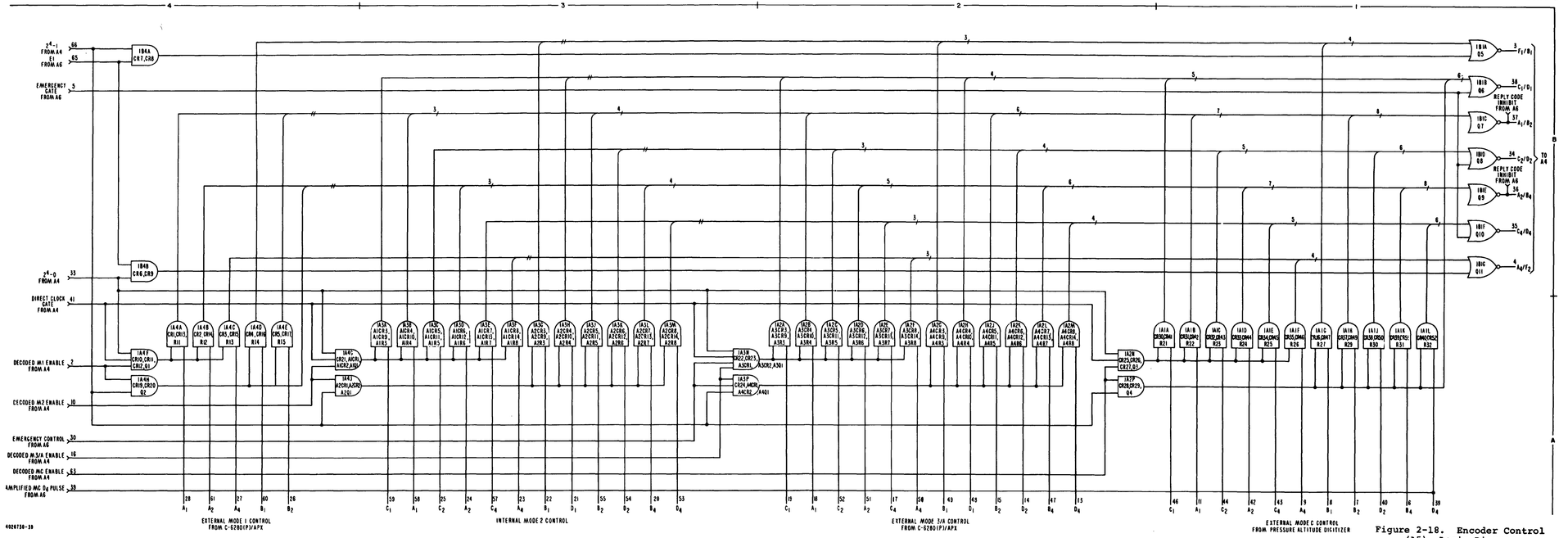


Figure 2-18. Encoder Control (A5), Logic Diagram

c. Mode 3/A Circuitry. The mode 3\A code set in the thumbwheel switches on the C-6280(P)\APX applies a ground through terminals 19, 18, 52, 51, 17, 50, 49, 48, 15, 14, 47, and 13 to logical AND circuits (1A2A) through (1A2M). The enabling inputs for mode 3\A are logical AND circuits (1A3N) and (1A3P). An additional emergency input is applied to (1A3N) and (1A3P) which will apply a ground to these circuits disabling them when the MASTER switch on the C-6280(P)\APX is in the EMER position. In normal operation, mode 3/A is identical to mode 2. Refer to paragraph 2-24a. for detailed description of circuit operation.

d. Mode C Circuitry. The mode C code is obtained from an external pressure altitude digitizer through terminals 46, 11, 44, 42, 43, 9, 8, 7, 40, 6, and 39 to logical AND circuits (1A1A) through (1A1L). The enabling inputs for mode C are logical AND circuits (1A2N) and (1A2P). There is no D1 pulse present in the mode C reply code. This pulse is inhibited by feeding the output of (1A2P) which is positive during the second half of the clock gate, into (1B1B) by diode CR48. In normal operation, mode C is identical to mode 2. Exceptions are: the source of the coded inputs, the use of resistance-capacitance filters, and the type of control leads used. The filters are used to integrate any transients that may appear on the control lines to ensure smooth operation when the altitude digitizer changes code settings due to changes in altitude. The control leads may be either resistance or voltage controlled; that is, a pulse may be transmitted by controlling the resistance or the voltage applied to the control leads. Refer to paragraph 2-24a for a detailed description of circuit operation.

NOTE

All references to mode C SPI or caboose pulse, in the following paragraph, apply for RT-859\APX-72 only.

2-25. ENCODER GATING (A6). The primary functions of the encoder gating circuitry (see figure 6-14 (RT-859/APX-72) or 6-15 (RT-859A/APX-72)) are to provide: a reset pulse for clearing the 2° through 2^{6} counters, an identification of position (I/P) signal, an emergency signal, and a regenerated D4 or caboose pulse. When activated, the reset generator returns all counters to the reset or clear state (O output positive, 1 output ground) ready to begin a new counting sequence. The I\P pulse is generated to enable an interrogating facility to distinguish a specific transponder carrier from a group replying in the same code. The emergency signal indicates that an emergency condition exists aboard the transponder carrier transmitting the reply. The SPI or caboose pulse is generated to indicate that the transponder carrier has exceeded a predetermined altitude. See figure 2-19 (RT-859\APX-72) or 2-20 (RT-859A\APX-72) for the following discussion.

a. Reset Generator. The reset generator (1C1A) is a single shot-which, when activated, provides a 2.1 µs output which clears or resets the 2^{4} to 2^{6} counters, (1B3A), (1B3B), (1A3B); the emergency flip-flop (1A2A); and through terminal T to the encoder clock (A4) to reset the

2^0 to 2^3 counters; and the clock gate single shot. The 0 outputs of (1B3A), (1B3B), (1A3B), and (1A2A) are respectively the collector of transistors Q16, Q8, Q1, and Q15, and the 1 output the collectors of transistors Q17, Q9, Q2, and Q14. The trigger input to (1C1A) under normal and emergency operation is the code separation gate applied through terminal U to logical AND (1B2B). Under normal operation all inputs to (1B2B) will be positive when the code separation gate arrives and its positive output will trigger transistor Q3 (1C1A). When in emergency operation, the code separation gate input to (1B2B) is inhibited for the first three frames by the outputs of (1B3B) and (1A3B) which are alternately positive and negative (see figure 2-23). After the third frame both (1B3B) and (1A3B) 0 outputs go positive and the next code separation gate will activate (1B2B) and trigger (1C1A). When in I/P operation in modes 2 or 31A, the code separation gate is inhibited at the end of the first frame by (1B2B) which is disabled by the low output of transistor Q18 (1C3C) for the duration of the I/P timing cycle. The output of (1C3C) is also fed through logical OR (1C2A) to enable loical AND (1C2B). When the 2^2 - 1 input at terminal 17 and the 1 output of (1B3B) go positive on the 35th count, logical NAND (1B2A) is activated. When transistor Q10 conducts, capacitor C15 (1C2B) discharges, triggering (1C1A) through diode CR8.

b. I/P Operation. An I/P reply is enabled when the IDENT-OUT-MIC switch on the C-6280(P)/APX is placed in IDENT applying a ground through terminal 6 to set flip-flop (1C4B). The ground input turns transistor Q20 off, providing a positive output on its collector which is applied to the 15-30-sec delay generator (1C4C) and to logical AND (1C3A). The input to (1C4C), which consists of transistor Q22, capacitors C23, C24, diode CR42, and thermistor RT1, causes capacitor C24 to charge. After approxi–mately 15 to 30 seconds, the potential on capacitor C24 is sufficient to cause transistor Q22 to conduct and clear (1C4B) turning transistor Q21 off and Q20 on. During the 15 to 30 seconds, the positive input to (1C3A), which is enabled except in emergency operation, provides a positive output causing inverter amplifier (1C3B) to conduct. When (1C3B) conducts, it provides a path to ground for emitter of transistor Q18, logical AND (1C3C), and also removes the high reverse bias from diodes CR20 and CR2 by enabling logical AND (1A4B). The circuitry is now set and will generate an I\P reply whenever a mode 1, 2, or 3/A interrogation is decoded.

1. In mode 1, the I/P reply consists of two frames containing normal replies (see figure 2-6). When a mode 1 interrogation is decoded the 2^5 and 2^6 set input is applied through terminal P activating (1A4B). The output of (1A4B) sets (1A3B) directly and (1B3B) through logical OR (1A3A). When (1B3B) and (1A3B) are set, their 0 outputs are low disabling (1B2B). Operation of (1C1A) will be inhibited until normal counter operation triggers (1B3B) and (1A3A) to clear state enabling (1B2B). When the code separation gate is applied through terminal U at the end of the first frame (see figure 2-21), (1B2B) is still disabled and the second frame of the I/P response will be

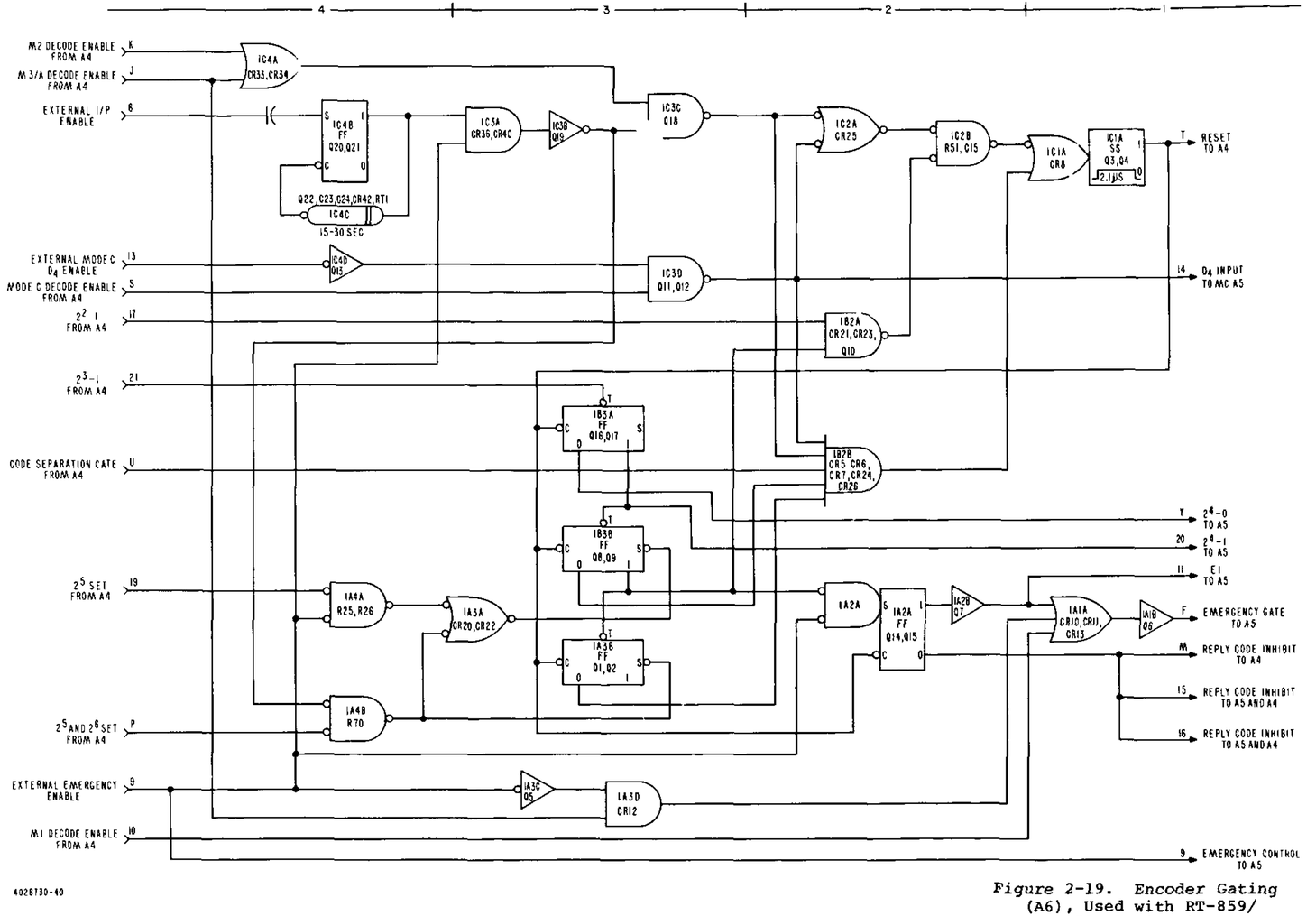


Figure 2-19. Encoder Gating (A6), Used with RT-859/ APX-72, Logic Diagram

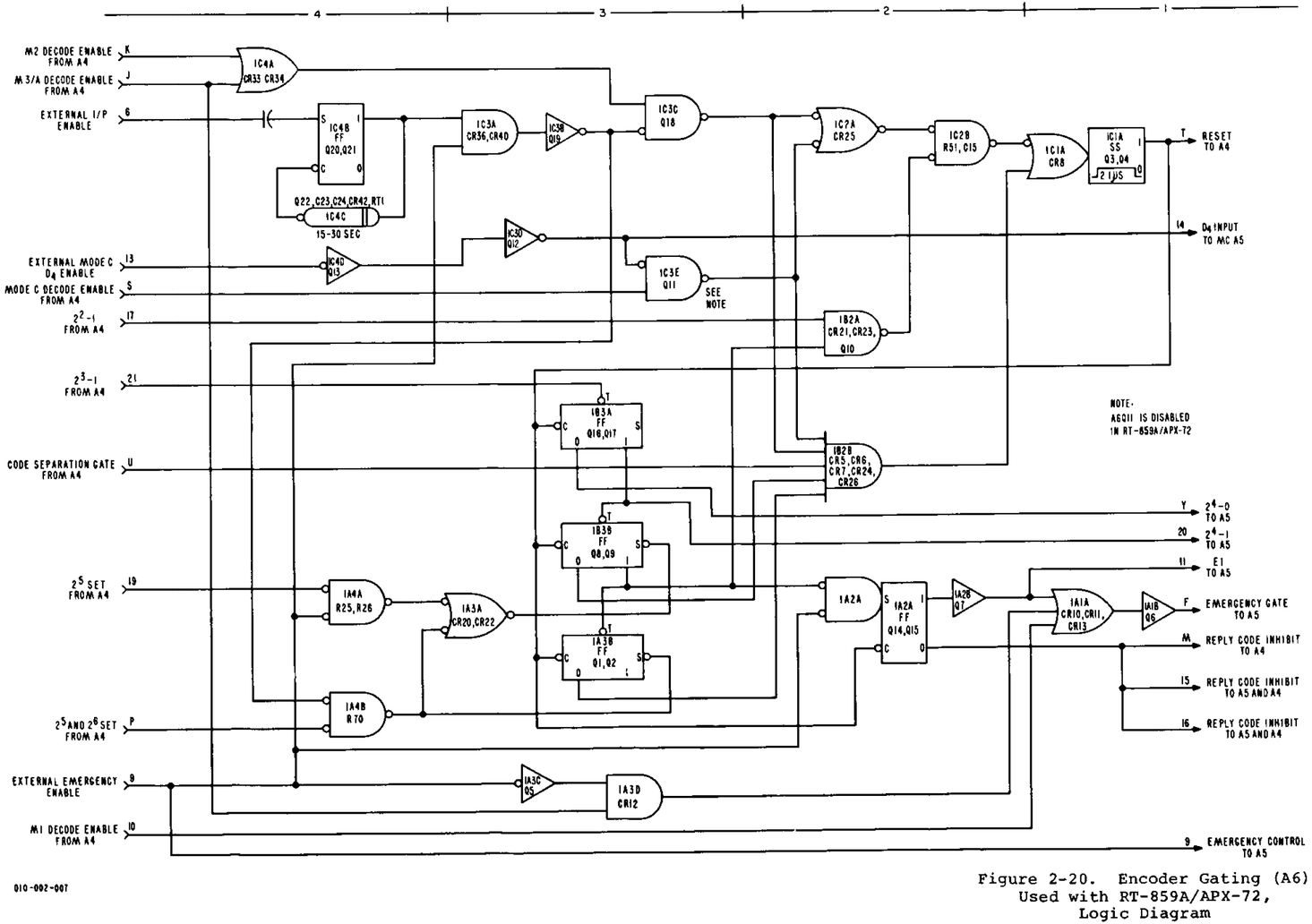


Figure 2-20. Encoder Gating (A6) Used with RT-859A/APX-72, Logic Diagram

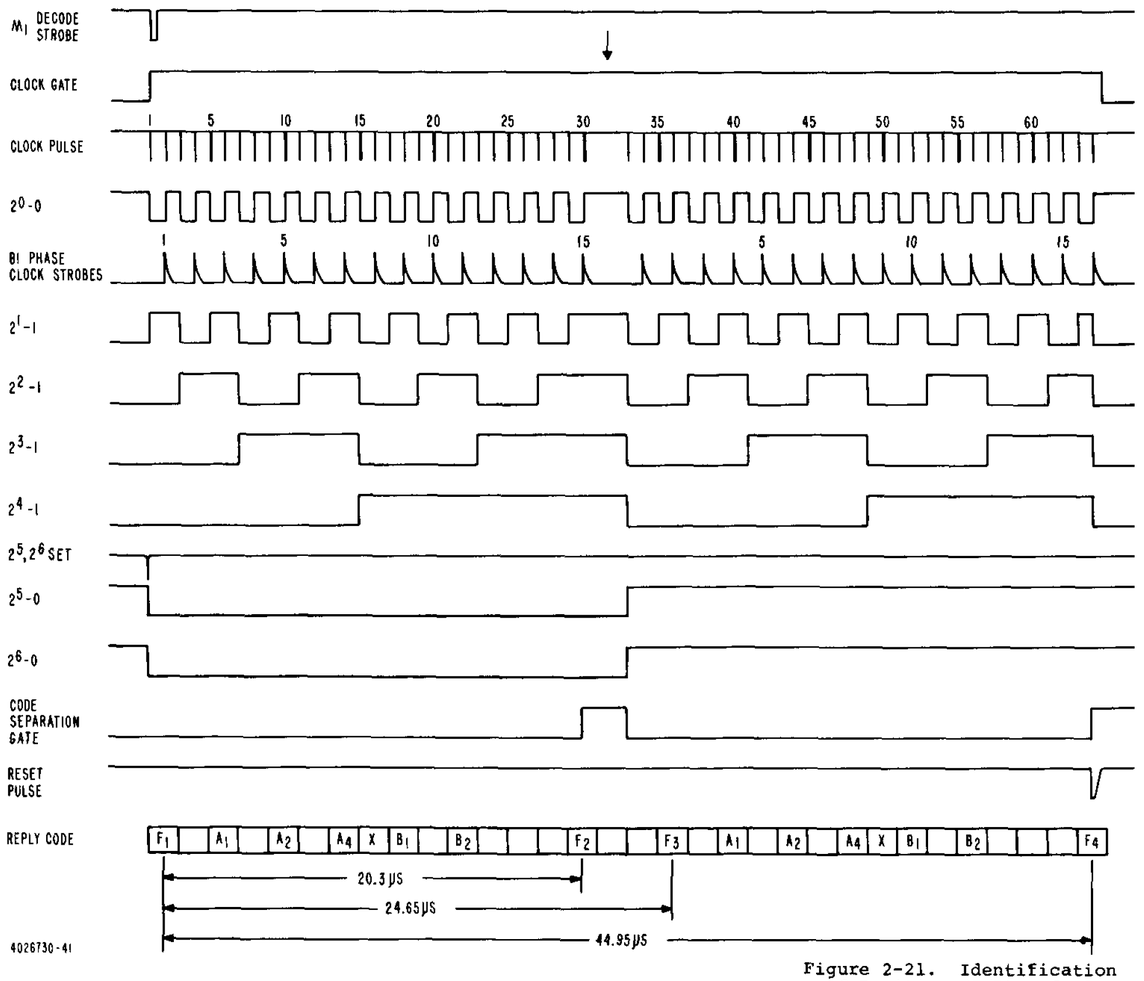


Figure 2-21. Identification of Position (I/P) Mode 1 Operation, Timing Diagram

transmitted. During this transmission, the 0 outputs of (1B3B) and (1A3B) will go positive enabling (1B2B) so that when the code separation gate is applied at the end of the second frame (1B2B) will activate and trigger (1C1A).

2. In modes 2 and 3/A, the I/P reply consists of a single frame containing the normal reply followed by an SPI pulse (see figure 2-6). Either a mode 2 or 3/A decode mode storage input, applied through terminal K or J, will activate logical OR (1C4A) and provide a positive input to the base of transistor Q18 (1C3C). With I/P enabled, (1C3C) will provide a low output to (1C2A) and to disable (1B2B) preventing triggering of (1C1A) by the code separation gate at the end of the first frame. The low output of (1C2A) enables (1C2B). The counters will continue to count and at the end of the 36th clockpulse an F3 pulse will be developed (see figure 2-22). On the 37th clockpulse (1B2A) will be activated by the 2^2 - 1 input through terminal 17 and a positive 1 output from (1B3B). Capacitor C15 will discharge through Q10 (1B2A) triggering (1C1A) and return the system to the start position awaiting a new interrogation.

c. Emergency Operation. The emergency reply to a mode 1, 2, or 3/A interrogation (emergency does not affect modes 4 or C) consists of four frames (see figure 2-6). In modes 1 and 2, the first frame contains the normal reply code followed by three frames containing only framing pulses. In mode 3/A, the first frame contains the code for 7700 and the following three frames contain only framing pulses. To provide these replies, the encoder gating circuitry provides for inhibiting the reset generator for three frames; the elimination of unwanted pulses in the last three frames; the elimination of mode 3/A normal replies; and the insertion of the mode 3/A special reply. The logic associated with emergency operation is shown in figure 2-19. The emergency operation is enabled when the MASTER switch on the C-6280(P)/APX is placed in EMER thus applying a ground to terminal 9 on the encoder gating circuit board (A6). This ground is applied simultaneously to terminal 30 on the encoder control (A5) disabling the mode 3/A switch inputs. The ground on terminal AND (1C3A) and inhibits I/P operation; enables the emergency flip-flop (1A2A); enables logical AND (1A4A); and turns off inverter amplifier (1A3C).

1. The reset generator (1C1A) is inhibited from operating, after each of the first three frames, by disabling (1B2B) during the periods the code separation gate is applied (see figure 2-23). Logical AND (1A4A) is activated by the 2^5 set pulse applied through terminal 19 whenever a mode 1, 2, or 3/A interrogation is decoded. When the external emergency is enabled, the low input activates (1A4A) feeding a low output through (1A3A) to set (1B3B). The 0 output of (1B3B) will remain low until triggered by (1B3A) at which time the 1 output of (1B3B) will trigger (1A3B) causing its 0 output to go low. The 0 outputs of (1B3B) and (1A3B) will disable (1B2B) during the periods the first three code separation gates are applied. After the third frame, both (1B3B) and (1A3B) are triggered positive, enabling

(1B2B) to be activated by the fourth code separation gate and trigger (1C1A). The timing diagram (figure 2-23) is the same for all modes; only the reply code in the first frame changes.

2. In modes 1 and 2, the first frame contains the normal reply code. The coded pulses, except for the framing pulses, are eliminated from the last three frames. The external emergency enable, through terminal 9, enables the set trigger of (1A2A). After the first frame, (1A2A) is set by a low input from the 1 output of (1B3B). In the set position, a low output is fed from the 0 output of (1A2A) providing: a reply code inhibit to encoder matrix (A4), to inhibit the "X" pulse and a reply code inhibit of A_1/B_2 and A_2/B_4 pulses to encoder control (A5) and encoder clock (A4) during the last three frames of the emergency reply. The 1 output of (1A2A) applies a positive input to amplifier (1A2B). The output of (1A2B) provides a positive pulse (E1) which is applied through terminal 11 to encoder control (A5). The E1 pulse enables two logical AND circuits which are activated by the 2^4 - 0 and 2 - 1 outputs to inhibit the B1 and A4 outputs during the last three frames. A second output of (1A2B) is applied through (1A1A) to (1A1B). The output of (1A1B) is applied as the emergency gate (also in mode 1 normal operation) through terminal F to encoder control (A5) to inhibit all C and D pulses during the last three frames.

3. In mode 3/A, the first frame contains code 7700 followed by three blank frames (see figure 2-6). The external emergency enable applied at terminal 9 is also connected to encoder control (A5) to inhibit the mode 3/A coded inputs. In this inhibited condition, an output code of 7777 will be developed on the encoder control (A5). The mode 3/A decode mode storage input through terminal J activates logical AND (1A3D) through diode CR12. This circuit was also enabled by the output of inverter amplifier (1A3C). The output of (1A3D) is applied through (1A1A), (1A1B), and terminal F to encoder control (A5) to eliminate the C/D pulses and change the 7777 code to 7700. After the first frame (1B3B) is triggered by (1B3A) providing a low output which triggers (1A2A. In the set position, (1A2A) provides a high input to (1A2B) the output of which is the E1 pulse which eliminates the B1 and A_4 pulses through (1A1A) and (1A1B), the emergency gate, which eliminates the C/D pulses. The 0 output of (1A2A) provides the reply code inhibit to encoder control (A5) and encoder clock (A4) to eliminate the A_1/B_2, A_2/B_4, and X pulses .

d. Caboose Pulse. For RT-859/APX-72 only, whenever a D4 pulse is present in the mode C reply, the normal reply train is followed by a single framing pulse (see figure 2-6) called the special position indicator (SPI). The external mode C D_4 enable is applied through terminal 13 to inverter amplifier (1C4D). Transistor Q13 turns off providing a positive output enabling logical NAND (1C3D). The mode C decode mode storage input through terminal S activates (1C3D) providing a low output to (1B2B); through terminal 14 to encoder control (A5); and to (1C2A). The input to (1B2B) disables the circuit and prevents triggering of (1C1A) at the end of the first frame. The input to the encoder control

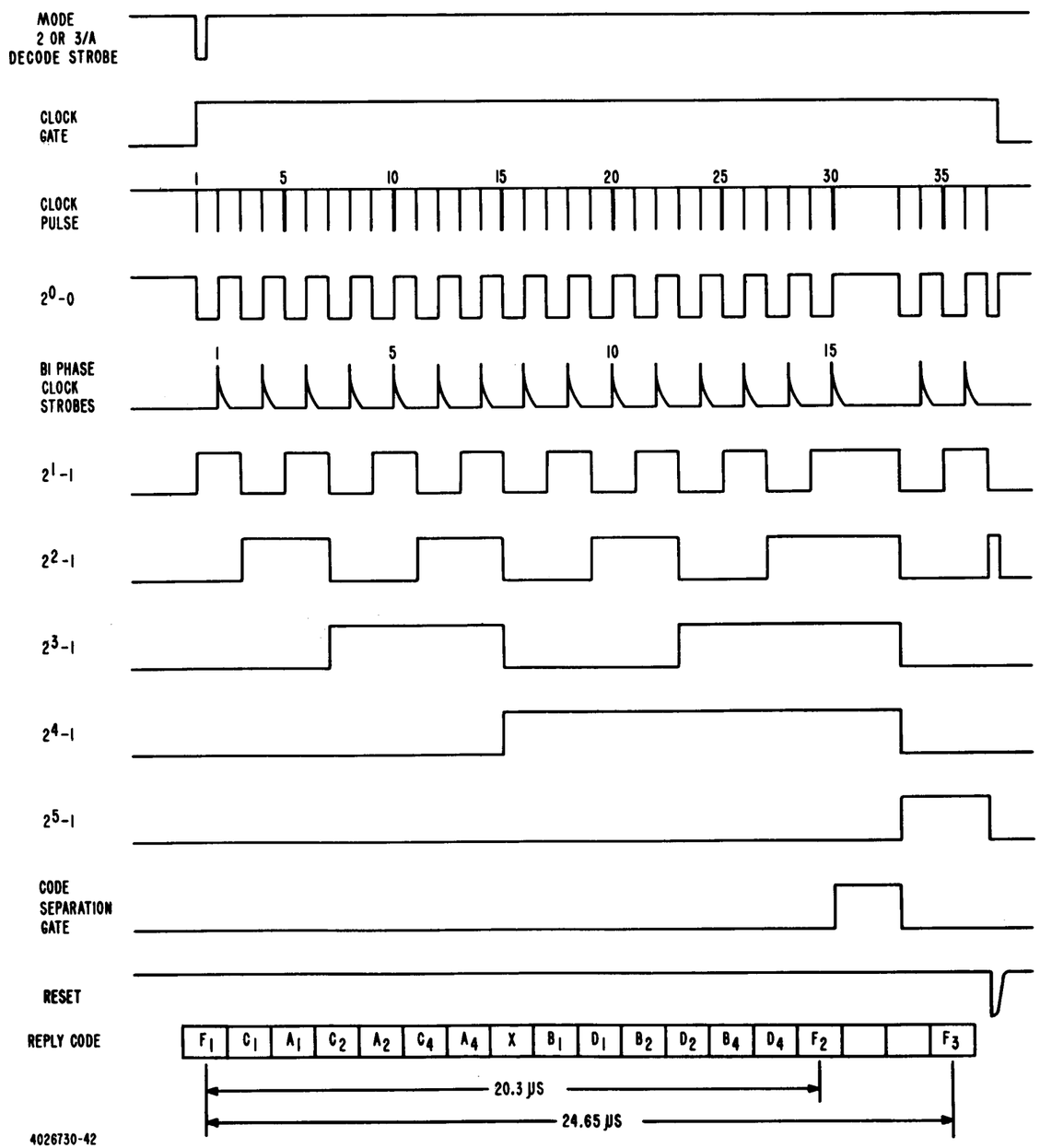


Figure 2-22. Identification of Position (I/P) Modes 2 and 3/A, Operation, Timing Diagram

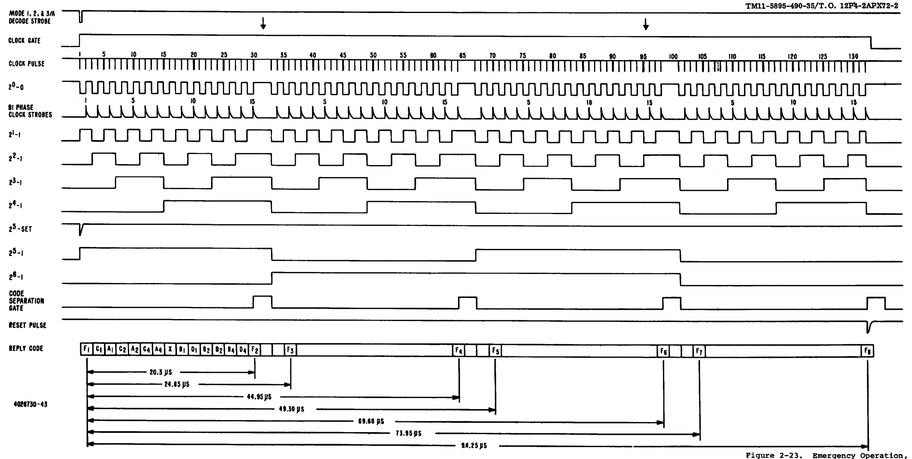


Figure 2-23. Emergency Operation, Timing Diagram

(A5) provides for display of the D4 pulse in the mode C reply. The input to (1C2A) enables (1C2B). The F3 framing pulse or SPI pulse is generated on the 36th count. When the 2^2 - 1 input through terminal 17 and (1B3B) 1 output go positive on the 37th count (see figure 2-22), (1B2A) is activated providing a low output which activates (1C2B) and triggers (1C1A).

2-26. TRANSMITTER. The transmitter consists of the modulator, oscillator, and power amplifier. The mode 1, 2, 3/A, TEST, C, and mode 4 replies are connected from the output of the encoder clock (A4) through the power supply (PS1) to the input of the modulator. The modulator determines the pulse width and provides the driver voltage for the oscillator. The oscillator operates on a frequency of 1090 MHz providing a puised output to the power amplifier which amplifies the oscillator input to a minimum power output of 500 Watts. Refer to paragraph 2-14 for a discussion of diplexer (CP1).

a. Modulator (A7). The modulator (see figure 6-16) is triggered by the negative input to terminal 2 which is either the mode 1, 2, 3/A, TEST, or C reply from the encoder clock (A4) or the mode 4 reply. The trigger input is coupled through capacitor Cl to the junction of the collector of transistor Q1 and pin 3 of transformer T2. A positive pulse is developed between pins 1 and 2 of transformer T3 which is applied to the base of transistor Q1 causing it to conduct and its collector voltage to go to ground. The resulting voltage change across pins 3 and 4 of transformer T2 is inverted in pins 5 and 6 developing a positive input to the base of transistor Q4. Transistor Q4 will conduct causing current flow through resistors R13, R14, and the primary of transformer T1. A positive-going pulse is developed in the secondary of transformer T1, which is coupled through resistor R16 to the base of transistor Q5, causing it to conduct. When transistor Q5 conducts, the -80 volts on its emitter will increase positively to a level just below ground. This pulse is applied, through parallel resistors R18 and R19 and terminal 8, to the grid of oscillator (22). When transistor Q5 turns off, the modulator output will drop to -80 vdc, stopping oscillations. Variable resistor R4, connected to the emitter of transistor Q1, is the modulator pulse width adjustment. Sensitor RT1 is a positive coefficient linear device which stabilizes transistor Q1 for temperature changes.

b. Oscillator (Z2). The oscillator is a tuned cavity pencil tube (see figure 4-17). The equivalent circuit of the oscillator would be that of a tuned-plate, tuned cathode oscillator with input signal applied at the grid. In the quiescent state, a -80 Vdc bias is applied to the grid through terminal 2 from the modulator. When the modulator operates, the -80 vdc bias goes to a value slightly below ground allowing the oscillator to oscillate at a frequency of 1090 MHz for the period the bias is removed. The output of the oscillator is applied through J1 to the power amplifier.

c. Power Amplifier (AR2). The power amplifier is a tuned cavity pencil tube (see figure 4-17). The input to the power amplifier is through terminal J2 from the

oscillator (see figure 6-21). This input is amplified to a minimum power output of 500 Watts and fed through terminal J1 to the diplexer (CP1). The 1000 vdc input to the power amplifier passes through a toroid transformer T1 (see figures 4-17 and 6-21). When the amplifier conducts, the current in the 1000 vdc line is sampled developing an output in transformer T1 which is fed back to decoder (A2) and mode 4 (A3) circuit boards as the modulation sample.

2-27. POWER SUPPLY (PS1). The power supply (see figure 6-17) operates on inputs of either 21 to 29 vdc or 107-122 vac, 400 Hertz. The output voltages, maximum load currents, and general electrical characteristics are listed in table 2-3. The power supply provides all of the voltages required for normal operation of the receiver-transmitter. The power supply provides six major functions: 400 Hertz transformation and rectification; input filtering; switching regulation; inverter driving; output rectification and filtering; and overcurrent protection. See figure 2-24 for the following discussion.

Table 2-3. Power Supply (PS1), Electrical Characteristics

VOLTAGE	CURRENT	ACCURACY	REGULATION	RIPPLE	POWER (W)
1000	0-19.5 mA*	+10% -0%	±2.5%	0.5%	19.50
-110	40 mA	+5 -0%	±5%	1%	4.40
+6	180 mA	±3%	±3%	1%	1.08
-6	160 mA	±3%	±3%	2%	0.96
+12	500 mA	±3%	±2%	0.5%	6.00
+25	40 mA	!	!	0.5%	1.00
-80	1mA	±3%	±3%	0.5%	0.08
+6.3	1.75 A	±3%	±3%	4%	11.20

*1.95-amp pulses at 1% duty cycle. ! Sum of accuracy + regulation = ±5% maximum.

a. 400 Hertz Transformation and Rectification. The 400 Hertz transformer and rectifier provides a full wave rectifier circuit consisting of transformer T1 and diodes CR1 and CR2. The 115 vac input is balanced with respect to ground, allowing either side to be grounded. The output of diodes CR1 and CR2 is applied to inductor L1, the input to the filter assembly.

b. Input Filtering. The filter consists of inductor L1 and capacitors C2 through C8. The external 28 vdc input through terminals 7 and 8 or the rectified ac from diodes CR1 and CR2 is applied to inductor L1. The filter components function to remove the harmonic ripple of the rectified ac input and to provide protection against power line transients. When the ac input is at 115 V 400 Hz, the nominal value of dc input is 29 volts.

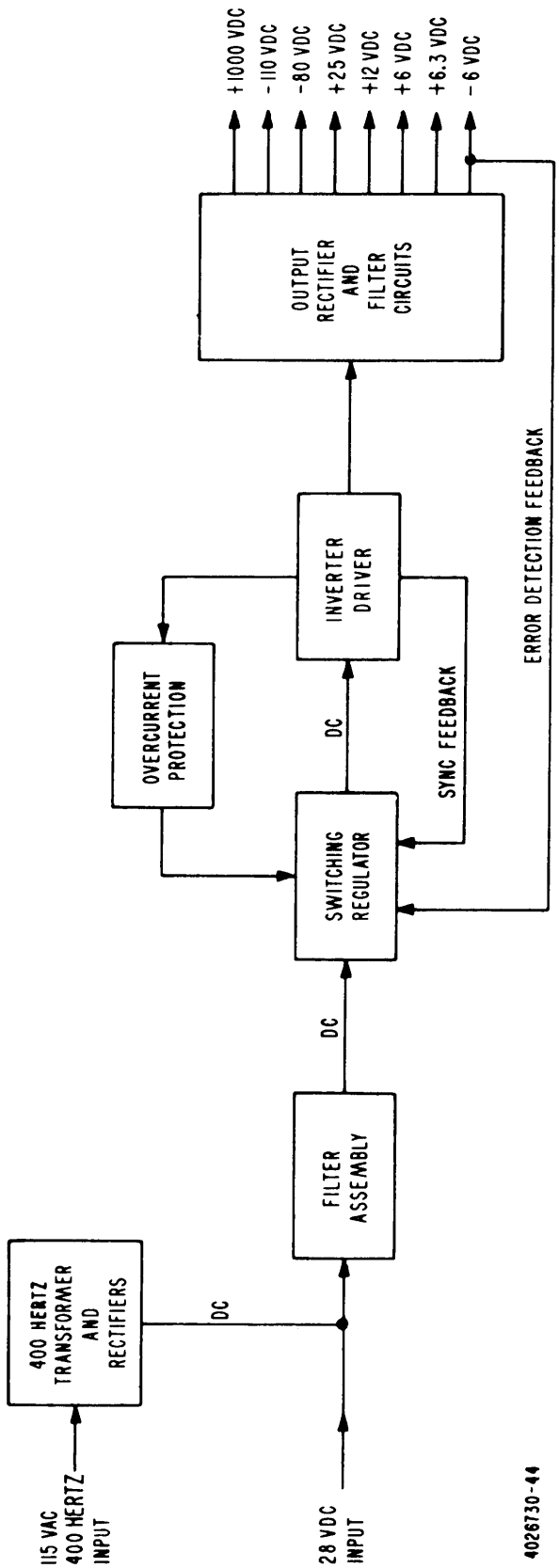


Figure 2-24. Power Supply (PS1), Block Diagram

c. Switching Regulation. The switching regulator assembly consists of transistors Q3 through Q8 and their associated components functioning in conjunction with switching transistors Q1 and Q2 on the filter assembly and output transistor Q9, diode CR11, and variable resistor R63 on the over-current assembly. The purpose of the switching regulator is to provide a constant dc voltage of approximately 17 volts to the dc inverter. To perform this function, the switching regulator monitors the -6 vdc output of the power supply and uses the deviations in this output to regulate the switching function. Transistors Q1 and Q2 comprise the switch which is closed when they conduct and open when they are off. In the closed position, capacitors C14 and C15 will charge to the voltage input from the filter assembly minus the voltage drop across inductor L2 increasing the dc voltage input to the inverter driver. In the open position, they will discharge through the inverter driver reducing the dc voltage input. The -6 vdc output is monitored at the junction of diodes CR31 and CR32 through resistor R28 and diode CR11 at the base of transistor Q9. The collector voltage of Q9 is determined by the -6 volt output and series resistors R62 and R63 which connect to the 6.2 volts reference diodes VR8 and CR9. Q9 operates in the active mode. The value of R63 is adjusted to set all the output voltages to their proper value. When the –6 vdc output becomes less negative, the collector current of Q9 will increase, causing a more negative input, relative to the voltage drop across diode VR8, to be applied through resistors R23 and R24 to the base of transistor Q8. C16 reduces the regulator band-width for stability purposes. Transistor Q8 will then turn off. This turns Q7 off since current no longer flows through R18 and R19. Likewise, Q6 is turned off because of the lack of current through R15 and R161 When Q6 turns off, Q5 turns on and saturates; Q5’s base current flows through R13. When Q5 saturates, R8 and R9 are driven negative through Q5 and R10 causing Q3 and Q4 to saturate. The collector outputs of transistors Q3 and Q4 drive the bases of transistors Q1 and Q2. When transistors Q3 and Q4 conduct, transistors Q1 and Q2 saturate. This closes the switch and charges C14 and C15 through L2. This increasing dc voltage output is applied to the inverter driver causing the -6 vdc output to become more negative. When the -6 vdc output becomes sufficiently negative, the reaction of the above circuits will reverse and the switch will open, reducing the dc voltage input to the inverter driver and returning the -6 vdc output to a less negative value.

d. Inverter Driving. The inverter driver consists of transistors Q14, Q15, Q16, transformers T2, T3, and other associated components. The output voltage of the switching regulator is applied to the emitter of transistor Q14 and the center tap (pin 2) of the primary of transformer T3. Initially, Q14 is forward-biased because of the current flow through CR15, CR16, R37, and R38. Q14 saturates, causing current to flow through R41 and into the bases of transistors Q15 and Q16. Circuit imbalance or thermal noise will then cause one transistor, Q15 or Q16, to conduct more heavily and turn the other off through transformer T2.

Assuming transistor Q15 conducts first, current will be drawn from pin 2 to pin 1 of transformer T3 placing pin 1 approximately 0.8 volt above ground. Because of self-inductance in the primary, the voltage at pin 3 will be about double the input voltage. This voltage causes current to flow through CR15, R37, and R38, turning off Q14. At this time, approximately twice the dc input voltage will be impressed across the primary of T2. The current flowing through the primary of T2 consists of two parts; a load current, that is, the transformed base drive being supplied to Q15 through R39, and a magnetization current. When transformer T2 reaches saturation, transformer action ceases and transistor Q15 turns off. Transistor Q16 then conducts due to regenerative action and the cycle will be repeated. Under normal operating conditions the inverter oscillates at a frequency of approximately 10 kHz. R42 acts to limit the peak magnetization current that can flow as the primary of T2 saturates. Feedback of the negative voltage spike developed at the output of diodes CR15 and CR16, through capacitor C40 to the switching regulator, enables the inverter driver and the switching regulator to remain in synchronization, preventing development of a beat frequency in the power supply.

e. Output Rectifier and Filtering Circuits. The required eight output voltages are obtained from four basic windings f transformer T3 with taps. The .000 vdc output is obtained from a voltage doubler circuit. It provides approximately 1000 vdc between terminals Al and 9 of P2. The output of test point 10 is approximately 1000/100 due to voltage divider consisting of resistors R45, R46, R66, and R47. The +25 vdc, -110 vdc, +12 vdc, +6 vdc, -6 vdc, and +6.3 vdc outputs are provided through full wave rectification with either LC or RC filtering. Diode CR36 connected between the +25 vdc and +12 vdc outputs provides the +25 vdc transformer winding with overcurrent protection insuring reaction of the overcurrent protection circuitry. The +6.3 volts and the 1 kV return leads are floating.

f. Overcurrent Protection. The overcurrent protection consists of transistors Q1O, Q11, Q12, and Q13. This circuit monitors the current drawn through resistor R36 in the inverter driver, and when it exceeds a threshold determined by variable resistor R64, operates to open the switching regulator for periods of three seconds so long as the excessive current exists. Transistors Q12 and Q13 share base drive through resistor R33. Normally transistor Q12 is in saturation and transistor Q13 is active. When the voltage across resistor R36 rises sufficiently, transistor Q13 will saturate. Any further increase in current in resistor R36 will cause almost all the current available for base drive to flow to the base of transistor Q13, thus starving transistor Q12 for drive. As transistor Q12 turns off, transistors Q1O and Q6 (switching regulator) are turned on. Transistor Q6 turns transistor Q5 off, opening the switch transistors Q1 and Q2 and isolating the short from the input circuit. When transistor Q1O was turned on, the cathode of diode CR13 was pulled to ground causing a negative voltage input through capacitor C18 to the bases of transistors Q12 and Q13. Transistors Q12 and Q13 remain off until capacitor C18

discharges through resistor R33, which is nominally a period of approximately three seconds. When transistor Q12 again conducts, it causes transistor Q10 to turn off, removing the ground potential from the cathode of diode CR13 and causing transistor Q11 to conduct. Transistor Q11 will conduct only for the short period necessary to charge capacitor C18. This cycle will continue as long as the excess current condition exists. Thus, transistors Q10, Q11, and Q12 function as a fast recovery multi-vibrator.

2-28. FILTERS. Since the transmitter is in the rf section, filter assemblies are provided to eliminate rf interference (RFI) between the transmitter and digital components. Elimination of RFI in the control lines is accomplished by filters FL1, filters on encoder control, and the use of shielded lines which function as distributed capacitances. Filter FL1 (see figure 6-18) provides for filtering all mode control lines with the exception of mode C. The mode C control lines are filtered by RC filters consisting of capacitors C2 through C12 and resistors R56 through R66 on the encoder control (A5) (see figure 6-13). RF1, caused, by ac transients and spurious energies, are eliminated by: ac filters FL2 and FL3, and dc filters FL4 and FL5 (see figure 4-21); filters FL6 through FL15 (see figure 4-17); filter FL16 (see figure 6-19); diodes CR2 and CR3 across relays K1 and K2; and capacitors C1 and C2. The above components are all showh schematically in figure 6-21.

2-29. CONDENSED DATA.

2-30. The section lists in tabular form the electrical, design, environmental, and physical characteristics of the Receiver-Transmitter, Radio RT-859/APX-72, RT-859A/APX-72 and Mountings MT-3809/APX-72 and MT-3948/APX-72, and a glossary of terms.

Table 2-4. Electrical and Design Characteristics

Input Power Requirements:	
DC	27.5 vdc, 2.36 A maximum, operating limits 21 to 29 vdc.
(or)	
AC	115 vac, 95 VA maximum, 380 to 420 Hz, operating limits 107 to 122 vac (dc control voltages required).
Receiver:	
Frequency	1030 ±0.5 MHz
Frequency stability	±1.5 MHZ maximum for a period of at least 500 hours.
Bandwith	Minimum 7 MHz at -6 dB point. Maximum ±25 MHz at -60 dB point.

Table 2-4. Electrical and Design Characteristics (Cont)

Receiver: (Cont)	
Sensitivity	
Normal triggering level	Adjustable from -80 to -90 dBV.
Low triggering level	Adjustable from -65 to -80 dBV.
Signal input	Pulse rf.
Triggering bandwith	±2.5 MHz.
Transmitter:	
Frequency	1090 ±0.5 MHz.
Frequency stability	±3.0 MHz maximum.
Signal output	Pulse rf.
Peak power output	500 W ±2 dB.
Duty cycle	1.1% maximum.
Spurious responses	60 dB down from amplitude of transmitted pulse.
External Suppression:	
Input:	
Amplitude	10 to 70 vdc.
Duration	1.5 to 250 µs.
Polarity	Positive.
Resistance	2200 Ω.
Rise time	At least 10 V/µs.
Decay time	Peak amplitude to 10 vdc within 10 µs.
Output:	
Amplitude	18 to 30 V.
Duration	18 V minimum until last transxmitted pulse has decayed to 10% level. Less than 5 V, 5 µs after last pulse has fallen to 10% level.
Polarity	Positive.
System impedance	300 to 2200 Ω shunted by not more than 1800 pF capacitance.
Rise time	20 vdc minimum per µs.
Decay time	20 vdc minimum per µs.
Spurious output	Less ±1 vdc.

Table 2-4. Electrical and Design Characteristics (Cont)

Interrogation Pulses:	
Modes 1, 2, 3/A, test, and C	Two pulses 0.8 to.1 µs wide spaced 3, 5, 8, 6.5, and 21 µs, respectively.
Mode 4	Four pulses 0.5 ±0.1 µs wide spaced 2 µs between pulses.
Reply Pulses:	
Mode 1	Maximum of 6 information pulses.
Modes 2, 3/A, and Test	Maximum of 13 information pulses.
Mode C	Maximum of 11 information pulses.
Mode 4	Determined by external computer.
Width	0.45 ±0.1 µs.
Spacing	1.45 ±0.05 µs.
Special Replies:	
Identification' of Position (I/P)	
Mode 1	Two reply code trains.
Modes 2 and 3/A	One reply and a single framing pulse (F3).
Emergency:	
Modes 1 and 2	One normal reply code train followed by three sets of framing pulses. (F3 through F8).
Mode 3/A	One reply train coded 7700 followed by three sets of framing pulses (F3 through F8).
Special Position Indicator (SPI) (RT-859/APX-72 only)	In mode C replies, the use of the D4 pulse developes F3 or SPI pulse.
"X" Pulse	Fourth information pulse in mode 1, seventh in modes 2 and 3/A indicating drone or pilotless aircraft.
Automatic overload Control:	
Reply rate limiting:	
Modes 1, 2, 3/A, Test, and C	500 to 3000 interrogations per second, adjustable.
Mode 4	1500 to 2500 interrogations per second, adjustable.

Table 2-4. Electrical and Design Characteristics (Cont)

SLS rate limiting	>5000 to >10,000 SLS pulses per second.
Delay	3 ±0.5 µs between last interrogation pulse and first reply pulse at the antenna.
Interference:	
CW and AMCW	Interference 10 dB below interrogation signal at levels between 0 and 50 dB above normal triggering level will not reduce replies more than 50%.
Pulse	Operates in the presence of random and regularly spaced pulses as follows:
Interrogation signal 3 to 10 dB above normal triggering.	Interference 10 dB below interrogation will not reduce replies more than 50%.
Interrogation signal 20 to 50 dB above normal triggering.	Interference 3 dB below interrogation will not reduce replies more than 50%.
Interrogation 10 dB above interference level.	Replies to 90% of interrogations when random pulse interference not recognized as normal or side lobe interrogation.
pulse Width Discrimination:	
Modes 1,2,3/A, and C interrogations 0 to 6 dB above MTL.	Pulse width less than 0.3 µs will not cause more than 10% replies.
Modes 1,2,3/A,4, and C interrogations 0 to 50 dB above MTL.	Pulse width greater than 1.6 µs for RT-859/APX-72 or 1.5 µs for RT-859A/APX-72 will not cause replies
Mode 4 interrogations 0 to 6 dB above MTL.	Pulse width less than 0.2 µs will not cause more than 10% replies.
Side Lobe Suppression (SLS):	
Will reply	When first pulse 9 dB or more positive than SLS control pulse.
Will not reply	When first pulse is equal to or less than SLS control pulse.

Table 2-5. Environmental Characteristics

Standard Conditions:	
Temperature	25 ± 5°C (room ambient)
Humidity	Room ambient up to 90% relative
Altitude	Sea level
Warm-up time	1 minute maximum
Services Conditions:	
Temperature	-54°C to +95°C (-65°F to +203°F)
Altitude	To 30,000 ft unpressurized to 70,000 ft pressurized 5 psig
Warm-up time	2 minutes maximum under extreme service conditions.

Table 2-6. physical Characteristics

ITEM	HEIGHT (in.)	DEPTH (in.)	WIDTH (in.)	UNIT WEIGHT (lb)
Receiver-Transmitter, Radio RT-859/APX-72, RT-859A/ APX-72	6.06	12.25	5.76	15.00
Mounting MT-3809/APX-72	0.81	12.40	5.06	1.50
Mounting MT-3948/APX-72	2.50	12.40	5.06	2.10

Table 2-7. Glossary of Terms

TERM	DEFINITION
A	Assembly
AJ	Anti-jamming
AMCW	Amplitude modulated continuous wave
A_1, A_2, A_4	Information pulses
B_1, B_2, B_4	Information pulses
C	Clear or reset
C_1, C_2, C_4	Information pulses
DL	Delay line
EMER	Emergency
FF	Flip-flop (multivibrator)

Table 2-7. Glossary of Terms (Cont)

TERM	DEFINITION
FO	Center frequency
F_1 through F_8	Framing pulses
I/P	Identification of position
ISLS	Interrogation sidelobe suppression
MTL	Minimum triggering level
M-1, M-2, M-3/A, M-C	Modes 1, 2, 3/A, and C
MOS	Metal oxide silicon composition
NARF	Naval Air Rework Facility
NC	No contact
NM	Not measured
NORM	Normal
S	Set
SLS	Sidelobe suppression
SPI	Special pulse indicator
SS	Single-shot
STBY	Standby
0	Logic level nominal OV or ground
1	Logic level nominal positive

SECTION III

SPECIAL SUPPORT EQUIPMENT (AGE) MAINTENANCE

3-1. GENERAL.

3-2. Special support equipment designated for use with the RT-859/APX-72 and RT-859A/APX-72 comprises six extender boards, listed in table 4-20; three test cables (part numbers 4023655, 4023656, and 4023657); one extraction/insertion tool (part number 2004307); Tester-Dummy Load TS-3243/APM. The extender boards (figure 4-14), test cables (figure 4-4), and extraction/insertion tool (figure 4-16) are furnished as accessories with Test Sets, Transponder AN/APM-239 and AN/APM-239A. Refer to manuals provided with these test sets for maintenance instructions for those parts. Tester-Dummy Load TS-3243/APM is supplied with a manual (NAVAIR 16-35TS3243-1, NAVY/T.O. 33AA7-79-1, AIR FORCE) which provides the necessary maintenance instructions. Should this tester not be available, a load bank may be constructed and used as a substitute. Instructions for the construction of such a load bank at the intermediate level of maintenance and above, are provided in the following paragraphs.

3-3. LOAD BANK ASSEMBLY.

3-4. Table 3-1 lists the components needed for assembling the load bank. A typical assembly procedure, using schematic diagram figure 3-1, follows:

a. procure components listed in table 3-1 together with a suitable chassis and mounting hardware.

b. Install connector XPS1 P2 in one end of chassis, positioned as shown in figure 3-1.

c. Install a common ground at the opposite end of the chassis, using a lug with multiple tie points connected to a grounded feed-through terminal (not listed in table 3-1).

d. Install test jacks TP1 and TP2 on chassis in positions conforming to general location indicated in figure 3-1.

e. Install switch, S1 on chassis (see figure 3-1 to determine best location).

f. Connect resistors R1 and R2 in series between terminal A1 (XPS1 P2) and TP1.

g. placard chassis adjacent to connector P2 as follows:

WARNING

1000 VDC ON PIN A1 OF CONNECTOR P2, ASSOCIATED RESISTORS AND LOAD BANK WIRING.

h. Connect resistor R3 between TP1 and common ground.

i. Connect TP2 to common ground.

j. Connect resistors R4, R5, and R6 in series between terminal 8 and common ground.

k. Connect resistor R7 between terminal 8 and switch S1.

l. Connect switch S1 to common ground.

m. Connect a length of wire between terminal 9 and common ground.

n. Connect resistors R8 and R9 in series between terminal 4 and common ground.

0. Connect resistors R10, R11,

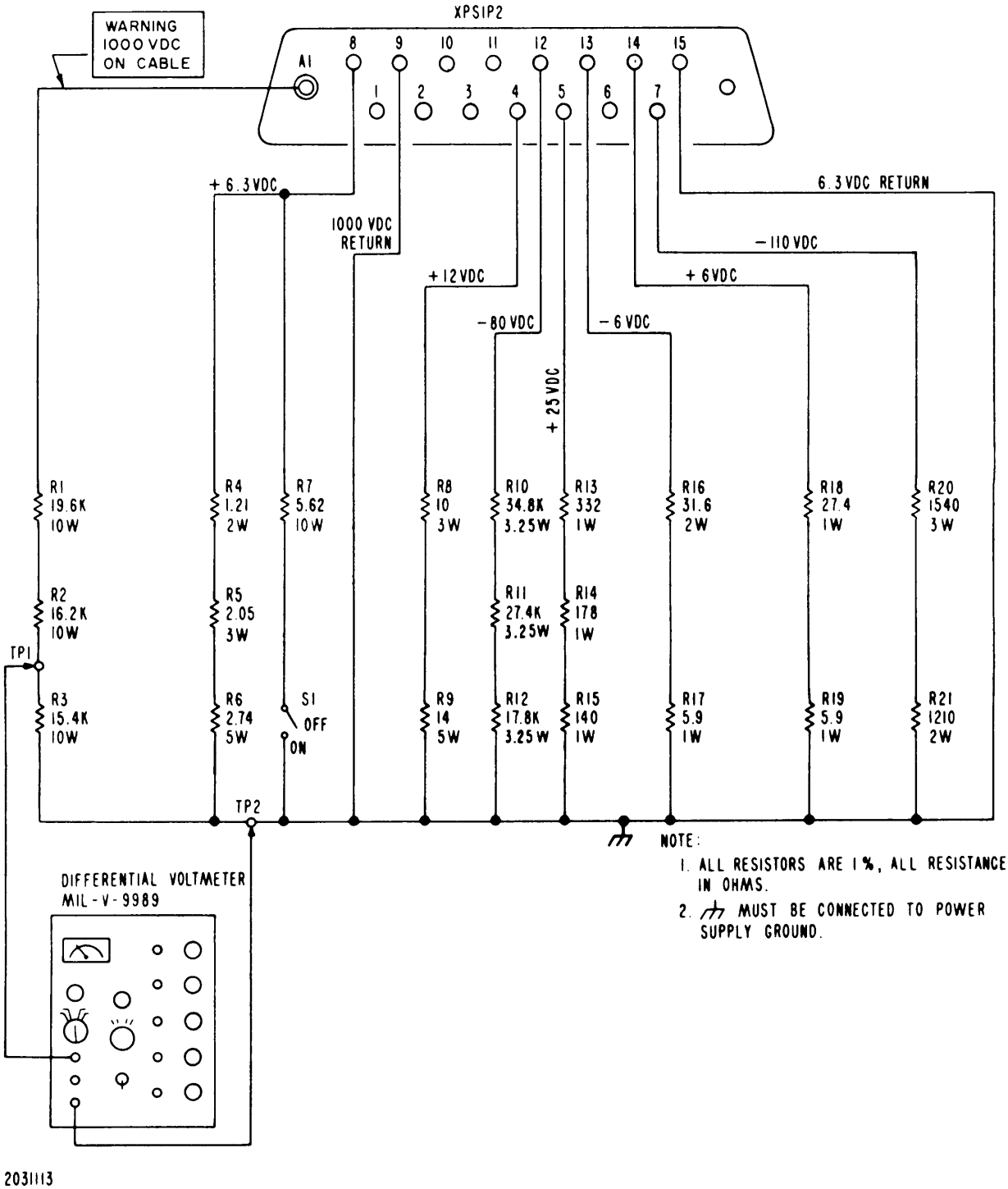


Figure 3-1. Schematic Diagram, Load Bank Assembly

and R12 in series between termi - nal 12 and common ground.

p. Connect resistors R13, R14, and R15 in series between termi- nal 5 and common ground.

g. Connect resistors R16 and R17 in series between terminal 13 and common ground.

r. Connect resistors R18 and R19 in series between terminal 14 and common ground.

s. Connect resistors R20 and R21 in series between terminal 7 and common ground.

t. Connect a length of wire between terminal 15 and common ground.

u. After assembly, make continuity and resistance measurements with switch S1 ON and OFF, to ensure that assembly is correctly wired.

3-5. LOAD BANK ASSEMBLY MAINTENANCE PROCEDURES.

3-6. PREVENTIVE MAINTENANCE. Perform the following two steps:

a. Clean by removing dust and other foreign matter with a dry cloth or dust brush.

b. Inspect visually for breaks, evidence of charring, and loose or missing hardware.

3-7. TROUBLESHOOTING. Use continuity and resistance measurements to detect cause of failure.

Table 3-1. List of Parts, Load Bank Assembly

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION	QUANTITY
A1	DM-51157	CONTACT, Electrical, high voltage, straight, ITT Cannon	1
R1	RWR78S1962FM	RESISTOR, MIL-R-39007	1
R2	RWR78S1622FM	RESISTOR, MIL-R-39007	1
R3	RWR78S1542FM	RESISTOR, MIL-R-39007	1
R4	RWR71S1R21FM	RESISTOR, MIL-R-39007	1
R5	RWR89S2R05FM	RESISTOR, MIL-R-39007	1
R6	RWR74S2R74FM	RESISTOR, MIL-R-39007	1
R7	RWR78S5R62FM	RESISTOR, MIL-R-39007	1
R8	RWR89S10R0FM	RESISTOR, MIL-R-39007	1
R9	RWR74S14R0FM	RESISTOR, MIL-R-39007	1
R10	RS2A34R8K1PCT	RESISTOR, 34.8K, 3.25W Dale Electronics	1
R11	RS2A00B1780F	RESISTOR, 27.4K, 3.25W Dale Electronics	1
R12	RS2A17R8K1 PCT	RESISTOR, 17.8K, 3.25W Dale Electronics	1
R13	RwR81S3320FM	RESISTOR, MIL-R-39007	1
R14	RWR81S1780FM	RESISTOR, MIL-R-39007	1

Table 3-1. List of Parts, Load Bank Assembly (Cont)

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION	QUAN-TITY
R15	RWR81S1400FM	RESISTOR, MIL-R-39007	1
R16	RWR71S31R6FM	RESISTOR, MIL-R-39007	1
R17	RWR81S5R90FM	RESISTOR, MIL-R-39007	1
R18	RWR81S27R4FM	RESISTOR, MIL-R-39007	1
R19	RWR81S5R90FM	RESISTOR, MIL-R-39007	1
R20	RWR89S1541FM	RESISTOR, MIL-R-39007	1
R21	RWR71S1211FM	RESISTOR, MIL-R-39007	1
S1	MS18151-1	SWITCH, Toggle, single pole	1
TP1	MS39024/1-02	JACK, Electrical, test point, red	1
TP2	MS39024/1-03	JACK, Electrical, test point, black	1
XPS1P2	DBM-17W2P	CONNECTOR, Electrical, recep-table ITT Cannon	1

Wire Type Specifications MIL-W-16878, Insulation Teflon MIL-M-14077

AWG SIZE	CONDUCTOR DIA NOMINAL	NO. OF STRANDS MINIMUM	MAX DC RESISTANCE OHMS/1000 FT AT 25°C	DIA OVER INSULATION MAXIMUM
22	0.030	19	16.7	0.054

SECTION IV

INTERMEDIATE AND DIRECT/GENERAL SUPPORT MAINTENANCE PROCEDURES

4-1. GENERAL.

4-2. This section contains instructions and information for performing the basic functions of maintenance support for the Receiver-Transmitter, Radio RT-859/APX-72 and RT-859A/APX-72.

a. System Test and Checkout. The testing of the receiver-transmitter as an integral part of the transponder system.

b. Performance Test and Measurements. Testing to determine the serviceability or unserviceability of the receiver-transmitter and its adequacy relative to minimum performance standards.

c. Troubleshooting. Testing to determine the location and cause of equipment malfunctions.

d. Repair. Restoration of the equipment to serviceable condition by replacing or reworking defective parts or assemblies.

e. Alignment, Adjustment, and Calibration. The alignment, adjustment, and calibration of the receiver-transmitter to obtain proper performance before and after repair.

4-3. Reported failed units received at intermediate maintenance levels will be subjected to checkout procedures to determine if the unit is properly aligned and adjusted. The tests will include the use of go/no-go performance tests to confirm the findings made with the unit installed in the aircraft or surface vessel. This test will be performed with auxiliary equipment (refer to paragraph 2-5) and without opening the receiver-transmitter case. If misalignment is indicated, the case will be opened and alignment completed, by maintenance personnel, before continuing the performance tests. After performance tests are completed and the general area of failure determined, troubleshooting procedures will be started to locate the defective stage. The troubleshooting procedures (refer to paragraph 4-13) will follow a logical sequence of isolating the fault to a particular circuit board or subassembly utilizing conveniently located test points.

4-4. For the purpose of maintenance, the following subassemblies are designated as intermediate-level maintenance assemblies.

a. R. F. Assembly

1. Detector and Video Amplifier circuit board assembly

2. Sensitivity circuit board assembly

3. Modulator circuit board assembly

b. Digital Circuit Board and Power Supply Assembly

1. Processor circuit board assembly

2. Delay line circuit board assembly

3. Decoder circuit board assembly

4. Mode 4 circuit board assembly

5. Encoder clock circuit board assembly

6. Encoder control circuit board assembly

7. Encoder gating circuit board assembly

8. Power supply

4-5. Table 4-1 is a list of test equipment approved for use with the receiver-transmitter at intermediate and depot maintenance levels. Test equipment characteristics are listed to enable selection of an equivalent substitute when listed equipment is not available. Refer to Organization Maintenance Manual for the Receiver-Transmitter RT-859/APX-72, NAVSHIPS 0967-217-4010, TM 11-5895-490-20, and applicable aircraft organizational maintenance manuals for a complete list of approved tool and test equipment requirements.

4-6. CHECKOUT.

4-7. Checkout procedures consist of system bench tests, using go/no-go performance tests to confirm the findings made with the receiver-transmitter installed in the aircraft or surface vessel; and performance bench tests and measurements to determine if the equipment meets operational performance standards.

4-8. SYSTEM BENCH TESTS. (U. S. Army only) System bench tests, to confirm the findings made with the receiver-transmitter installed in the aircraft or surface vessel, are made with the AN/APM-123 transponder test set and auxiliary test equipment shown in figure 4-1. To perform these tests, proceed as follows:

WARNING

Dangerous voltages exist in this equipment. Take precautions when performing maintenance checks while power is on.

a. preliminary procedures. Assemble and connect the receiver-transmitter and test equipment as shown in figure 4-1 and described below. The cables are supplied with the test equipment. Test equipment should be allowed to warm up for a minimum of ten minutes before starting test procedures. Preliminary control settings are as described in the following paragraphs:

1. Test Set AN/APM-239 with C-6280(P)/APX inserted.

(a) Connect PWR INPUT (P2) to the 115-vac, 400 Hz voltage source.

(b) Connect TRANSPONDER power and control jack to POWER, CONTROL, and VIDEO jack (J1) on the receiver-transmitter.

(c) Set all controls and switches as directed in table 4-2.

2. Test Set, Transponder, AN/APM-123.

(a) Set 28 VDC-115VAC-OFF power switch to OFF.

(b) Set MODE switch to any mode except mode 4.

(c) Set ISLS ON-OFF switch to OFF.

(d) Set FUNCTION switch to SELF TEST.

(e) Set AB-CD CODE controls to 0000.

(f) Connect POWER connector to the 115 vac, 60 Hz power source. Refer to instruction manual supplied with test set for proper selection of cable.

(g) Connect one end of the CG-409G/U rf cable to the PROBE jack of the AN/APM-123.

Table 4-1. Test Equipment Requirements

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Attenuator	Weinschel Model 10-10	X			5960-581-8192	Power rating: 10 Watts average Frequency: DC - 1 GHz Attenuation: 10 dB
Electronic Counter	Hewlett-Packard Model 5245L Without Plug-in	X			6625-973-4837	Frequency range: 0 to 50 MHz Period average measurements range: Single period 0 to 1 MHz Multiple period 0 to 300 MHz
	AN/USM-207		X		6625-911-6368	Time base: 0.1 to 10 MHz in 0.1 MHz steps Accuracy: ±1 count ± base accuracy ± trigger error when applicable Sensitivity: 100 mV rms
Generator, Signal	AN/URM-64A	X	X		6625-570-5721	Range : 900 to 2100 MHz Accuracy: ±1% output: 0.2 µV -0.16 V Modulation: Internal 40 4000 pps
Generator, Sweep Signal	SG-677/U	X		X	6625-NC-10531K	Frequency: VHF range 500 kHz to 400 MHz UHF range 350 MHz to 1200 MHz
	AN/USM-203		X		6625-086-7165	Sweep width: Variable 100 kHz to 400 MHz Markers, internal: 1 MHz, 10 MHz 100 MHz RF output: Minimum 0.25 V rms on VHF range Minimum 0.50 V rms on UHF range Output impedance: 50 Ω, nominal RF output attenuator: Minimum of 50 dB in 10 dB steps

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Generator, Sweep Signal (Cont)	AN/USM-203 (Cont)		X		6625-086-7165 (Cont)	Spurious or harmonics: At least 20 dB down
Multimeter	AN/PSM-4D	X			6625-073-2227	DC voltage: 0.05 - 1000 vdc, 20,000 Ohms /V
	TS-352B/U		X		6625-242-5023	AC voltage: 0.1 - 500 vac, 1000 Ohms/V
	AN/PSM-6			X	6625-724-8582	Current: 20 ma - 10 Amp dc Resistance: 1 - 100 MΩ Accuracy: 4% all ranges
Multimeter, Meter	ME-26/U		X		6625-646-9409	DC voltage: 0 - 1000 vdc 122 MΩ
	ME-26A/U	X			6625-554-8691	AC voltage: 0 - 300 vdc 122 MΩ
	HP410B			X	6625-360-2993	Resistance: 0.2 - 500 MΩ Accuracy: ±3%
Oscilloscope, Plug-In	AN/USM-140B H02-162F	X	X		6625-987-6003	Frequency range: DC - 120,000 Hz Sweep duration: 0.05 - 60 V peak-to-peak Sensitivity: 0.02 - 7 V/cm vertical 0.1 - 30 V/cm horizontal Frequency response: 0 - 1 MHz X-axis 0 - 22 MHz, Y-axis Input impedance: 1 MΩ, 40 pF shunt
	MIL-0-9960			X	6625-892-5251	
Pump Dehydrator, Manual	MK-20A/UP	X	X	X	4320-342-6446	Pressure gage: 0 - 30 lb/in^2 Output :26 cubic inches per piston stroke Dehydration:170 cu ft of air from 60% to 10% relative humidity

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Radar	AN/UPM-98A	X	X	X	6625-912-0429	SIF coder: Code range 2 - 14 pulse Pulse train repetition rate 15 - 4100 pps Pulse amplitude 0 to 5 V Modes 1,2,3/A, emergency I/P and X Marker and sync trigger: Delay zero and variable 0 - 750 ps Trigger polarity positive PRF variable 15 - 4100 pps Amplitude 5 - 50 V (nominal 20 ±5 V) Markers 1 μs and 1.45 ps Visual display: CRT zero delay and variable 5 to 750 PS Vertical sensitivity 0.05 - 20.0 V per inch Sweep variable: 1.0 - 20,000 μs Frequency response essentially flat 50 Hz to 6 MHz Pulsed frequency range 925 - 1225 MHz Wavemeter frequency range 925 - 1225 MHz accuracy ±0.7 MHz

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Radar (Cont)						Power measurement: RF attenuation 0.5 - 3500 watts peak at maximum pulse train repetition rate with accuracy of ±1 dB Pulse counter: Pulse rate 0 - 500 pps with an accuracy ±10% full scale Demodulator: Frequency detection range 925 - 1225 MHZ with peak inputs to 3500 W
Test Set, Radar	AN/UPM-137 NOTE Only the following test equipment is required when performing maintenance using the AN/UPM-137 test set: a. AN/APM-245 b. AN/APM-239 (with C-6280 (P) APX-72 plug-in) c. Electronic Counter HP Model 5745L	X		X	6625-264-2249	Selective Identification Signal (SIS) Generator SG-865/UPM-137 Triggers (zero and delayed): Polarity: Positive; Duration: 1 - 2 µs; Amplitude: 20 ±5 V (75 Ohms, 1100-pF load) SIF 1 coder: Normal Code Selection: 0000 - 7777 (2. to 14 pulses); Emergency format (fixed): Train followed by three sets of bracket pulses (F1-F2); Bracket set spacing: 4.35 to.1 µs

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Radar (Cont)	NOTE (Cont) d. Attenuator Weinschel Model 10-10 e. Voltmeter MIL-V-9989					Selective Identification Signal (SIS) Generator SG-865/UPM-137 SIF 1 coder (Cont): "X" pulse: Spaced 10.15 ±0.05 µs from first pulse (F1) SPI pulse: Spaced 24.65 ±0.1 µs from first pulse (F1) SIF 2 coder: Same as SIF coder 1 Mode 4 word A generator: 28 pulses in train Mode 4 word B generator: 28 pulses in train Suppressor pulse generator: Amplitude (separate output): <15 V into 75-Ω/1100-pF load Challenge/tag video: Five modes (plus provision for ISLS) Mode repeat: Sequentially 1,2,3, 4,8, or 16 times (any combination of modes) P1-P3 amplitude: (separate output) 0 to >15 V (variable) into 75 Ω ±5% load Mixed video output: SIF 1 train, SIF 1 and SIF 2 trains; Tag-SIF l-Reset; Tag-SIF 1 and 2-Reset

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Radar (Cont)						Interrogator Signal Simulator SM-559/UPM-137 RF output (fixed): Frequency: 1090 MHz ±0.01% RF output (sweep): Frequency: 1070 - 1110 MHz at a rate of 250 Hz ±5% Markers: 1090 MHz, and ±3, ±5, ±10, and ±20 MHz from center frequency (9 total); accuracy is within ±0.1 MHz Sweep sync output: Amplitude: 8 ±2 V, negative Width: 360 to 440 µs 60 MHz sweep generator: Input rf: 1030 MHz Frequency range: 40 to 80 MHz at 250 Hz Pulse counter: Ranges: 0 to 1000 pps 0 to 10,000 pps ±5% at full scale ±10% at 1/10th full scale Simulated radar system video: Azimuth change pulse and north reference output

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARNY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Radar (Cont)						SIF target gate: Coincident with Y-gate and inhibits an SIF reply train of the SIS generator until target time of active readouts RF Signal Generator SG-866/UPM-137 RF output: (fixed) Frequency: 1030 MHz ±0.01% Main power control: Variable 0 – -100 dBm; ±l.5 dB at any setting, 1010 - 1110 MHZ ±1 dB at 1030 MHz Auxiliary power control: +3 to -60 dB with respect to main power RF output: (sweep) Frequency: 1010 - 1050 MHz at a 250-Hz rate ±5% Sweep rf markers: 1030 MHz and ±3, ±5, ±10, and ±20 MHz from center frequency (9 total); accuracy is within ±0.1 MHz Sweep sync: Polarity: Negative Amplitude: 8 ±2 V Pulse width: 400 ±40 µs RF inputs: Frequency: L-band

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Radar (Cont)						RF Signal Generator SG-866/UPM-137 (Cont) Modulation inputs: Main: Pulse input to main rf line Auxiliary: Pulse input to auxiliary rf line associated with main rf line Demodulator: 0.5 W rf input will produce a minimum video output indicated in calibration charts for power vs. video out, at least 0.5 V amplitude. Accuracy: ±1 dB with calibration chart Oscilloscope OS-208/UPM-137 Vertical amplifiers: (dual channel) Frequency response: DC to 8 MHz flat within ±1.5 dB (3 dB down at 12 MHz) Sensitivity: 0.05 V/div to 20 V/div ±5% in nine calibrated steps Sweep rates: 0.1 µs/div to 2 ms\div ±5% in 14 calibrated steps

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Radar (Cont)						Oscilloscope OS-208/UPM-137 (Cont) Sweep delays: <1 to 4400 µs in four continuously variable ranges Trigger: (modes) Internal: DC (+) or (-) crystal marker External: AC or DC (+) or (-) Trigger: (external level) AC: 0.1 V min DC: 2 V min Markers (µs): 0.1, 1.0, 1.45, 5.0, 50, or 0.1 and 1.0 ±0.02%
Test Set, Simulator	AN/APM-245 used to modulate AN/UPM-98A for mode 4	X	X	X	6625-087-1227	Inputs: External trigger outputs: Internal trigger: Selectable groups 2 - 10 triggers variable 10 - 10,000 pps Amplitude: 4 – 40 V Polarity: positive or negative Width: 0.5 - 1.0 µs Mode 4 enable trigger: Amplitude: 3.0 - 6.5 V Polarity: positive Width: 0.3 - 3.0 µs Rise time: 0.1 µs max. Test Word: 37 selectable bits “0” or "1" Amplitude: 5.0 - 35 V Polarity: positive

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Simulator (Cont)						Outputs: (Cont) Width: 0.5 ±0.1 µs Spacing: ±0.1 µs of even multiples of 1.0 µs Auxiliary pulse: Test word pulse adjustable from 0 - 10.0 µs Markers Mode 4 reply Mode 4 disparity Mode 4 video Pulse counter: pulse rate 0 - 1000 and 0 - 10,000 with an accuracy of ±5% Delayed pulse: Delay 1: 8 - 76 µs Delay 2: 194 - 270 µs Amplitude: 4.0 ±10() V Polarity: positive Width: 0.3 to 1.0 µs Reply train: 3 pulses spaced 1.8 ±0.2 µs Amplitude: 3.0 - 5.0 V Polarity: positive Pulse width: 0.3 - 0.7 µs Position adjustable: 200 - 276 µs
Test Set, Transistor	TS-1100A/U	X			6625-580-4166	Test ranges: Beta 1-4, 3-12, 10-40, and 30-300 ICO 0-5 PA, 0-500 PA Beta accuracy: In-circuit, maximum of ±20% plus out-of-circuit inaccuracy Internal battery source
	TS-1836/U		X		6625-617-5817	
	Model 1890M			X	6625-993-3389	

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Transponder	AN/APM-123 (V)		X		6625-948-0076	Transmitter: Frequency: 1030 MHz Power output: -9 dBm at antenna terminal Side lobe suppression: 3-pulse type PRF: 400 pps Pulse output group: 2 (p_1, p_3) without side lobe suppression 3 (P_1, P_2, P_3) with side lobe suppression Pulse spacing: Mode 1: 3 ±0.2 µs 2: 5 ±0.2 µs 3/A: 8 ±0.2 µs 4: internal modulation C: 21 ±0.2 µs Test: 6.5 ±0.2 us Receiver: Frequency: 109O MHz Bandwidth: 6.5 ±1.0 MHz (3 dB down points) Sensitivity: -9 dBm Gating: Duration of replies Decoding: Codes 0000-7777 emergency, and I/P Power Input: 115 vac single phase, 320 - 480 Hz at 6 Amp Output: 0 - 130 vat, 320 - 480 Hz 25 - 35 Vdc Mode C reply encoding: Codes 0000-7776 ON voltage +1.5 ±0.5 vdc OFF voltage +20.0 ±1.5 vdc
with Adapter (U.S. Army only)	UG-564/U		X		5935-258-9891	
Test Set, Transponder	AN/APM-239, AN/APM-239AX	X		x	6625-918-6286 6625-802-7425	

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Test Set, Transponder (Cont)						Mode 4 functions: Mode 4 reply Disparity Zeroize Landing gear interlock Test points: Suppression input, suppression output, auxiliary trigger input, mode 4 enabling trigger, interrogation, reply, disparity, audio, and return.
Test Set, Electronic Circuit Plug-in Unit (used at depot level only)	AN/APM-338	X	X	X	RX6625-423-6617AZ7X	Test Capabilities: Semi-automatic fault isolation on assemblies A1 through A8, DL1, AR3, and PS1. Crystal marker frequency: 1.000 MHz Sync pulse output: -3 V peak into 1000 Ω
Tester-Dummy Load	TS-3243/APM	X	X	X		Loads: 51.2 KΩ at 19.5 mA average 2.76 KΩ at 40 mA average 33.3 Ω at 180 mA average 37.5 Ω at 160 mA average 24 Ω at 500 mA average 625 Ω at 40 mA average 80 KΩ at 1 mA average 6 Ω at 1.1 mA average 2.7 Ω at 2.3 mA average
Voltmeter, Differential	MIL-V-9989	X		X	6625-724-4114	DC voltage: 0 - 500 vdc ±0.05% AC voltage: 0 - 500 vac ±0.2% 20 Hz to 10 kHz

Table 4-1. Test Equipment Requirements (Cont)

EQUIPMENT	TYPE	SERVICE USAGE NAVY	SERVICE USAGE ARMY	SERVICE USAGE USAF	FEDERAL STOCK NUMBER	CHARACTERISTICS
Voltmeter, Electronic	ME-202( )/U		X		6625-709-0288	Resistance: DC resistance infinite at NULL from 0 - 500 vdc

Equivalent equipment may be substituted for above requirements if specified equipment is not available.

Table 4-2. Preliminary Control Settings, Test Set AN/APM-239

CONTROL	POSITION
Mode C Encoder Simulator	
C1, A1, C2, A2, C4, A4, B1, B2, D2, B4, and D4	IN
TEST CONDITION	VOLTS
NORMAL-FAILURE (APM-239 Only)	NORMAL
Altitude Digitizer In/Out AN/APM-239A (only)	OUT
Mode 4	
Landing Gear INTLK-ON APM-239 (only)	Landing Gear INTLK
LDG GR Up/Down (APM-239A only)	Down
ZEROIZE-OFF	OFF
DISPARITY	DISPARITY
INTRR VIDEO (APM-239 only)	INTRR VIDEO
Reply/Interrupt (APM-239A only)	Reply
SPECIAL (APM-239 only)	CAUTION LIGHT RESET
Xpulse/OFF/Caution Light Reset (APM-239A only)	OFF
TRANSPONDER PWR INPUT	$\frac{\text{AC/DC}}{\text{DC}}$ or DC ONLY as required
C-6280(P)/APX	
MASTER	OFF
IDENT-OUT-MIC	OUT
M-1 TEST-ON-OUT	OUT
M-2 TEST-ON-OUT	OUT
M-3/A TEST-ON-OUT	OUT
M-C TEST-ON-OUT	OUT
RAD TEST-OUT-MON	OUT
MODE 4-ON-OUT	OUT

Table 4-2. Preliminary Control Settings, Test Set AN/APM-239 (Cont)

CONTROL	POSITION
AUDIO-OUT LIGHT	OUT
CODE	As required
MODE 1	73
MODE 3/A	7777
Power Control Unit	

CAUTION

Determine if the C-6280(P)/APX inserter in AN/APM-239 is wired for 6 or 28 volts before proceeding.

Table 4-2. Preliminary Control Settings, (Cont)
Test Set AN/APM-239

CONTROL	POSITION
PILOT	6-28 as applicable
6 AMP PWR	UP
METER SELECTION	DC-AC as applicable
DC OUTPUT CONTROL	Adjust for 28 volts
METER SELECTION	DC
AC OUTPUT CONTROL	Adjust for 115 volts

(h) Connect one end of the CN-1088/U fixed attenuator through a UG-564/U adapter to the ANT jack (J5) of receiver-transmitter. Connect the other end to the CG-409G/U rf cable.

3. Receiver-Transmitter, Radio RT-859/APX-72.

(a) Ensure the POWER, CONTROL, and VIDEO jack (J1) is connected to the TRANSPONDER power and control jack on the AN/APM-239.

(b) Ensure the antenna input jack (J5) is connected through the UG-564/U adapter and CN-1088/U fixed attenuator to the PROBE jack of the AN/APM-123.

(c) Set MODE 2 code switches to 00000

(d) Pressurize unit to 5 lb/ IN^2 gage.

b. AN/APM-123 Starting Procedures.

1. Set the 28 VDC-115 VAC-OFF power switch to either 28 VDC or 115 VAC, determined by which power source is being used. The POWER indicator should come on. Allow the AN/APM-123 to warm up for approximately two minutes.

2. Push and lock the PUSH TO TEST switch on the AN/APM-123. The ACCEPT indicator should come on. If the REJECT indicator comes on and remains on, the AN/APM-123 requires maintenance.

3. Set the ISLS ON-OFF switch to ON. The ACCEPT indicator should remain on.

4. Release the PUSH TO TEST switch.

5. Return ISLS switch to OFF.

c. Mode 1 Tests. The operating control positions (code, mode, etc.) of the AN/APM-123 must agree with the operating control positions of the receiver-transmitter and the C-6280(P)/APX. For mode 1 tests proceed as follows:

1. Set C-6280(P)/ApX controls as follows:

(a) MASTER switch to STBY (1 minute) then NORM.

(b) M-1 switch to ON.

(c) MODE 1 code switches to desired setting.

2. Set AN/APM-123 controls as follows:

(a) Mode switch to 1.

(b) CODE selector to agree with MODE 1 code setting on C-6280(P)/APX.

(c) FUNCTION switch to SYSTEM.

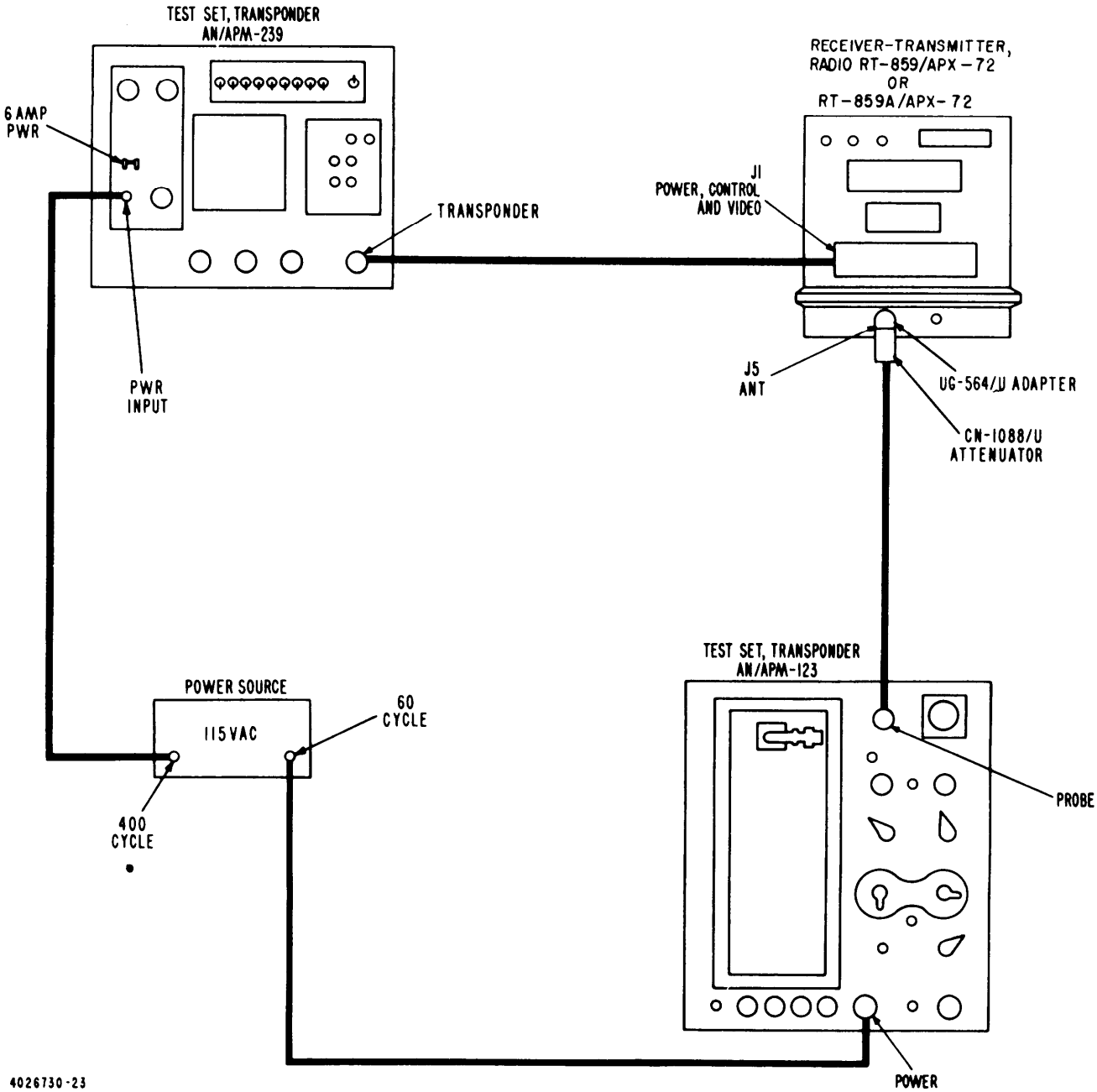


Figure 4-1. Bench Test Setup Using AN/APM-123 (U.S. Army Only)

3. Push and hold the AN/APM-123 PUSH TO TEST switch. The ACCEPT indicator should come on and remain on. If the REJECT indicator comes on, perform the procedure given in step 4., below.

4. press and turn the AN/APM-123 PUSH TO TEST switch to LOCK and set the FUNCTION switch to FREQ-POWER. If the ACCEPT indicator comes on, the power output is normal and the coder operation is abnormal.

5. Release the PUSH TO TEST switch.

d. Mode 2 Tests. For mode 2 tests proceed as follows:

1. Set C-6280 (P)/APX controls as follows, all other controls to remain as shown in table 4-2.

(a) M-1 switch to OUT.

(b) M-2 switch to ON.

2. Set MODE 2 code selector on receiver-transmitter to desired setting.

3. Set AN/APM-123 controls as follows:

(a) MODE switch to 2.

(b) CODE selector to agree with d.2.

4. Repeat steps c.3, c.4, and c.5.

e. Mode 3/A Tests. For mode 3/A tests proceed as follows:

1. Change C-6280(P)/APX controls as follows, all other controls remain as set in table 4-2.

(a) M-2 switch to OUT.

(b) M-3/A switch to ON.

(c) MODE 3/A code selector to desired setting.

2. Set AN/APM-123 controls as follows:

(a) MODE switch to 3/A.

(b) CODE selector to agree with step e.1. (c).

3. Repeat steps c.3, c.4, and c.5.

f. Emergency Tests (Military and Civil). Military emergency tests can be performed in modes 1, 2, and 3/A only. Set the C-6280(P)/APX MASTER and the AN/APM-123 FUNCTION switches to EMER. Use table 4-3 to set the mode and code switches of the AN/APM-123 and the transponder system. Select settings for each mode, in turn, and test all three modes as follows:

1. Push and hold the AN/APM-123 PUSH TO TEST switch. The ACCEPT indicator should come on.

2. Perform previous step in all modes.

3. Set the C-6280(P)/APX MASTER switch to NORM.

g. Identification of Position Test (I/P). To perform the I/P Tests, proceed as follows:

1 For mode 1 set mode and code switches in accordance with steps d.1, d.2, and d.3, and for mode 3/A in accordance with steps e.1 and e.2.

2. Set the AN/APM-123 FUNCTION switch to I/P and push and lock the PUSH TO TEST switch.

3. Push the C-6280(P)/APX IDENT-MIC switch to IDENT and release. The accept indicator light on the AN/APM-123 should come on for approximately 15-30 seconds.

4. Release the PUSH TO TEST switch.

h. Mode C (Altitude) Tests. Mode C tests are performed using the Mode C Encoder Simulator on the AN/APM-239.

1. Set AN/APM-123 MODE to C and FUNCTION switch to SYSTEM.

2. Set C-6280(P)/APX M-C to ON and all other mode switches to OUT.

3. Set MODE C ENCODER SIMULATOR switches C, A_4, and B_1 to up positions. (This setting represents an altitude of 3200 feet; refer to table 4-4.)

4. Preset code for 3200 feet ($\begin{matrix} A & B & C & D \\ 4 & 1 & 1 & 0 \end{matrix}$) AN/APM-123 CODE control. (Refer to table 4-4.)

5. Push and hold the AN/APM-123 PUSH TO TEST switch. The ACCEPT indicator should come on.

Table 4-3. Switch Settings for Emergency Operation

MODE SELECTED	TEST SET SWITCHES		TRANSPONDER SYSTEM		
	MODE	CODE	C-6280(P)/APX TRANSMITTER		SETTINGS
1	1	0000-7300 (CD always 00)	M-1 to ON all others to OUT		00-73
2	2	0000-7777	M-2 to ON all others to OUT	MODE 2 code	0000-7777
3/A	3/A	7700 (for normal use)	M-3/A to ON all others to OUT		0000-7700

Table 4-4. Selected AN/APM-123 and Mode C Encoder Simulator Settings

ALTITUDE (feet)	AN/APM-123				ENCODER SIMULATOR
	A	B	C	D	
1000	0	3	2	0	$C_2 B_1 B_2$
3200	4	1	1	0	$C_1 A_4 B_1$
5200	4	2	1	0	$C_1 A_4 B_2$
8700	6	2	4	0	$A_2 C_4 A_4 B_2$
10000	6	5	2	0	$C_2 A_2 A_4 B_1 B_4$
16000	3	6	2	0	$A_1 C_2 A_2 B_2 B_4$
32000	1	6	0	4	$A_1 B_2 B_4 D_4$
62000	0	4	0	4	$B_4 D_4$
95000	1	0	0	2	$A_1 D_2$

6. Release the PUSH TO TEST switch.

i. Stopping Procedure.

1. To stop the AN/APM-123, release the PUSH TO TEST switch if it is in LOCK position, and set the 28 VDC-115 VAC-OFF power switch to OFF.

2. Stop the auxiliary test equipment as follows:

(a) Set C-6280(P)/APX MASTER switch to OFF.

(b) Set AN/APM-239 PWR ON-OFF switch to OFF.

4-9. PERFORMANCE TESTS AND MEASUREMENTS USING RADAR TEST SET AN/UPM-98A OR AN/UPM-137.

4-10. Performance tests and measurements are made to determine the serviceability of the receiver-transmitter and its conformity to minimum acceptable performance standards. Two radar test sets, AN/UPM-98A or AN/UPM-137, are available for performing these tests. Refer to table 4-1 for appropriate service usage. Test procedures using these test sets are provided in paragraphs 4-11

and 4-12. All tests and measurements, except power supply performance which is included as part of troubleshooting, are made with the receivex-transmitter case closed. If testing indicates misalignment, refer to alignment and adjustment procedures (para. 4-35) and perform the required alignment before continuing the performance testing. If unit or component failure is indicated, refer to the troubleshooting procedures (para. 4-13). Identify and repair malfunction before proceeding with the performance tests.

4-11. PERFORMANCE TESTS AND MEASUREMENTS USING RADAR TEST SET AN/UPM-98A. The following tests and measurements are applicable when using the AN/UPM-98A test set and associated test equipment.

WARNING

Ensure that the MASTER switch, on the C-6280(P)/APX on the AN/APM-239, is in OFF or STBY before disconnecting cable between ANT. J5 on the receiver-transmitter and HP IN on the AN/UPM-98A. This prevents damage to the receiver-transmitter.

a. Preliminary Procedures. Assemble and connect the receiver-transmitter and test equipment as shown in figure 4-2, and described below. Warmup time for the AN/UPM-98A is one hour. All other test equipment should be allowed to warmup for a minimum of ten minutes before starting test procedures.

1. Test Set, Transponder, AN/APM-239 with C-6280(P)/APX inserted.

(a) Connect PWR INPUT to the 115 vac, 400 Hz voltage source.

(b) Connect TRANSPONDER power and control jack to POWER, CONTROL and VIDEO jack (J1) on the receiver–transmitter.

(c) Connect SUPP OUT to AC SIGNAL INPUT on electronic counter.

(d) Set all controls and switches as directed in table 4-2.

2. Radar Test Set, AN/UPM-98A.

(a) Connect power cord to the 115 vac, 60 Hz voltage source .

(b) Connect a jumper cable from DELAYED TRIGGER (XTAL MARK & SYNC) to TRIG input (INTERROGATION CODER).

(c) Connect a jumper cable from SG IN to SG OUT.

(d) Terminate LP IN with dummy load plug 8P15 attached.

(e) Connect HP IN with cable of known loss to ANT. (J5) on the receiver-transmitter.

(f) Connect SUP TRIGGER (XTAL MARK & SYNC) to EXT SYNC on AN/USM-140B.

(g) Connect VIDEO OUT to VERTICAL PREAMP A on AN/USM-140B.

(h) Set all controls and switches as shown in table 4-5.

3. Oscilloscope, AN/USM-140B.

(a) Connect power cord to the 115 vac, 60 Hz voltage source.

(b) Ensure that EXT SYNC is connected to SUP TRIGGER (XTAL MARK & SYNC) on AN/UPM-98A.

(c) Ensure VERTICAL PREAMP A is connected to VIDEO OUT (CAL-CONTROL) on AN/UPM-98A.

(d) Set POWER ON.

(e) Set all controls and switches to preliminary settings required to obtain a presentation on the oscilloscope.

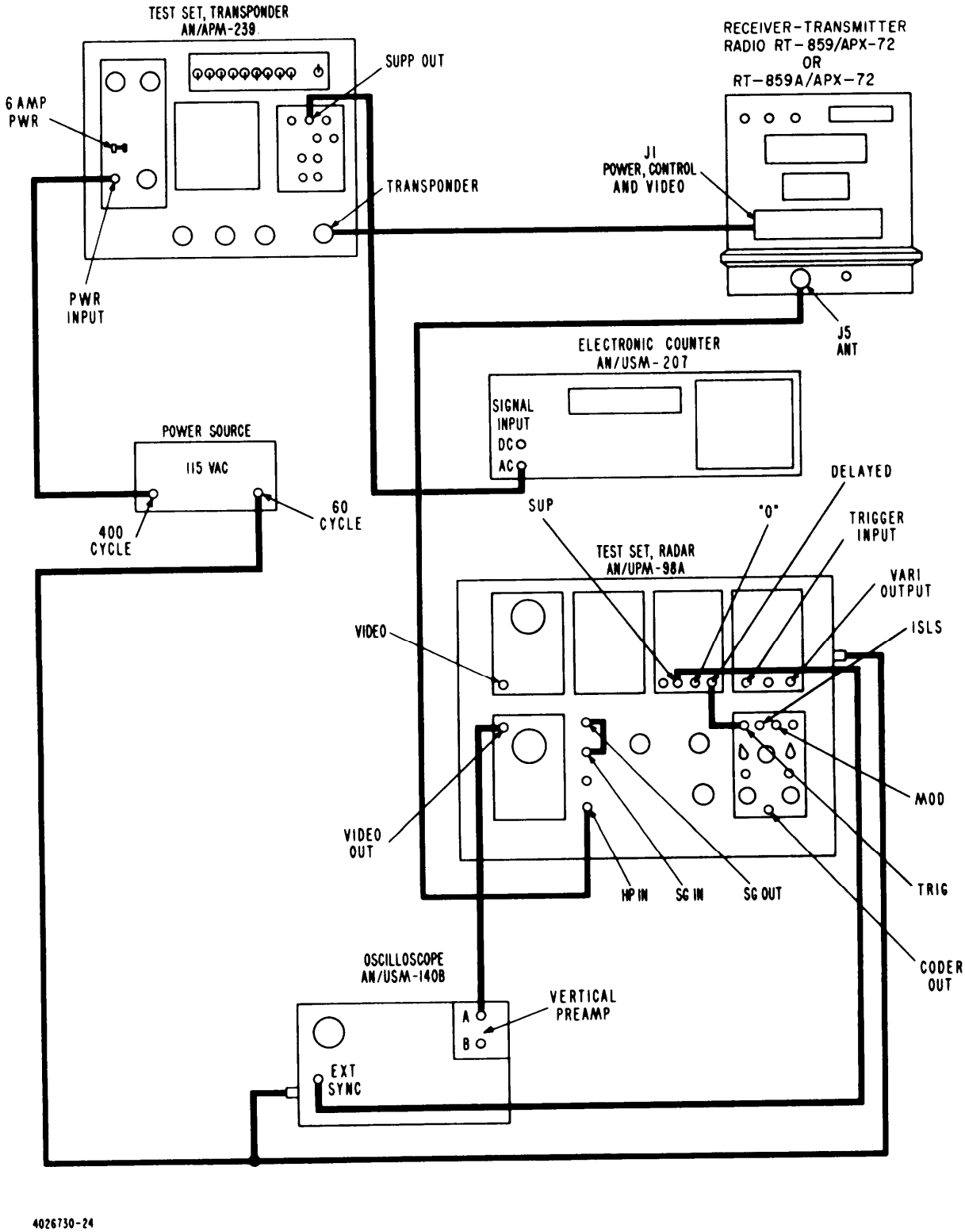


Figure 4-2. Performance Tests and Measurements (Excluding Mode 4) Test Setup

Table 4-5. preliminary Control Settings Radar Test Set, AN/UPM-98A

CONTROL	POSITION
RADAR TEST SET TS-1253A/UP	
DISPLAY UNIT	
INTEN	Fully CCW
FOCUS	Center
HOR	Center
VERT	Center
75 Ω	OUT
VOLTS/IN	20
VIDEO SENS	CAL
SCALE	Fully CCW
ASTIG	Center
SWEEP & INTEN MARK UNIT	
SWEEP SPEED RANGE	1-30
SWEEP SPEED ADJUST	Center
MARKER TRIGGER	NORMAL
INTENSITY MARKS RANGE	OFF
INTENSITY MARKS LEVEL	Fully CCW
XTAL MARK & SYNC UNIT	
SWEEP DELAY RANGE	0
SWEEP DELAY COARSE	Fully CCW
SWEEP DELAY FINE	Fully CCW
TRIGGER DELAY RANGE	0
TRIGGER DELAY COARSE	Fully CCw
TRIGGER DELAY FINE	Fully CCW
SYNC SELECT	INT
XTAL MARK LEVEL	Fully CCW
PRF	Center
SUP	Fully CCW
SIF CODER UNIT	
CODE	0000
FUNCTION	N
SUB-PULSE SELECT	OFF
LEVEL	LO
SUB-PULSE POS	0
PULSE WIDTH	0.45
AMPLITUDE	Fully CCW
INTERLEAVE	Fully CCW
POWER ON-OFF	

CONTROL	POSITION
CODER SIMULATOR SM-197A/UPM-98	
ATTENUATION	Fully CCW
SG FREQUENCY	As required
WAVEMETER INPUT	SIG GEN
WAVEMETER FREQUENCY	As required
CAL–CONTROL UNIT	
METER SELECT	CAL
WM SENS	Fully CCW
VIDEO OUT	As required
CAL ADJ	Fully CCW
TRIGGER	DEMOD
INTERROGATION CODER	
VIDEO Selector Switch	CODE
Sub-Pulse Position Control	0
ISLS LEVEL Control	0
Mode Selector Switch	2
Function Selector Switch	MOD-INT
CODE WIDTH Control	Center
CODE LEVEL Control	Fully CCW
TRIG Connector Terminate Switch (75 Ω)	Off
MOD Connector Terminate Switch (75 Ω)	Off
ISLS Connector Terminate Switch (75 Ω)	Off
ISLS Selector Switch	OUT
Substitute Pulse Selector Switch	OUT
ISLS WIDTH Control	Center
VIDEO LEVEL Control	Center
POWER ON-OFF	ON

4. Receiver-TRansmitter RT-859/APX-72, RT-859A/APX-72.

(a) Ensure that POWER, CONTROL and VIDEO jack (J1) is connetted to the TRANSPONDER power and control jack on the AN/APM-239.

(b) Ensure that ANT. (J5) is connected to HP IN on the AN/UMP-98A.

(c) Set MODE 2 code switches to 7777.

5. Electronic Counter (Hewlett-Packard 5245L or equivalent).

(a) Connect power cord to the 115 vat, 60 Hz voltage source.

(b) Ensure that AC SIGNAL INPUT is connected to SUPP OUT on the AN/APM-239.

(c) Set POWER ON.

(d) Set TIME BASE to 1 SECOND; set FUNCTION switch to FREQUENCY.

b. Starting Procedures. Adjust and preset controls and switches as follows:

NOTE

Verify that AN/APM-239 AC switched power light is illuminated.

1. Set C-6280(P)/APX (AN/APM-239) MASTER switch to STBY, M-2 to ON.

2. AN/UPM-98A

(a) TRIGGER (CAL-CONTROL) to INT.

(b) Adjust CAL-ADJ (CAL-CONTROL) to obtain a full scale meter indication.

(c) METER SELECT (CAL-CONTROL) to 500 PRF.

(d) Adjust AN/USM-140B to view an interrogation pulse pair and adjust pulse width to 0.8 ±0.1 µs by rotating CODE WIDTH control on AN/UPM-98A.

(e) Set SENSITIVITY (VOLTS RMS) to 10 and adjust outer level control as necessary to trigger counter.

(f) Adjust PRF (XTAL MARK & SYNC) for a counter indication of 500 PRF.

(g) VIDEO OUT (CAL-CONTROL) to SIG MON.

(h) ISLS SELECT (INTERROGATION CODER) to 2 µs.

(i) Adjust ISLS pulse width to 0.8±0.1 µs by rotating ISLS WIDTH control.

(j) ISLS SELECT to CHECK.

(k) Adjust SG FREQUENCY for 1030 MHz by zero beating the first interrogation pulse with precision 1030 MHz ISLS pulse. Set ISLS SELECT to OUT.

(1) Adjust ATTENUATION FOR A-60 dBV signal at ANT.J5 of RT-859/APX-72. Use the following formula: ATTENUATION dial indication equals 60 dBV minus SG IN to HP IN loss minus cable loss; i.e. , ATTENUATION dial indication = 60 dBV -32.2 (from calibration chart) - 1.4 (cable loss 0.23 x 6 ft) = 26.4.

(1) VIDEO OUT TO SHAPE

3. C-6280(P)/APX(AN/APM-239) MASTER switch to NORM.

4. Adjust AN/USM-140B to observe demodulated transmitted reply pulses.

c. Receiver Sensitivity Tests. These tests determine if the receiver-transmitter responds properly to all the interrogation patterns that might be encountered. Indication of proper response, to authentic interrogations of minimum signal level,

are obtained by interrogating the receiver-transmitter with the AN/UPM-98A and determining that responses appear 90 percent of the time. Minimum performance standards and sensitivity test procedures are listed in table 4-6.

d. Receiver Bandwith and Center Frequency Tests. These tests determine that the receiver bandwidth and center frequency are within the required limits of the minimum performance standards in table 4-7. The tests consist of interrogating the receiver-transmitter in mode 2 with the AN/UPM-98A test set. perform the preliminary procedures in paragraph 4-11 a. and b. before performing the procedures of table 4-7.

e. Transmitter Frequency and Power Measurements. These measurements determine that the transmitter frequency and power outputs are within the limits of the minimum performance standards in table 4-8. The measurements consist of interrogating the receiver-transmitter in mode 2 with the AN/UPM-98A and determining the frequency and power output of the reply pulse. Perform preliminary procedures of paragraph 4-11 a. and b. , then the procedures in table 4-8.

f. Automatic Overload Control (AOC) Test. This test determines that the automatic overload circuitry in the receiver-transmitter is limiting the reply rate to 1200 ±100 replies per second. The test consists of interrogating the receiver-transmitter at 3 dB above MTL and then increasing interrogation rate until AOC action begins. Perform preliminary procedures of paragraph 4-11 a. and b., then the procedures of table 4-9.

g. Interrogation Side Lobe Suppression (ISLS) Test. This test determines that the operation of the side lobe detection and decoding circuitry is within the limits of the minimum performance standards in table 4-10. Perform the preliminary procedures of paragraph 4-11 a. and b., then the procedures of table 4-10.

h. Suppression. These tests determine that the receiver-transmitter is generating an external suppression pulse to suppress operation of external equipment and an internal suppression pulse to suppress internal functions during certain operations . perform the preliminary procedures of paragraph 4-11 a. and b., then the procedures in table 4-11.

i. Mode 1, 2, 31A, Test, and C Reply Tests. These tests determine that the receiver-transmitter reply pulse trains are spaced within the required performance standards listed in table 4-12 (for modes 1, 2, 3/A, test, and C). Pulse spacing tests require the use of 1.45 µs markers to examine the reply pulse spacing. Perform the preliminary procedures of paragraph 4-11 a. and b. , then the procedures in table 4-12.

j. Mode 4 Reply Tests. These tests determine that mode 4 circuitry is functioning within the minimum performance standards of table 4-14. The AN/APM-245, Test Set, Simulator is required to modulate the AN/UPM-98A for mode 4 interrogation, and to provide the mode 4 reply through the AN/APM-239. Tests are conducted with the receiver-transmitter and test equipment assembled and connected as shown in figure 4-3. Connect equipment and perform preliminary procedures as follows preparatory to the procedures of table 4-14.

Table 4-6. Receiver Sensitivity, Minimum Performance Standards Using AN/UPM-98A

STEP		PROCEDURE	PERFORMANCE STANDARD
1.	Normal sensitivity	a. On AN/UPM-98A (CAL-CONTROL) set METER SELECT to 500 PRF and TRIGGER to DEMOD. Slowly adjust ATTENUATION until suppression count on electronic counter indicates an average of 400 suppressions. Decrease ATTENUATION (CCW) until an average count of 450 suppressions (90% replies) is indicated on counter. Read ATTENUATION dial and compute receiver sensitivity using formula in paragraph 4-11 b.3. (k).	-90 dBV ±3 with a maximum difference of 1 dBV between modes of interrogation.
		b. Set C-6280(P)\APX (AN/APM-239) M-2 to OUT, M-1 to ON. On AN/UPM-98A (INTERROGATION CODER) set MODE SELECT to 1. Perform procedures of step la.	-90 dBV ±3 with a maximum difference of 1 dBV between modes of interrogation.
		c. Set C-6280(P)/APX (AN/APM-239) M-1 to OUT, M-3/A to ON. On AN/UPM-98A (INTERROGATION CODER) set MODE SELECT to 3/A. Perform procedures of step la.	-90 dBV ±3 with a maximum difference of 1 dBV between modes of interrogation.
		d. Set C-6280(P)\APx (AN/APM-239) M-3/A to OUT, M-C to ON. On AN/UPM-98A (INTERROGATION CODER) set MODE SELECT to C. Perform procedures of step la.	-90 dBV ±3 with a maximum difference of 1 dBV between modes of interrogation.
2.	Low sensitivity	Set C-6280 (P)/APX(AN/APM-239) to OUT, M-2 to ON, MASTER to LOW. On AN/UPM-98A (INTERROGATION CODER) set MODE SELECT to 2 and adjust ATTENUATION until suppression count on electronic counter indicates an average 400 suppressions. Decrease ATTENUATION (CCW) until an average count of 450 suppressions is indicated on counter. Read ATTENUATION DIAL and compute receiver sensitivity	-78 dBV ±2 or as directed by local command.

Table 4-6. Receiver Sensitivity, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
2. Low sensitivity (Cont)	using formula of paragraph 4-11.b.3. (1). Repeat for MODES 1, 3/A and C.	

Table 4-7. Receiver Bandwidth and Center Frequency, Minimum Performance Standards Using AN/UPM-98A

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Lower sideband FL6 frequency measurement	a. On AN/UPM-98A (CAL-CONTROL) set TRIGGER to DEMOD and slowly adjust ATTENUATION until suppression count on electronic counter indicates an average of 400 suppressions. Decrease ATTENUATION (CCW) until an average count of 450 suppressions (90% replies) is indicated on counter. Note indication on ATTENUATION dial which will be reference MTL for this procedure. b. Decrease ATTENUATION (CCW) until dial indicates 6 dB less than reference MTL. Decrease SG FREQUENCY (CCW) until an average suppression count of 450 is indicated on electronic counter. c. Set WAVEMETER INPUT to SIG GEN, METER SELECT to WM, and adjust WAVEMETER FREQUENCY until PRF meter needle dips, indicating resonance. Readjust WM SENS to ensure maximum needle deflection. Record WAVEMETER FREQUENCY indication and compute FL6 using calibration curves provided with AN/UPM-98A.	
2. Upper sideband FH6 frequency measurement	Detune WAVEMETER FREQUENCY and increase SG FREQUENCY through a suppression count of 500 until an average suppression count of 450	

Table 4-7. Receiver Bandwidth and Center Frequency Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
2. Upper sideband FH6 frequency measurement (Cont)	is indicated on electronic counter. Repeat procedures of step 1.c. to obtain FH6.	
3. Bandwidth computations	Calculate and record center frequency and bandwidth at -6-dB points.	
	Center frequency (FO) $FO = \frac{FL6 + FH6}{2}$	1030 ±1.5 MHz
	Bandwidth (BW) $BW = FH6 - FL6$	7 MHz minimum

Table 4-8. Transmitter Frequency and Power, Minimum Performance Standards Using AN/UPM-98A

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Frequency output	a. Set C-6280 (P)/APX (AN/APM-239) MASTER to OFF. Set MODE 2 code (receiver-transmitter) to 7777.	
	b. Connect a 10 dB pad (minimum power rating 5 Watts, frequency 1090 MHz) between ANT. J5 on the receiver-transmitter and cable connected to HP IN on AN/UPM-98A.	
	c. Set C-6280(P)/APX MASTER switch to STBY for 1 minute; then to NORM.	
	d. On AN/UPM-98A set WAVEMETER INPUT to DEMOD, METER SELECT to WM, and adjust WAVEMETER FREQUENCY for maximum needle dip on PRF meter, varying WM SENS as required. Observe the WAVEMETER FREQUENCY dial and correlate setting with test set calibration curves to determine frequency. Detune WAVEMETER FREQUENCY.	1090 ±3.0 MHz

Table 4-8. Transmitter Frequency and Power, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
1.	Frequency output (Cent)	e. Set C-6280(P)/APX MASTER switch to OFF. Remove 10 dB pad and reconnect cable between ANT. J5 on receiver-transmitter and HP IN on AN/UPM-98A. Set C-6280(P)/APX MASTER switch to STBY for 1 minute then to NORM.	
2.	Power output	a. Set VIDEO OUT (CAL-CONTROL) on AN/UPM-98A to POWER. Adjust AN/USM-140B to view F_1, pulse and measure peak-to-peak voltage amplitude.	
		b. Adjust AN/USM-140B to observe F_2 pulse and measure peak-to-peak voltage amplitude.	
		c. Compute power levels using calibration charts provided with AN/UPM-98A corresponding to peak voltage amplitudes adding rf connecting cable attenuation (approximately 1 dB per 5 feet) to obtain power outputs.	F_1 = 27 ±3 dBW F_2 = F_1 ±1 dBW

Table 4-9. Automatic Overload Control, Minimum Performance Standards Using AN/UPM-98A

STEP	PROCEDURE	PERFORMANCE STANDARD
Reply rate limiting	a. Set MODE 2 code (receiver-transmitter) to 7777. On AN/UPM-98A (CAL-CONTROL) set METER SELECT to 500 PRF, TRIGGER to DEMOD, and observe electronic counter for an average suppression count of 500.	
	b. Increase ATTENUATION until an average of 450 is indicated on counter. Decrease ATTENUATION 3dB. Set METER SELECT to 5000 PRF. Increase PRF (XTAL Mark & Sync) until counter indication no longer	RATE: 1200 ±100 replies per second (from 3-50 dBV above MTL).

Table 4-9. Automatic Overload Control, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
Reply rate limiting (Cont)	increases, at which point AOC action begins.	
	c. Repeat step b for MODES 1, 3/A, and C with fully coded replies.	(from 3-50 dBV above MTL)

Table 4-10. Interrogation Side Lobe Suppression, Minimum Performance Standards Using AN/UPM-98A

STEP	PROCEDURE	PERFORMANCE STANDARD
	WARNING Do not place the MASTER switch, on the C-6280(P)/APX on the AN/APM-239, to any position but OFF or STBY when using the following connections. This will prevent damage to the transmitter.	
1. ISLS equal level of interrogation	a. Set MASTER switch on C-6280(P)/APX (AN/APM-239) to STBY. ON AN/UPM-98A, remove cable between SIG IN and SIG OUT; disconnect cable from HP IN and connect cable to SIG OUT; set VIDEO OUT (CAL-CONTROL) to SIG MON; set ISLS level (INTERROGATION CODER) to 0, ISLS SELECT to 2 µs, and adjust ISLS amplitude (CAL) observing AN/USM-140B for a side lobe pulse equal to level of first interrogation pulse. Set ISLS SELECT to OUT. Disconnect cable to counter from SUPP OUT and connect to 0 trigger (XTAL MARK & SYNC) and adjust PRF for a count of 500 ±3. Disconnect counter from 0 trigger and connect to SUPP OUT on AN/APM-239.	Read 500 ±3 suppressions en counter.
	b. Adjust ATTENUATION on AN/UPM-98A for an average count of 450 suppressions on counter. Indication on ATTENUATION dial is reference MTL for this procedure.	

Table 4-10. Interrogation Side Lobe Suppression, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
1.	ISLS equal level of interroga-tion (Cont)	c. Set ISLS SELECT (INTERROGATION CODER) to 2 µs. Observe counte for 0 to a maximum of 5 suppressions while interrogating over an attenuation range 3 dB to 50 dB lower than ATTENUATION indication defined as references MTL.	Read 0 to 5 replies on counter.
		d. Repeat steps b and c for MODES 1, 3/A and C.	
2.	ISLS 9 dB below in-terrogation	Set ISLS level (INTERROGATION CODER) to 9. Observe counter for a minimum of 495 replies averaged over a ten-second inter-Val while interrogating over an attenuation range 3 dB to 50 dB lower than ATTENUATION indication defined as reference MTL. (Repeat for MODES 1, 3/A, and C).	Read 495 suppressions minimum on counter averaged over a ten-second interval.

Table 4-11. Suppression, Minimum Performance Standards Using AN/UPM-98A

STEP		PROCEDURE	PERFORMANCE STANDARD
1.	External Suppression out	a. On AN/UPM-98A (CAL-CONTROL) set TRIGGER to DEMOD and slowly adjust ATTENUATION until an average suppression count of 400 is indicated on counter. Decrease ATTENUATION (CCW) until an average count of 450 suppressions is indicated on counter. ATTENUATION dial indication is reference MTL for this procedure. Set ATTENUATION 3 dB lower than reference MTL. Disconnect cable from AC SIGNAL INPUT on counter and connect to VERTICAL AMPLIFIER B on AN/USM-140B.	
		b. Observe on AN/USM-140B, that suppression pulse reaches a minimum of 18 volts by the time F_1 pulse	

Table 4-11. Suppression, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
1.	External Suppression out (Cont)	reaches 10% of its amplitude and remains at 18 volts or greater until the F2 pulse has-decayed to the 10% level. Suppression level shall be less than 5 volts 5 µs after the F2 pulse decays to 10% level.	
	c.	Disconnect the cable from the XTAL MARK SYNC SUPP OUT jack and connect to "O" TRIGGER OUT, sync oscilloscope externally. Connect a cable between the XTAL MARK and SYNC SUPP OUT and the APM-239 SUPPRESSION IN. Slowly adjust the XTAL MARK and SYNC SUPP WIDTH control from full CCW to full CW.	Verify that reply train is suppressed.
	d.	Adjust SUPP WIDTH control back to its CCW Position.	Verify that reply train is present.
	e.	Return cables and oscilloscope controls to starting position.	
	f.	Disconnect vertical amplifier B input on AN/USM-140B from SUPPRESSION OUT on AN/APM-239.	
2.	Internal Suppression	a. On AN/UPM-98A (INTERROGATION CODER) remove cable connection from TRIG. Connect coax tee connector with two cables attached to TRIG input. Connect one cable to 0 TRIGGER and other cable to DELAYED TRIGGER on XTAL MARK & SYNC chassis. Set MODE 2	

Table 4-11. Suppression, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
2. Internal Suppression (Cont)	code receiver-transmitter to 7777. Set TRIGGER DELAY RANGE (XTAL MARK & SYNC) on AN/UPM-98A to 50-750. This allows the receiver-transmitter to be interrogated twice. b. On AN/UPM-98A (XTAL MARK & SYNC) vary TRIGGER DELAY (COARSE and FINE) until the second set of replies appear approximately 50% of the time on the AN/USM-140B. Adjust leading edge of F2 pulse of first reply train to the first vertical line on the grid of the AN/USM-140B. c. Set VIDEO OUT (CAL-CONTROL) to SIG MON and measure the time delay between first vertical line on AN/USM-140B and P_1 pulse of second interrogation. The time delay should be between 75 and 100 μs.	

Table 4-12. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-98A

STEP		PROCEDURE	PERFORMANCE STANDARD
1.	Frame spacing	a. On AN/UPM-98A (CAL-CONTROL), set METER SELECT to 500 PRF, TRIGGER to DEMOD. Increase ATTENUATION to obtain an average counter indication of 450. Observe ATTENUATION dial indication, this is reference MTL for this procedure. Set ATTENUATION 3dB lower than reference MTL.	
		b. On AN/UPM-98A (CAL-CONTROL) , disconnect cable to VIDEO OUT. Insert a coax tee connector, reconnect original cable to one end of coax tee and connect a cable between the other end and VIDEO on DISPLAY chassis. Adjust INTENSITY and FOCUS as required to obtain a display. Set TRIGGER (CAL-CONTROL) to INT. On (XTAL MARK & SYNC) set SYNC SELECT to INT 1.45, adjust PRF to indicate 500 ±3 on counter, XTAL MARK LEVEL fully CW, TRIGGER DELAY RANGE to 1-11, SWEEP DELAY RANGE to 5-50, SWEEP SPEED RANGE (SWEEP & INTEN MARK) to 1-3. Volts/IN (DISPLAY) to 1.	
		c. View crystal markers on (DISPLAY) scope and adjust SWEEP SPEED ADJUST (SWEEP & INTEN MARK) and SWEEP DELAY (XTAL MARK & SYNC) until markers are spaced exactly 29 small divisions apart (each small division equals 0.05 µs).	
		d. Adjust SWEEP DELAY (FINE and COARSE) to locate F_1 on scope and align F_1 with the negative peak on a crystal marker by adjusting FINE TRIGGER DELAY (XTAL MARK & SYNC). Adjust COARSE and FINE SWEEP DELAY counting 15 crystal markers including F_1 reference. The leading edge of F_2 should be aligned with the 15th marker ±0.05 µs.	20.3 ±0.05 µs. (See figure 2-5)
		e. Set MODE 2 code (receiver-transmitter) to 0007. Repeat step 1.d.	20.3 ±0.05 µs.

Table 4-12. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

	STEP		PROCEDURE	PERFORMANCE STANDARD
1.	Frame spacing (Cont)	f.	Set C-6280(P)/APX (AN/APM-239) IDENT-MIC to IDENT and release. View I/P replies on AN/USM-140B timing duration of appearance.	15 to 30 seconds.
		g.	Referring to step 1.d., align F_1 pulse with negative peak of a marker. Count to 18th marker and initiate I/P. F_3 should be aligned with 18th marker.	24.65 ±0.5 µs.
		h.	Set SYNC SELECT to INT on AN/UPM-98A and adjust PRF for 500 ±3 on counter.	
2.	Pulse width		On the AN/USM-140B, measure width of F_1 pulse at the 50% point.	0.45 ±0.1 µs.
3.	Rise time		On the AN/USM-140B, observe and measure rise time of F_1 pulse from 10% to 90% amplitude points on leading edge of pulse.	0.05 to 0.1 µs.
4.	Fall time		On the AN/USM-140B, observe and measure fall time of F_1 pulse from 90% to 10% amplitude points on trailing edge of pulse.	0.05 to 0.2 µs.
5.	Mode 2 replies	a.	On the receiver-transmitter rotate MODE 2 code select dials in sequence observing appearance of proper code pulses with each change on AN/USM-140B.	Verify F_1, C_1, A_1, C_2, A_2, C_4, A_4, B_1, D_1, B_2, D_2, B_4, D_4, and F_2 pulses appear in proper sequence. (See figure 2-5.)
		b.	On AN/APM-239, place SPECIAL in X PULSE and observe that X pulse appears in proper location in reply train. Return SPECIAL to CAUTION LIGHT RESET.	(See figure 2-6.)
		c.	Set receiver-transmitter code switches to 7777. Set C–6280 (P)/APX IDENT MIC to IDENT and release.	Verify that a normal reply train and a F3 pulse are present. (See figure 2-6.)

Table 4-12. Mode 1, 2, 3/A, Test, and C Repliess, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
5.	Mode 2 replies (Cont)	d. Set C-6280(P)/APX MASTER switch to EMER.	Verify one normal reply pulse train and three sets of framing pulses are present. (See figure 2-6)
		e. Set C-6280(P)/APX MASTER switch to STBY.	Verify reply pulse not present.
		f. Set C-6280 (P)/APX MASTER switch to NORM, M–2 to OUT.	Verify reply pulses not present.
6.	Mode 1 replies	a. On AN/UPM-98A, set (INTERROGATION CODER) MODE SELECT to 1. On C-6280(P)/APX, set M-1 to ON and rotate MODE 1 code select dials in sequence observing appearance of proper code pulses with each change on AN/USM-140B.	Verify that F_1, A_1, A_2, A_4, B_1, B_2, and F_2 pulses appear in proper sequence. (See figure 2-5.)
		b. Repeat step 5.b.	
		c. Set C-6280 (P)/APX MODE 1 CODE to 73, IDENT-MIC to IDENT and release .	Verify that two reply pulse trains are present. (See figure 2-6.)
		d. Set C-6280(P)/APX MASTER switch to EMER.	Verify one normal reply pulse train and three sets of framing pulses are present. (See figure 2-6.)
		e. Set C-6280(P)/APX MASTER switch to NORM, M-1 to OUT.	Verify reply pulses not present.
7.	Mode 3/A replies	a. On AN/UPM-98A (INTERROGATION CODER) set MODE SELECT to 3/A. On C-6280(P)/APX, set M-3/A to ON and rotate MODE 3/A code select dials in sequence observing appearance of proper	Verify F_1, C_1, A_1, C_2, A_2, C_4, A_4, B_1, D_1, B_2, D_2, B_4, D_4, and F_2 pulses appear in proper sequence. (See figure 2-5.)

Table 4-12. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
7.	Mode 3/A replies (Cont)	code pulses with each change on AN/USM-140B.	
	b.	Repeat step 5.b.	
	c.	Set C-6280 (P)/APX MODE 3/A CODE 7777, IDENT-MIC to IDENT and release.	Verify that a normal reply pulse train and an F_3 pulse are present. (See figure 2-6.)
	d.	Set C-6280 (P)/APX MASTER switch to EMER.	Verify that F_1, A_1, A_2, A_4, B_1, B_2, B_4, F_2, F_3, F_4, F_5, F_6, F_7, and F_8 only are present. (See figure 2-6.)
	e.	Set C-6280 (P)/APX MASTER switch to NORM, M-3A to OUT	Verify reply pulses not present.
8.	Test mode replies	a. Disconnect cable between TRIGGERS DELAYED (XTAL MARK & SYNC) and TRIG (INTERROGATION CODER) at TRIG input and connect to TRIGGER INPUT (SIF CODER). Connect VARI OUTPUT (SIF CODER) to MOD INPUT (INTERROGATION CODER). Set VIDEO OUT (CAL-CONTROL) to SIG MON. On SIF CODER set FUNCTION SELECT to N, code dial A to 2, and SUB PULSE SELECT to A2. FUNCTION SELECT (INTERROGATION CODER) to MODE LOW. Adjust AMPLITUDE CW SUB PULSE POSITION (SIF CODER) to position pulse 2 to 6.5 µs measured from leading edge of P1 on AN/USM-140B. Adjust CODE WIDTH (INTERROGATION CODER) to obtain 0.8 µs pulse width. Return VIDEO OUT to SHAPE.	
	b.	Set MODE 3/A code (C-6280 (P)/APX to 7777. Hold RAD TEST-MON to MD TEST.	VerifY F_1, C_1, A_1, C_2, A_2, C_4, A_4, B_1, D_1, B_2, D_2, B_4, D_4, and F_2 pulses are present. (See figure 2-5.)

Table 4-12. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
8.	Test mode replies (Cont)	c. Set RAD TEST-MON to OUT.	Verify reply pulses not present.
		d. Disconnect cable from TRIGGER INPUT (SIF CODER) and reconnect to TRIG (INTERROGATION CODER). Set FUNCTION SELECT (INTERROGATION CODER) to INT.	
9.	Mode C replies (RT-859/ APX-72)	a. On AN/UPM-98A (INTERROGATION CODER) set MODE SELECT to C. Set M-C (C-6280(P)/APX) to ON. Set MODE C ENCODER SIMULATOR (AN/APM-239) to $C_1, A_1, C_2, A_2, C_4, A_4, B_1, B_2, D_2$, and B_4 observing appearance of each pulse on AN/USM-140B as it is switched on.	Verify that F_1, F_2, and all other pulses, except X,D1 and D_4. are present. (See figure 2-5.)
		b. Set AN/APM-239 MODE C ENCODER SIMULATOR switch to D4,	Verify that, in addition to pulses above, D_4 and SPI (F_3) pulses appear. (See figure 2-6.)
		c. Set AN/APM-239 MODE C ENCODER SIMULATOR switches to OUT.	Verify that only F_1 and F_2 pulses are present.
		d. Set C-6280(P)/APX IDENT MIC to IDENT and release.	Verify no effect on mode C reply.
		e. Set C-6280(P)/APX MASTER switch to EMER.	Verify no effect on mode C reply.
		f. Set C-6280(P)/APX MASTER switch to NORM, M-C to OUT.	Verify no reply pulses present.
9A.	Mode C replies (RT-859A/ APX-72)	a. On AN\/UPM-98A (INTERROGATION CODER) set MODE SELECT to C. Set M-C (C-6280(P)/APX) to ON. Set MODE C ENCODER SIMULATOR (AN/APM-239) to $C_1, A_1, C_2, A_2, C_4, A_4, B_1, B_2, D_2, B_4$, and D_4 observing appearance of each pulse on AN/USM-140B as it is switched on.	verify that F_1, F_2, and all other pulses, except X and D_1 are present. (See figure 2-5.)

Table 4-12. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
9A.	Mode C replies (RT-859A/APX-72) (Cont)	b. Set AN/APM-239 MODE C ENCODER SIMULATOR switches to OUT.	Verify that only F_1 and F_2 pulses are present.
		c. Set C-6280(P)/APX IDENT-MIC to IDENT and release.	Verify no effect on mode C reply.
		d. Set C-6280(P)/APX MASTER switch to EMER.	Verify no effect on mode C reply.
		e. Set C-6280(P)/APX MASTER switch to NORM, M-C to OUT.	Verify no reply pulses present.
10.	Auxiliary trigger	On AN/UPM-98A (INTERROGATION CODER) set FUNCTION SELECT to TEST (+) , MODE SELECT to 2, connect a cable from CODER OUT to B input VERTICAL AMPLIFIER AN/USM-140B. Adjust VIDEO LEVEL to obtain 40 volts on AN/USM-140B. Disconnect cable connection to B input of VERTICAL AMPLIFIER of AN/USM-140B and connect it to AUX TRIG on AN/APM-239.	Verify two pulses present on trace A AN/USM-140B.

Table 4-13. Preliminary Control Settings, Test Set, Simulator AN/APM-245, Using AN/UPM-98A

CONTROL	POSITION
TEST WORD (1 through 37)	Down
METER	
SCALE	X10
FUNCTION	INT/EXT
MOD 4 REPLY	OFF
AM	Fully CCW
DELAY	Fully CCW
AUXILIARY PULSE	OFF
AM	Fully CCW
DELAY	Fully CCW

Table 4-13. Preliminary Control Settings, Test Set, Simulator AN/APM-245, Using AN/UPM-98A (Cont)

CONTROL	POSITION
DISPARITY	OFF
DL1	Fully CCW
DL2	Fully CCW
INT PRF FREQ ADJ	Fully CCW
GO NO-GO	OFF
PRF SEL	EXT
TEST WORD AM	Fully CCW
MKR AM	Fully CCW
ON-OFF	ON

Table 4-14. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-98A

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Trigger level	a. Disconnect cable from EXT TRIG (AN/APM-245) and connect to TRIG (INTERROGATION CODER) on AN/UPM-98A. Set VIDEO OUT (CAL CONTROL) to SIG MON, FUNCTION (INTERROGATION COCER) to INT, mode select switch to 4 and adjust AN/USM-140B to observe interrogation pulses. Adjust width of first pulse to 0.5 µs using CODE WIDTH control. Set ISLS SELECT (INTERROGATION CODER) to 8 µSEC and adjust width of fifth pulse (ISLS pulse) to 0.5 µs using ISLS WIDTH control.	
	b. Disconnect cable from TRIG (INTERROGATION CODER) and connect to EXT TRIG (AN/APM-245). Set FUNCTION (INTERROGATION CODER) to MOD-LOW, ISLS SELECT to OUT, TRIGGER (CAL-CONTROL) to DEMOD, and METER SELECT to 500 PRF. Disconnect cable from 0 TRIG (XTAL MARK & SYNC) and connect to SUPP OUT on AN/APM-239. On AN/APM-245, adjust MODE 4 REPLY AM until counter indicates reading.	
	c. On AN/APM-239, remove 50-Ohm termination from REPLY, then remove	

Table 4-14. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Trigger level (Cont)	cable connection from TRIG MODE 4 and connect to REPLY. On AN/APM-245, adjust MODE 4 REPLY AM for a five-volt reply pulse amplitude on B trace of AN/USM–140B.	
	d. Return cable connection from REPLY to MODE 4 TRIG and place 50-Ohm termination on REPLY. Increase ATTENUATION to obtain an average suppression count of 400 on electronic counter then decrease ATTENUATION to obtain an average suppression count of 450. Reduce ATTENUATION dial setting 3 dB. Observe B trace on AN/USM-140B for trigger pulse characteristics.	Trigger pulse characteristics: Amplitude: 1.5 to 5 v Pulse width: 0.5 to 3.0 µs
2. Video output (RT-859/ APX-72)	Observe pulse characteristics on A trace of AN/USM-140B. Remove cable from MODE 4 TRIG (AN/APM–239) and connect to MODE 4 INTRR. view pulse characteristics on B trace of AN/USM-140B. Set TEST WORD (AN/APM-245) 1 through 37 to up position. Observe that A and B displays on the AN/USM-140B contain 37 pulses with B display pulses being larger in amplitude. Set TEST WORD 5 through 37 to down position.	video pulse characteristics: A display: Equals number of pulses compared with B display. B display: Amplitude: 1.5 to 5 V Pulse width: 0.5 ±0.1 µs
2A. Video output (RT-859A/ APX-72)	Observe pulse characteristics on A trace of AN/USM-140B. Remove cable from MODE 4 TRIG (AN/APM-239) and connect to MODE 4 INTRR. View pulse characteristics on B trace of AN/USM-140B. Set TEST WORD (AN/APM-245) 1 through 37 to up position. Observe that A display on the AN/USM-140B contains 37 pulses and the B display contains 35 pulses with B display pulses being larger in amplitude. Set TEST WORD 5 through 37 to down position.	video pulse characteristics: A display: Contains two more pulses than B display. B display: Amplitude: 1.5 to 5 V Pulse width: 0.5 +0.1 µs

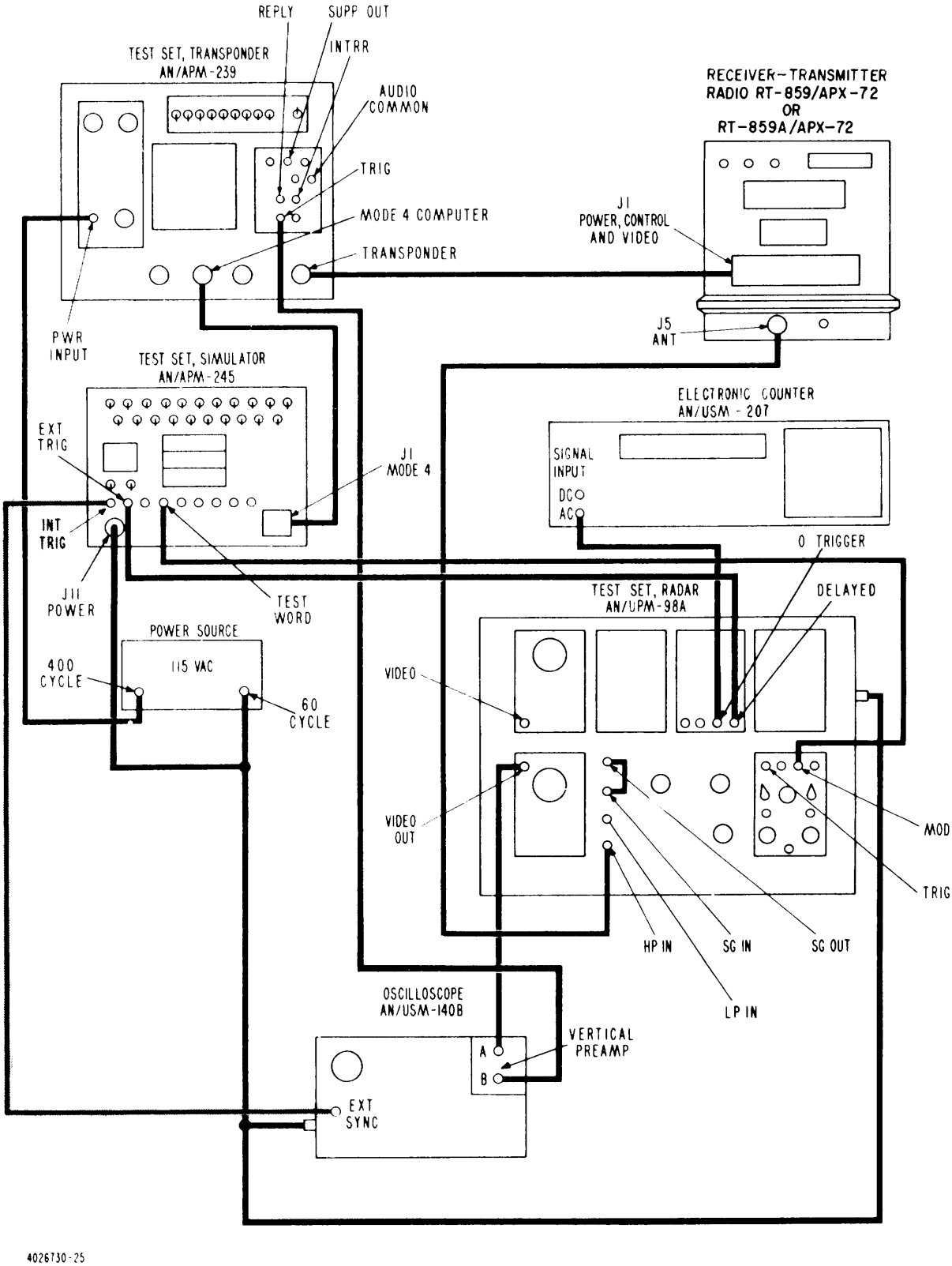


Figure 4-3. Performance Tests and Measurements (Mode 4) Test Setup

Table 4-14. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
		NOTE If a display pulse amplitudes decrease as more test word bits are added, decrease TEST WORD AM. This condition caused by loading MOD input circuit (AN/UPM-98A).	
3. Replies	a.	Set VIDEO OUT (CAL-CONTROL) on AN/UPM-98A to SHAPE. Set MODE 4 AUDIO-LIGHT (C-6280 (P)/APX) on AN/APM-239 to LIGHT. Observe REPLY lamp (C-6280 (P)/APX) on PN/APM-239 lights and three mode 4 reply pulses appear on A input display of AN/USM-140B. Measure risetime and decay time between 10% and 90%.	Verify that REPLY light comes on. Reply pulse characteristics: Duration: 0.45 +0.1 µs Resetime: 0.05 to 0.1 µs Decay time: 0.05 to 0.2 µs Amplitude jitter: 5% or less
	b.	Set C-6280 (P)/APX IDENT-MIC to IDENT and release.	Verify no effect on mode 4 reply.
	c.	Set C-6280 (P)/APX MASTER switch to EMER.	Verify no effect on mode 4 reply.
	d.	Set C-6280 (P)/APX MASTER switch to STBY.	Verify no mode 4 reply.
	e.	Set C-6280 (P)/APX MASTER switch to NORM.	Verify mode 4 reply appears.
4. Reply light	a.	On the AN/UPM-98A, set TRIGGER (CAL-CONTROL) to INT, adjust PRF (XTAL MARK & SYNC) to obtain a counter indication of 91 +2. On the AN/APM-245, set GO NO-GO switch to GO. Press GO/NO-GO pushbutton. REPLY on C-6280 (P)/APX lights. Set GO NO-GO switch to OFF.	Verify REPLY light comes on for period of 2 to 5 seconds.
	b.	Using preceding procedure, adjust to obtain a counter indication of 61 +2. Set GO NO-GO switch to NO-GO. Press GO/NO-GO pushbutton. REPLY on C-6280 (P)/APX does not light. Set GO NO-GO switch to OFF.	Verify REPLY light remains off.

Table 4-14. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
5. Caution light	a.	On the AN/UPM-98A, set TRIGGER (CAL-CONTROL) to INT. Adjust PRF (XTAL MARK & SYNC) to obtain a counter indication of 91 ±2. Set MODE 4 REPLY to OFF. On the AN/APM-245, set GO NO-GO switch to GO. Press GO/NO-GO pushbutton. CAUTION light on AN/APM-239 comes on. Set GO NO-GO switch to OFF, MODE 4 REPLY switch to ON.	Verify CAUTION light comes on for a period of 2 to 5 seconds.
	b.	Using above procedure, adjust PRF to obtain a counter indication of 61 ±2. Set MODE 4 REPLY to OFF. Set GO NO-GO switch to NO-GO. Press GO/NO-GO pushbutton. CAUTION light on AN/APM-239 remains off. Return GO NO-GO switch to OFF.	Verify CAUTION light does not light.
6. Audio output	a.	On AN/APM-239, remove cable from MODE 4 INTRR jack and connect it to AUDIO jack. Set C-6280(P)/APX AUDIO-OUT-LIGHT to AUDIO. Set MODE 4 REPLY (AN/APM-245) to ON. On AN/UPM-98A (XTAL MARK & SYNC) adjust PRF to obtain counter indication of 500 ±3. Observe audio signal on B input of VERTICAL AMPLIFIER AN/USM-140B. Set MODE 4 REPLY (AN/APM-245) to OFF.	Audio signal characteristics: Width of negative part of pulse 500 µs minimum with a pulse amplitude of 3 V p-p (minimum).
	b.	Set AN/APM-245 MODE 4 DISPARITY to DELAY #1 and if audio is present on AN/USM-140B, adjust DL-1 clockwise until audio disappears.	Verify audio signal not present.
	c.	Set AN/APM-245 MODE 4 DISPARITY to OFF.	Verify audio signal present.
	d.	Set C-6280(P)/APX AUDIO-OUT LIGHT to OUT. Set MODE 4 REPLY (AN/APM-245) to ON.	Verify audio signal not present.
7. Limiter	a.	On AN/UPM-98A set METER SELECT to 5000 PRF. Observe reply pulse on A input VERTICAL AMPLIFIER AN/USM-140B.	

Table 4-14. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-98A (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
7.	Limiter (Cont)	b. Set TRIGGER (CAL-CONTROL) to DEMOD and increase PRF (XTAL MARK & SYNC) on AN/UPM-98A until counter indication stops increasing. This indicates point at which mode 4 duty limiter begins operation. (3-50 dBV above MTL).	Rate 1500 to 2500 replies per second.
8.	MTL	On AN/UPM-98A (CAL-CONTROL) , set TRIGGER to INT, METER SELECT to 500 PRF. Adjust PRF (XTAL MARK & SYNC) to obtain a counter indication of 500 ±3. Set TRIGGER (CAL-CONTROL) to DEMOD. Increase ATTENUATION until counter indication drops to 400 average. Decrease ATTENUATION until counter indication reaches 450 average. Compute MTL using formula found in paragraph 4-11.b.3.(1).	-90 dBV ±3.

1. Test Set, Transponder, AN/APM-239.

(a) Connect PWR INPUT to the 115 vat, 400 Hz voltage source.

(b) Connect TRANSPONDER power and control to POWER, CONTROL AND VIDEO J1 on RT-859/APX-72.

(c) Connect MODE 4 COMPUTER to J1 MODE 4 on AN/APM-245.

(d) Terminate AUDIO COMMON with attached termination

(e) Terminate REPLY with a 50 Ohm termination.

(f) Connect MODE 4 TRIG to input B on VERTICAL AMPLIFIER AN/USM-140B.

(g) Set all controls and switches as directed in table 4-2.

2. Test Set, Simulator, AN/APM-245.

(a) Connect J11 POWER to 115 Vat, 60 Hz voltage source.

(b) Ensure that J1 MODE 4 is connected to MODE 4 COMPUTER on AN/APM-239.

(c) Connect TEST WORD to input A on VERTICAL AMPLIFIER AN/USM-140B.

(d) Connect EXT TRIG to DELAYED TRIGGERS (XTAL MARK & SYNC) on AN/UPM-98A.

(e) Set all controls and switches as directed in table 4-13.

3. Test Set, Radar AN/UPM-98A.

(a) Connect power cord to 115 vat, 60 Hz source.

(b) Ensure that DELAYED TRIGGERS (XTAL MARK & SYNC) is connected to EXT TRIG on AN\APM-245.

(c) Connect a jumper cable from SG IN to SG OUT.

(d) Terminate LP IN with dummy load plug 8P15 attached.

(e) Connect HP IN to ANT. J5 on RT-859/APX-72.

(f) Connect SUP TRIGGERS (XTAL MARK & SYNC) to EXT SYNC on AN/USM-140B.

(g) Connect 0 TRIGGER (XTAL MARK & SYNC) to AC SIGNAL INPUT on electronic counter.

(h) Set all controls and switches as directed in table 4-5.

4. Oscilloscope, AN/USM-140B.

(a) Connect power cord to 115 vat, 60 Hz source.

(b) Ensure that input A VERTICAL AMPLIFIER is connected to TEST WORD on AN/APM-245.

(c) Ensure that input B VERTICAL AMPLIFIER is connected to MODE 4 TRIG on AN/APM-239.

(d) Ensure that EXT SYNC is connected to SUP TRIGGERS (XTAL MARK & SYNC) on AN/UPM-98A.

(e) Set POWER ON.

(f) Set all controls and switches to obtain a presentation on oscilloscope.

5. Receiver-Transmitter.

(a) Ensure that POWER, CONTROL & VIDEO J1 is connected to TRANSPONDER power and control on AN/APM-239.

(b) Ensure that ANT.J5 is connected to HP IN on AN/UPM-98A.

6. Electronic Counter (Hewlett-Packard 5245L or equivalent).

(a) Connect power cord to the 115 vac, 60 Hz voltage source.

(b) Ensure that AC SIGNAL INPUT is connected to O TRIGGER (XTAL MARK & SYNC) on AN/UPM-98A.

(c) Set TIME BASE to 1 SEC.

(d) Set FUNCTION switch to FREQUENCY.

(e) Set POWER ON.

7. Preliminary Procedures.

(a) Set TEST WORD switches (AN/APM-245) 1 through 4 to Up position and adjust TEST WORD AM for a 20-volt amplitude on A trace of AN/USM-140B.

(b) Disconnect cable from input A on VERTICAL AMPLIFIER AN/USM-140B and connect to MOD (INTERROGATION CODER on AN/UPM-98A.

(c) Connect VIDEO OUT (CAL-CONTROL) on AN/UPM-98A to input A on VERTICAL AMPLIFIER AN/USM-140B.

(d) Set TRIGGER (CAL-CONTROL) to INT and METER SELECT to CAL.

(e) Adjust CAL-ADJ (CAL-CONTROL) to obtain a full scale meter indication.

(f) Set C-6280(P)/APX (AN/APM-239) MASTER switch to STBY for 1 minute then to NORM and MODE 4 to ON.

(g) On AN/APM-245 set MODE 4 REPLY to ON and adjust AM to mid range.

(h) On electronic counter, set SENSITIVITY (VOLTS RMS) to 10 and adjust outer level control as necessary to trigger counter.

(i) Adjust PRF (XTAL MARK & SYNC) on AN/UPM-98A for a counter indication of 500 ±3.

4-12. PERFORMANCE TESTS AND MEASUREMENTS USING RADAR TEST SET AN/UPM-137. The following tests and measurements are applicable

when using the AN/UPM-137 test set and associated test equipment. The performance tests and measurements that use the AN/UPM-98A radar test set are provided in paragraph 4-11.

WARNING

Ensure that the MASTER switch, on the C-6280 (P)/APX-72 of the AN/APM-239, is in OFF or STBY before disconnecting cable between ANT.J5 on the receiver-transmitter and RF IN/OUT on the AN/UPM-137. This will prevent damage to the transmitter.

a. preliminary Procedures. Assemble and connect the receiver-transmitter and test equipment as shown in figure 4-4. Warm-up time for the AN/UPM-137 is 15 minutes. All other test equipment should be allowed to warm up for a minimum of ten minutes before starting test procedures.

1. Test Set, Transponder, AN/APM-239 with C-6280 (P)/APX-72 inserted.

(a) Set all controls and switches of this test set to the positions identified in table 4-2, page 4-16.

2. Radar Test Set, AN/UPM-137.

(a) Set all controls and switches of this test set to the positions identified in table 4-15, page 4-48.

3. Receiver-Transmitter.

(a) Set MODE 2 code switches to 0000.

4. Electronic Counter (Hewlett-Packard 5245L or equivalent).

(a) Set POWER to ON.

(b) Set TIME BASE to 1 SECOND.

(c) Set FUNCTION switch to FREQUENCY.

b. Starting Procedures. Adjust and preset controls and switches as follows:

1. Set C-6280(P)/APX (AN/APM-239) MASTER switch to STBY and the M-1 TEST ON-OUT to ON.

NOTE

Verify that AN/APM-239 AC switched power light is illuminated.

2. Set the electronic counter SENSITIVITY (VOLTS RMS) to 10. Adjust counter sensitivity as necessary when in use.

3. AN/UPM-137

(a) Turn POWER switch to ON and allow 15 minutes warmup before performing tests.

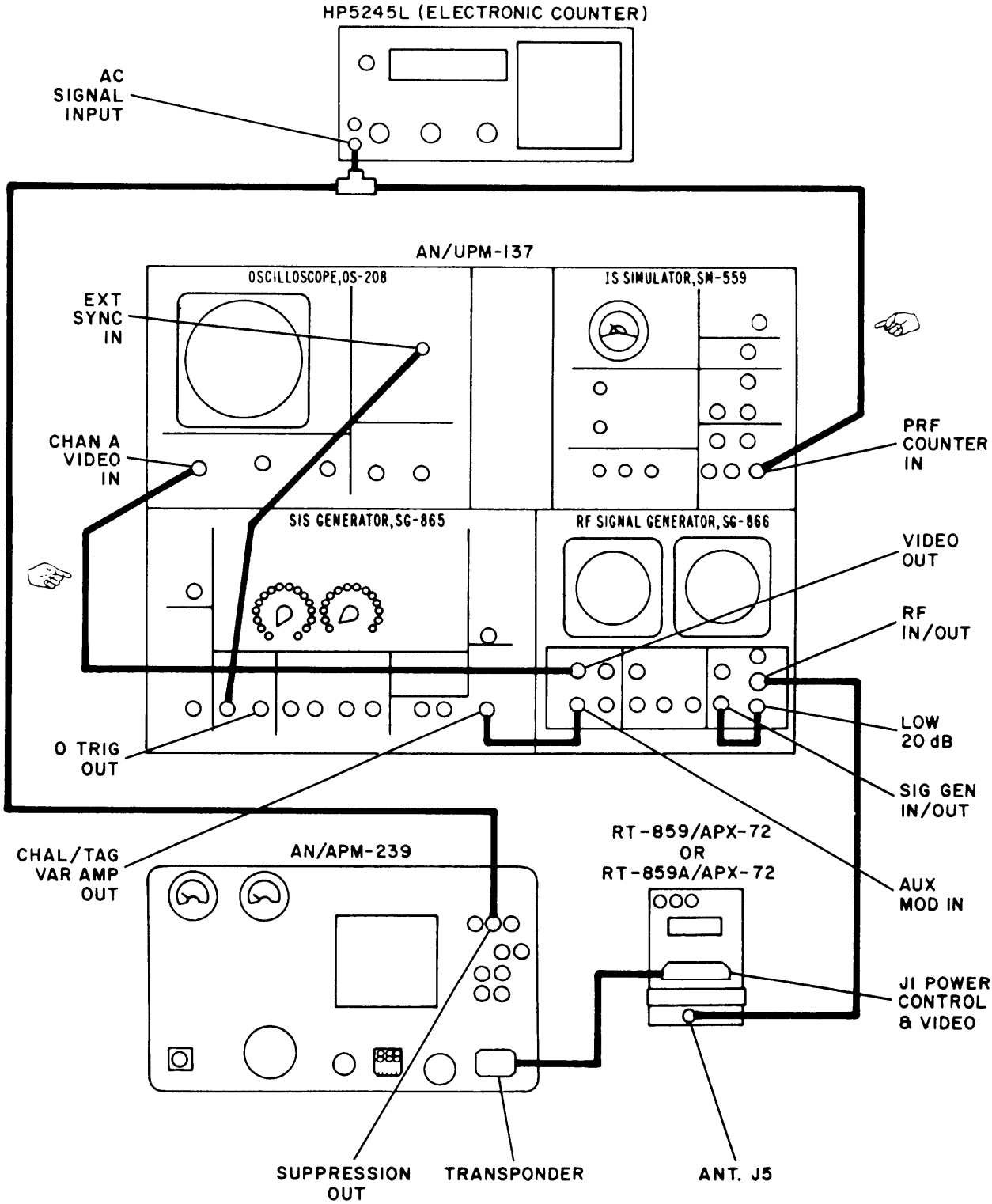
(b) Temporarily disconnect cable from electronic counter to PRF COUNTER IN. Connect cable from PRF IN to O TRIG OUT jack on the SIS Generator using a T connector.

(c) On the Interrogator Signal Simulator, assure that METER SELECT switch is set to X1000.

(d) Verify that the PRF RANGE MULT switch on the SIS generator is set to X100 and vary the PRF MULT 1–11 control to obtain a reading of 500 on the METER of the Interrogator Signal Simulator and the electronic counter.

(e) Disconnect cable from O TRIG OUT jack and reconnect to electronic counter.

(f) Adjust the OUTPUT ATTEN 0-100 dBm control for a -47 dBm challenge signal at ANT.J5 on the receiver-transmitter. (Cont on page 4-51)



Figuxe 4-4. Receiver Sensitivity/AOC Tests, Test Setup

Table 4-15. Preliminary Control Settings, Radar Test Set, AN/UPM-137

CONTROL	POSITION
POWER ON/OFF	OFF
OSCILLOSCOPE OS-208/UPM-137	
HORIZONTAL:	
SYNC Switch	EXT DC +
STABILITY Control	Fully cw
TRIG LEVEL Control	Fully cw
TIME/DIV Switch	20 USEC
TIME/DIV - VARIABLE Control	Fully cw
STROBE SELECT (CHAN A) Switch	Center position
SWEEP DELAY:	
DLY RANGE MULT Switch	OFF
MULT 1-11 Control	Fully cw
CALIBRATORS:	
AMP CAL Switch	OFF
XTAL MARK (μs) Switch	OFF
LEVEL Control	Fully ccw
VERTICAL:	
CHAN A AC/DC Switch	DC
CHAN A 75 Ω Switch	IN
CHAN A VOLT/DIV Switch	1
CHAN A VERT POSN Control	Center
CHAN B AC/DC Switch	DC
CHAN B 75 Ω Switch	OUT
CHAN B VOLTS/DIV Switch	1
CHAN B VERT POSN Control	Center
DISPLAY:	
INTENSITY Control	As required
FOCUS Control	As required
ASTIGMATISM Control	As required
HORIZ POSN Control	As required
CHAN A - ALT - CHAN B	As required

Table 4-15. Preliminary Control Settings, Radar Test Set, AN/UPM-137 (Cont)

CONTROL	POSITION
SIS GENERATOR SG-865/UPM-137	
SUPPRESSOR:	
WIDTH ADJ Control	Fully ccw
PRF:	
RANGE MULT Switch	X100
MULT 1-11 Control	Approximately 5.00
DELAY TRIG (µs):	
DLY RANGE MULT Switch	OFF
MULT 1-11 Control	Fully ccw
MIXED VIDEO:	
MIXED VID SEL Switch	TAG/RESET
VAR AMPL Control	Fully ccw
SIF DELAY (µs)	00
RESET DELAY (µs)	00
SIF 1 CODER:	
FUNCTION SEL Switch	N
WIDTH ADJ Control	N
VAR EMER SPACE Control	Fully ccw
A-B-C-D Switches	0000
SUBST PULSE POSN Control	0
SUBST PULSE SEL Switch	OFF
SIF 2 CODER:	
A-B-C-D Switches	0000
SUBST PULSE SEL Switch	OFF
SUBST PULSE POSN Control	0
TRIG DELAY Control	Fully ccw
WIDTH ADJ Control	NORM (or center position)
TRIG SEL	INT
CHAL/TAG CODER:	
MODE REPEAT Switch	1
MODE 1 Switch	ON

Table 4-15. Preliminary Control Settings, Radar Test Set, AN/UPM-137 (Cont)

CONTROL	POSITION
SIS GENERATOR SG-865/UPM-137 (Cont)	
CHAL/TAG CODER: (Cont)	
MODE 2 Switch	Off (MODE 2)
MODE 3/A Switch	Off (MODE 3/A)
MODE C Switch	Off (MODE c)
MODE 4 Switch	Off (MODE 4)
SIDE LOBE SUPPRESSION:	
SLS WIDTH Control	NORM
SLS POSN Control	NORM
CHAL/TAG RESET VIDEO:	
RESET VAR AMPL 0-5 V Control	Fully ccw
CHAL/TAG VAR AMPL 0-15 V Control	Fully ccw
CHAL/TAG Switch	SLS OUT
CHAL/TAG WIDTH Control	NORM
CHAL/TAG RESET SUBST SELECT	OFF
CHAL/TAG RESET SUBST POSITION	0
INTERROGATOR SIGNAL SIMULATOR SM-559/UPM-137	
PRF COUNTER:	
METER SELECT Switch	X1000
60 MHz SWEEP GEN:	
OUTPUT ATTEN Control	20.0
TRANSMITTER:	
XMTR FREQ Switch	XTAL
SYSTEM SIMULATOR:	
VIDEO LEVEL Control	Fully ccw
NOISE LEVEL Control	Fully ccw
SIG TGT GATE - RANGE ADJ.	Fully ccw
NORTH EXT/INTL Switch	EXT
RF SIGNAL GENERATOR SG-866/UPM-137	
AUX ATTEN +3 -60 dB Control	0
OUTPUT ATTEN 0 - 100 dBm Control	100

Table 4-15. Preliminary Control Settings, Radar Test Set, AN/UPM-137 (Cont)

CONTROL	POSITION
RF SIGNAL GENERATOR SG-866/UPM-137 (Cont)	
TRANSMITTER:	
XMTR FREQ Switch	XTAL
CW SOURCE Switch	INTL 1030 MHz

The correct setting is found using the following formula: OUTPUT ATTEN dial setting equals desired signal level at J5 (dBm) + corrected (see chart provided with AN/UPM-137) attenuation of LOW probe + cable loss (dB) (AUX ATTN dial should be set to 0). Thus for a cable loss of 1 dB, with LOW probe attenuation at 20 dB, the formula would be: OUTPUT ATTEN dial setting equals -47 dBm +20 dB +1 dB equals -26dB equals 26 dB.

(g) Adjust STABILITY control ccw until sweep stops or syncs and then adjust the TRIG LEVEL ccw until sweep starts. (This synchronizes the sweep with the "0" trigger.)

(h) Temporarily disconnect cable from AUX MOD IN of rf generator and connect to CHAN A - VIDEO IN jack on the oscilloscope. Adjust the CHAL/TAG VAR AMPL control on the SIS generator to display the challenge tags on the oscilloscope, and set their level to 5 volts. (Adjust oscilloscope display controls to obtain proper display.) Expand the display using the TIME/DIV and SWEEP DELAY controls on the oscilloscope, then set the width of the challenge tags to 0.8 microsecond by adjusting the CHAL/TAG WIDTH control on the SIS generator.

(i) Disconnect the end of the cable to the CHAN A - VIDEO IN jack and reconnect it to the AUX MOD IN jack on the rf signal generator. The PRF COUNTER should read 500 (detected challenge tags are being counted). Set AUX ATTEN +3-60 dB dial reading to -30 dB, and the PRF COUNTER should read 0.

c. Receiver Sensitivity Tests. The tests provided in table 4-16, page 4-53, are performed to determine the interrogation response using the AN/UPM-137 test set and test setup shown in figure 4-4, page 4-47. Perform the preliminary and starting procedures, page 4-46, before the performance tests.

d. Receiver Bandwidth and Center Frequency Tests. The tests provided in table 4-17, page 4-54, are performed to determine the receiver bandwidth and center frequency with interrogations in Mode 1 using the AN/UPM-137 test set and test setup shown in figure 4-5, page 4-52. Perform the preliminary and starting procedures, page 4-46, before the performance tests.

e. Transmitter Frequency and Power Measurements. The tests provided in table 4-18, page 4-56, are performed to determine the transmitter frequency and power outputs with interrogations in mode 1 using the AN/UPM-137 test set and test setup shown in figure 4-5, page 4-52. Perform the preliminary and starting procedures, page 4-46, before the performance tests.

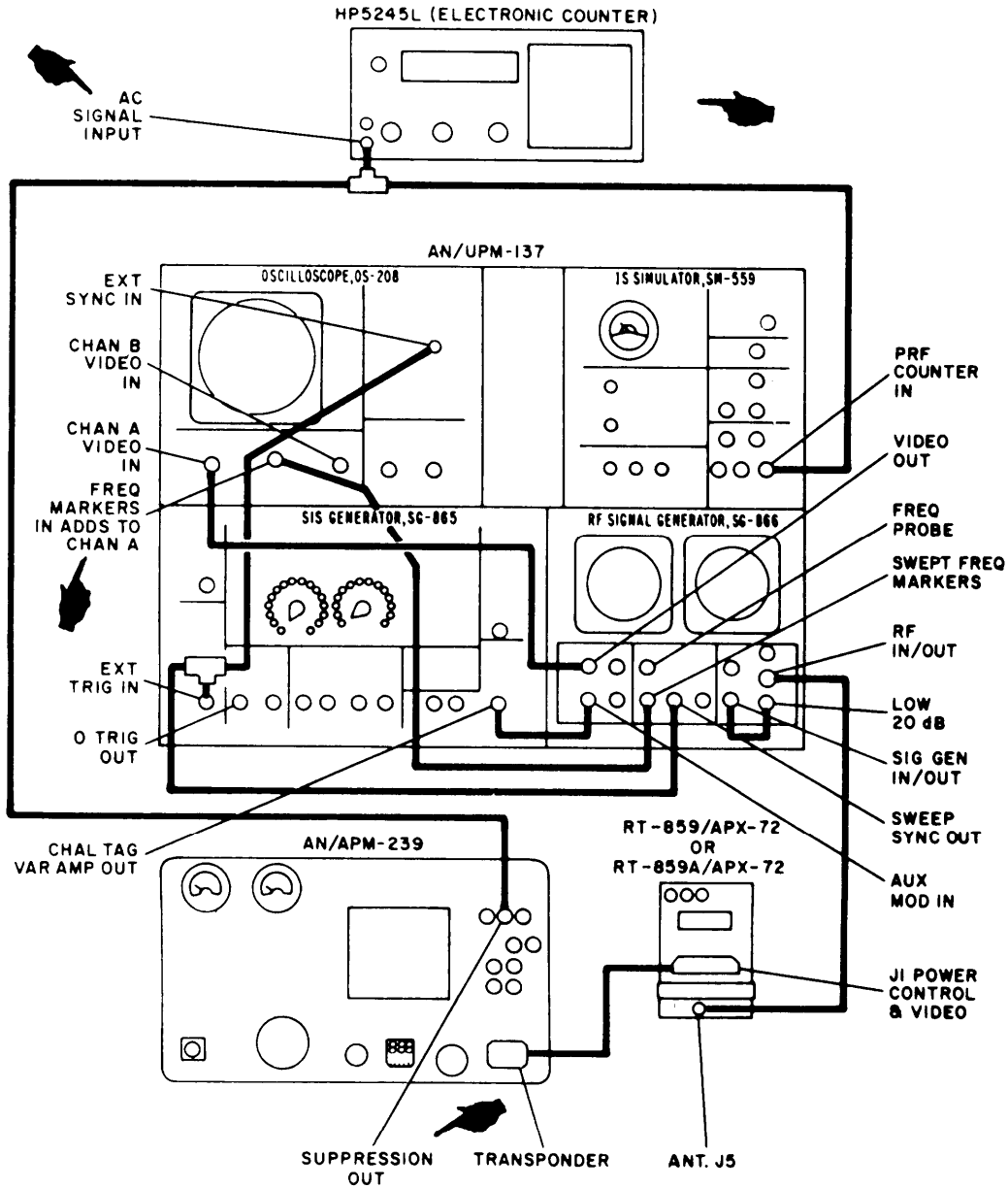


Figure 4-5. Receiver Bandwidth/Transmitter Power Tests, Test Setup

f. Automatic Overload Control (AOC) Test. The tests provided in table 4-19, page 4-59, are performed to determine reply rate limiting using the AN/UPM-137 test set and test setup shown in figure 4-4, page 4-47. Perform the preliminary and starting procedures before the performance tests, page 4-46.

g. Interrogation Side Lobe Suppression (ISLS) Tests. The test procedures provided in

(cont. on page 4-61)

Table 4-16. Receiver Sensitivity, Minimum Performance Standards Using AN/UPM-137

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Normal triggering level sensitivity	s. On AN/UPM-137 set OUTPUT ATTEN 0-100 dBm control to 100. On the C-6280(P)/APX (AN/APM-239), set the MASTER switch to NORM. Center CHAL/TAG RESET (SG-865/UPM-137) 0-15 V control. Disconnect electronic counter from PRF COUNTER IN and connect to SUPPRESSION OUT jack on AN/APM-239. Decrease OUTPUT ATTEN 0-100 dBm dial (cw) until an average of 450 replies per second (90%) are indicated on the counter.	
	b. Compute receiver minimum triggering level (MTL) for Mode 1 interrogation using the following formula: MTL(dBm) = ___ OUTPUT ATTEN dB +AUX ATTEN dB +___ cable loss dB +___ probe dB.	-77 dBm +3 with a maximum difference of 1 dBm between modes of interrogation.
	c. On the C-6280(P)/APX (AN/APM-239), set the M1-TEST/ON/OUT switch to OUT and the M2-TEST/ON/OUT switch to ON. On the SIS generator of the AN/UPM-137, set the CHAL/TAG CODER - MODE 1 switch to MODE 1 (off) and the MODE 2 switch to ON (up). Repeat the MTL measurement of step b. for MODE 2, recording the results.	-77 dBm ±3 with a maximum difference of 1 dBm between modes of interrogation.
	d. On the C-6280 (P)/APX (AN/ApM-239), set the M2-TEST/ON/OUT switch to OUT and the M3/A-TEST/ON/OUT switch to ON. On the SIS generator, set the CHAL/TAG CODER - MODE 2 switch to MODE 2 (off) and the MODE 3/A switch to ON (up). Repeat the MTL measurement of step b. for MODE 3/A and record the results.	-77 dBm ±3 with a maximum difference of 1 dBm between modes of interrogation.
	e. On the C-6280 (P)/APX (AN/APM-239), set the M3/A-TEST/ON/OUT switch to OUT and the MC-TEST/ON/OUT switch to ON. On	-77 dBm ±3 with a maximum difference of 1 dBm between

Table 4-16. Receiver Sensitivity, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Normal triggering level sensitivity (Cent)	the SIS generator, set the CHAL/TAG CODER - MODE 3/A switch to MODE 3/A (off) and the MODE M-C switch to ON (up). Repeat the MTL measurement of step b . for MODE M-C and record the results.	modes of interrogation.
	f. Verify that the MTL values obtained in steps b. through e. differ by no more than 1 dBm.	
2. Lowsensitivity	On the C-6280(P)/APX (AN/APM-239), set the MASTER switch to LOW, the MC-TEST/ON/OUT switch to OUT, and the M1-TEST/ON/OUT switch to ON. On the SIS generator, set the CHAL/TAG CODER - MODE C switch to MODE C (off) and the MODE 1 switch to ON (up). Repeat the measurements of steps l.b. thru 1.f. for low sensitivity and record the results.	-65 dBm ±2

Table 4-17. Receiver Bandwidth and Center Frequency, Minimum Performance Standards Using AN/UPM-137

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Receiver bandwidth and center frequency measurements	a. Set XMTR FREQ switch to SWEEP on the rf signal generator of the AN/UPM-137. Set the oscilloscope CHAN A/ALT/CHAN B switch to ALT, the SYNC switch to EXT DC-, and the CHAN A 75 Ω switch to OUT.	
	b. On the SIS generator of the AN\ UPM-137, set the PRF - RANGE MULT switch to EXT -. On the oscilloscope, adjust the TRIG LEVEL and STABILITY controls to synchronize the sweep with the sweep sync trigger. Vary the TIME/DIV VAR and DLY RANGE MULT controls to display one complete set of frequency markers on the oscilloscope. Set the AUX ATTEN +3 -60 dB dial to 0.	

Table 4-17. Receiver Bandwidth and Center Frequency, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Receiver bandwidth and center frequency measurements (Cont)	c. On the SIS generator? set the DELAY TRIG-DLY RANGE MULT switch to X400 and increase the challenge tag delay with the MULT 1-11 control (turn CW) until the mode 1 interrogation train (Channel A) is aligned with the 1030 MHz marker. (See figure 4-6, page 4-60, view A.) (Set the CHAN A VOLTS/DIV switch to conveniently view the interrogation pulses.) 1. Expand the display using the TIM/DIV and SWEEP DELAY controls until each centimeter on the horizontal scale represents 1 MHz with the -5 MHz frequency marker aligned with the leftmost graticule on the oscilloscope display. (See figure 4-6, page 4-60, view B.) 2. Refine the alignment of the interrogation with the 1030 MHz marker. d. Read the sweep frequency prf rate on the PRF COUNTER (250 nominal) . Multiply reading by 90% for reply rate. 1. Vary the OUTPUT ATTEN 0-100 dBm dial (CW) until the PRF COUNTER-METER reads the 90% reply rate noted above and note the level indicated by the OUTPUT ATTEN 0-100 dBm dial. 2. Decrease the attenuation of the OUTPUT ATTEN 0-100 dBm dial by 6 dB. Vary the DELAY TRIG-MULT 1-11 control to move the interrogation pulse to the points on each side of the 1030 MHz marker where the PRF COUNTER METER indicates a 90% reply rate. (Adjust the SWEEP DELAY - MULT 1-11	

Table 4-17. Receiver Bandwidth and Center Frequency, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Receiver bandwidth and center frequency measurements (Cont)	control and the TIME/DIV control, if necessary.) These two points are the high (FH6) and low (FL6) frequency points of the 6 dB receiver bandwidth.	
	e. Compute and record the 6 dB receiver bandwidth using the following formula: 6 dB bandwidth = FH6 - FL6	7.0 MHz minimum
	f. Compute and record the receiver frequency using the following formula: center freq = $\frac{FH6 - FL6}{2}$ + FL6	1030 ±1.5 MHz

Table 4-18. Transmitter Frequency and Power, Minimum Performance Standards Using AN/UPS-137

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Transmitter frequency output	a. Remove cable from VIDEO OUT of rf signal generator and connect it to FREQ PROBE of rf generator. Set XMTR FREQ switch to SWEEP on the rf signal generator of the AN/UPM-137. Set the oscilloscope CHAN A/ALT/CHAN B switch to CHAN A, the SYNC switch to EXT DC-, and the CHAN A 75 0 switch to OUT. Set VOLTS/DIV control of Channel A to .5.	
	b. On the SIS generator of the AN/UPM-137, set the PRF – RANGE MULT switch to EXT -. Using the TRIG LEVEL and STABILITY controls on the oscilloscope, synchronize the sweep with the SWEEP SYNC OUT trigger. Vary the TIME/DIV, DLY RANGE MULT, and VAR controls to display one full set of frequency markers on the Channel A Sweep. (See figure	

Table 4-18. Transmitter Frequency and Power, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Transmitter frequency output (Cent)	4-6, view A.) Set the C–6280 (P)/APX (AN/APM-239) MASTER switch to NORM.	
	c. On the SIS generator, set the DELAY TRIG - DLY RANGE MULT switch to X400. Adjust (lower) the OUTPUT ATTEN 0-100 DBM dial to approximately -10 dBm to view replies, then increase the DELAY TRIG MULT 1-11 control setting until the transponder replies become visible on the Channel A sweep. (See figure 4-6, view A.)	
	1. Vary the MULT 1-11 control further until the replay peaks in amplitude. (Adjust VOLT/DIV controls as required.) Now ex–pand and delay the sweep with the TIME/DIV, VAR, and SWEEP DELAY controls until each centimeter on the horizontal scale corresponds to 1 MHz, with the -5 MHz marker on the left-most vertical display graticule. (See figure 4-6, view B.)	
	2. Refine the amplitude peaking by peaking just the F_1 pulse to maximum amplitude. Adjust OUTPUT ATTEN 0-100 dBm dial for convenient level, taking care not to exceed saturation level of demodulator.	
	d. Interpolate and record the fre-quency at which the F1 pulse is peaked as transmitter frequency.	1090 ±3.0 MHz
2. Transmitter power mea-surement	a. Set all controls on AN/UPM-137 as listed in table 4–15, page 4-48 except for CHAL/TAG RESET VIDEO WIDTH Set to 0.8 micro-seconds and CHAL/TAG RESET VAR AMPL 0-15V, centered. Set XMTR FREQ switch to XTAL on the rf signal generator of the	

Table 4-18. Transmitter Frequency and Power, Minimum Performance Standards Using AN/UPM-137 (Cont)

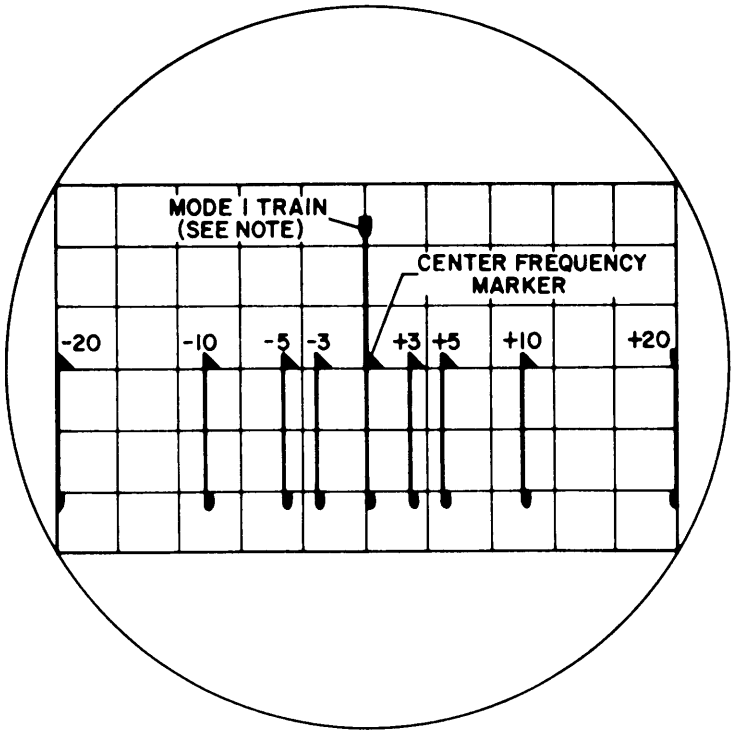
STEP	PROCEDURE	PERFORMANCE STANDARD
2. Transmitter power measurement (Cont)	AN/UPM-137. On the SIS generator, set the CHAL/TAG CODER - MODE 1 switch to MODE 1 (off) and the MODE 3/A switch to ON (up). On the C-6280 (P)/APX (AN/APM-239) , set the Ml - TEST/ ON/OUT switch to OUT, the M-3/A TEST/ON/OUT switch to ON, the MODE 31A code switches to 7777. b. Set the MASTER switch on the C-6280(P)/APX control to NORMAL. Disconnect cable between SWEEP SYNC OUT of rf generator and EXT TRIG IN of SIS generator. Remove cable connector from EXT TRIG IN and connect to O TRIG OUT on SIS generator. Disconnect cable connector from FREQ PROBE and connect it to VIDEO OUT using a "T" connector (other end of this cable should be connected to CHAN A VIDEO IN). Set AUX ATTEN to 20 dBm. 1. Set the oscilloscope TIME/DIV control to 5 USEC and VOLTS/ DIV of Channel A to . 2. Synchronize the oscilloscope sweep to the 0 TRIG OUT. The detected interrogator pulses should appear on oscilloscope. 2. Decrease attenuation of the OUTPUT ATTEN 0-100 dBm control (turn cw) until the transponder begins to reply to the interrogations. (Replies will appear on oscilloscope after the P3 challenge pulse.) c. Adjust the TIME/DIV and SWEEP DELAY controls to display the F_1 pulse of the reply train. Adjust the OUTPUT ATTEN 0-100 dBm dial until the detected F pulse is at the level given by the DEMODULATOR CALIBRATION CHART for the AN/ UPM-137. Read the OUTPUT ATTEN dial setting and the cable loss	

Table 4-18. Transmitter Frequency and Power, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
2. Transmitter power measurement (Cont)	as labeled on the rf cable from the RF IN/OUT jack to the ANT jack on the transponder.	
	d. Using the formula given on the DEMODULATOR CALIBRATION CHART, compute and record the power level of the F_1 pulse.	F_1 = +57 ±3 dBm
	e. Repeat the preceding measurement for the F_2 pulse and record the power level.	$F_2 = F_1 \pm 1$ dBm

Table 4-19. Automatic Overload Control, Minimum Performance Standards Using AN/UPM-137

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Reply rate limiting	a. Set AUX ATTEN +3 -60 dB control on the RF signal generator to -30. Set the C-6280(P)/APX (AN/APM-239) M1-TEST/ON/OUT switch to OUT, and the M2-TEST/ON/OUT switch to ON. On the SIS generator, set the CHAL/TAG CODER - MODE 1 switch to MODE 1 (off) and the MODE 2 switch to ON (up).	
	D. Set the C-6280(P)/APX MASTER switch to NORM. Connect counter to SUPPRESSION OUT jack on AN/APM-239. Vary the OUTPUT ATTEN 0-100 dBm dial until the electronic counter reads an average 450 (90% replies), then increase the signal level by 3 dB.	Rate 1200 ±100 replies per second.
	1. Set the MODE 2 code switches to 7777 on the receiver-transmitter and observe a reading of 500 on the electronic counter. Set the METER SELECT switch to X10,000.	
	2. Increase the PRF - MULT 1-11 control (and the RANGE MULT control) until the electronic counter indication no longer increases at which point AOC action begins. Record the electronic counter indication at this point.	



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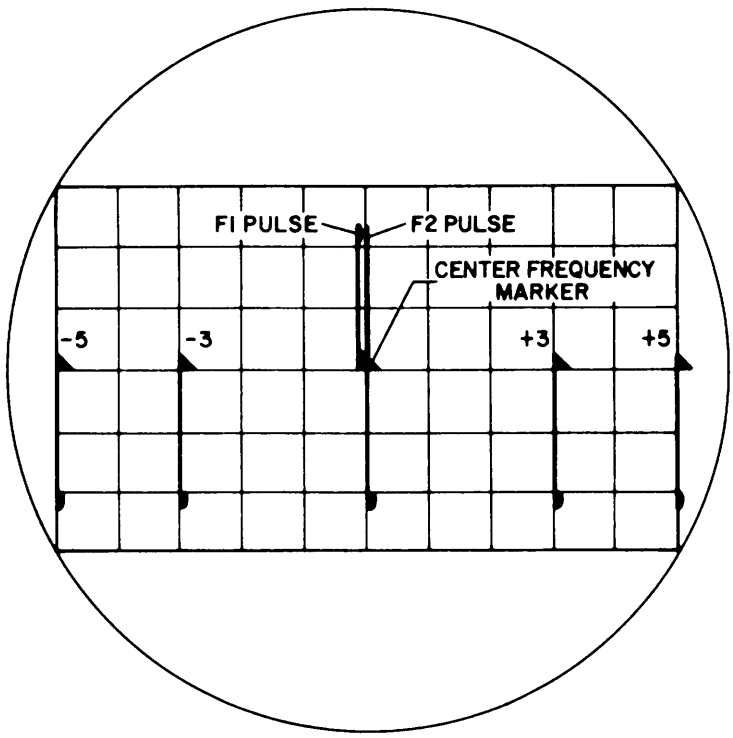


B

NOTE : THESE PULSES ARE INTERROGATION PULSES DURING RECEIVER BANDWIDTH TESTS (CENTER MARKER : 1030 MHz). THEY ARE DETECTED TRANSMITTED REPLIES DURING TRANSMITTER FREQUENCY TESTS (CENTER MARKER : 1090 MHz).

Figure 4-6. Swept Frequency Marker Deviation Presentations

table 4-20, page 4-66, are performed to determine that the side lobe detection, and decoding circuits are within minimum performance standards. These tests are made using the AN/UPM-137 test set and test setup of figure 4-7, page 4-62. Perform the preliminary and starting procedures, page 4-46, before the performance tests.

h. Suppression Tests. The test procedures provided in table 4-21, page 4-67 are performed to determine that the receiver-transmitter is generating an external pulse to suppress operation of external equipment and an internal suppression pulse to suppress internal functions during certain modes of operation. These tests are made using the AN/UPM-137 test set and the test setup of figure 4-8, page 4-63. Perform the preliminary and starting procedures, on page 4-46, before the performance tests.

i. Mode 1, 2, 3/A, Test, and C Reply Tests (Using the AN/UPM-137 Test Set). These tests determine that the reply pulse trains are spaced within the required performance standards. Pulse spacing tests require the use of 1.45 μs markers to examine the reply pulse spacing. Perform the preliminary and starting procedures, page 4-46, before the procedures of table 4-22, page 4-70. Set up the test equipment as shown in figure 4-9, page 4-64, before doing the performance tests.

j. Mode 4 Reply Tests (Using AN/UPM-137 Test Set). These tests determine that mode 4 circuitry is functioning within the minimum performance standards. The AN/APM-245 Test Set Simulator is required to modulate the AN/UPM-137 for mode 4 interrogation, and to provide the mode 4 reply through the AN/APM-239. Tests are conducted with the receiver-transmitter and test equipment assembled and connected as shown in figure 4-10. Connect equipment and perform preliminary procedures as follows preparatory to the procedures of table 4-23.

1. Test Set, Transponder AN/APM-239.

(a) Connect PWR INPUT to the 115 vac, 400 Hz voltage source.

(b) Terminate AUDIO COMMON with shorting cap.

(c) Terminate REPLY with a 50-ohm termination.

(d) Set all controls and switches as directed in table 4-2.

2. Test Set, Simulator AN/APM-245.

(a) Connect TEST WORD TO CHAN A VIDEO IN on AN/UPM-137 oscilloscope.

(b) Connect INT TRIG to EXT TRIG IN on the AN/UPM-137 SIS generator.

(c) Set all controls and switches as directed in table 4-13, except set PRF SEL to INT-MED.

3. Test Set, Radar AN\UPM-137.

(a) Connect power cord to 115 vac, 60 Hz source.

(b) Set Channel A and B 75 Ω switches of oscilloscope to OUT.

(c) Place caps on all unused jacks of rf signal generator.

(d) Set all controls and switches as directed in table 4-15, except set the PRF RANGE MULT switch on the S1S generator to EXT +.

4. Electronic Counter (Hewlett-Packard 5245L or equivalent).

(a) Connect power cord to the 115 vat, 60 Hz voltage source.

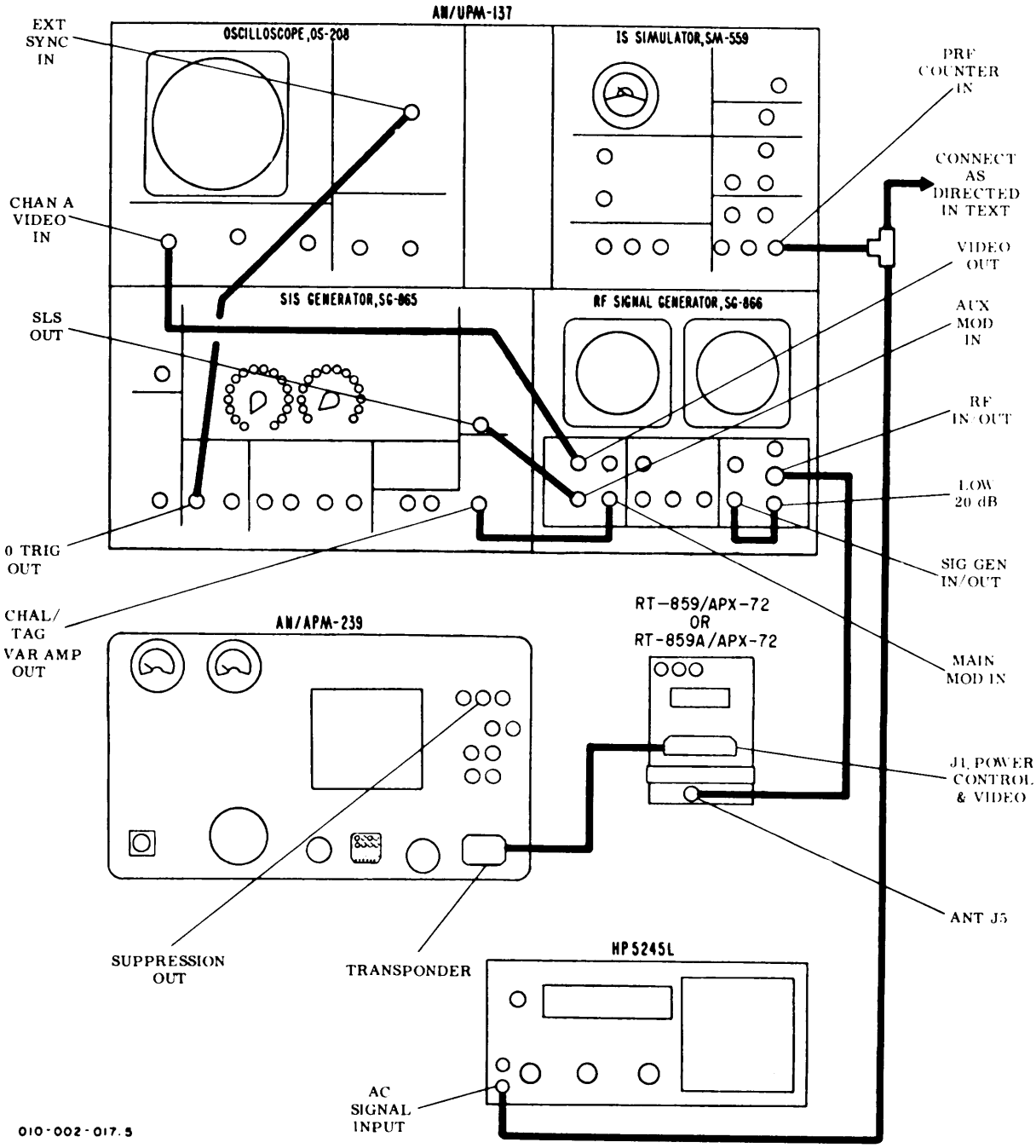


Figure 4-7. ISLS Tests, Test Setup

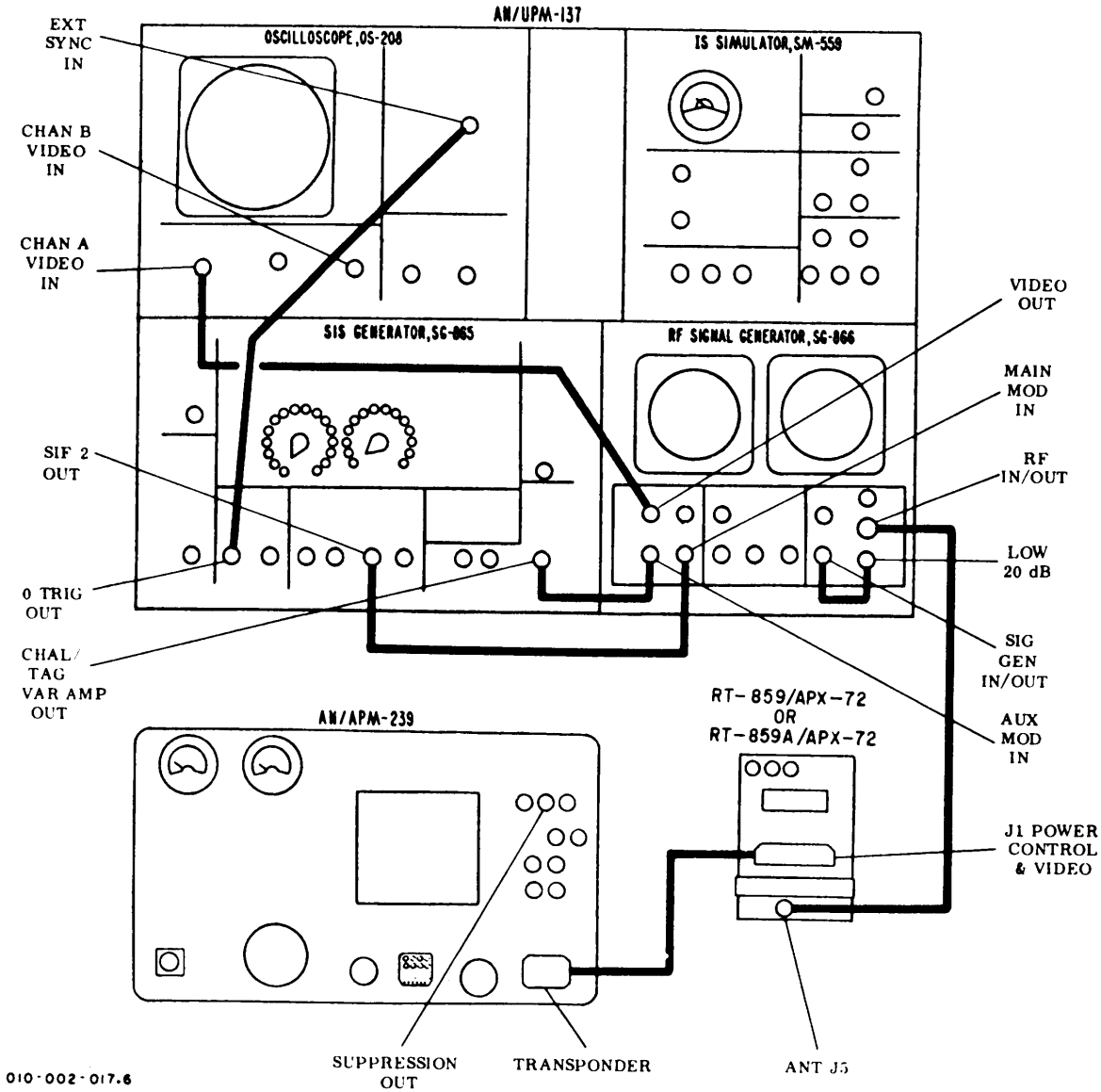


Figure 4-8. Suppression Tests, Test Setup

(b) Connect AC SIGNAL INPUT of counter to 0 TRIG OUT on AN/UPM-137 using a "T" connector.

(c) Set TIME BASE to 1 SEC.

(d) Set FUNCTION switch to FREQUENCY.

(e) Set POWER ON.

5. Preliminary Procedures. Perform the following procedures before doing the mode 4 tests of table 4-23.

(a) Momentarily hold METER SCALE switch of AN/APM-245 in the X1 position and adjust INT PRF FREQ ADJ control for a reading of 0.5 kHz on the PRF meter.

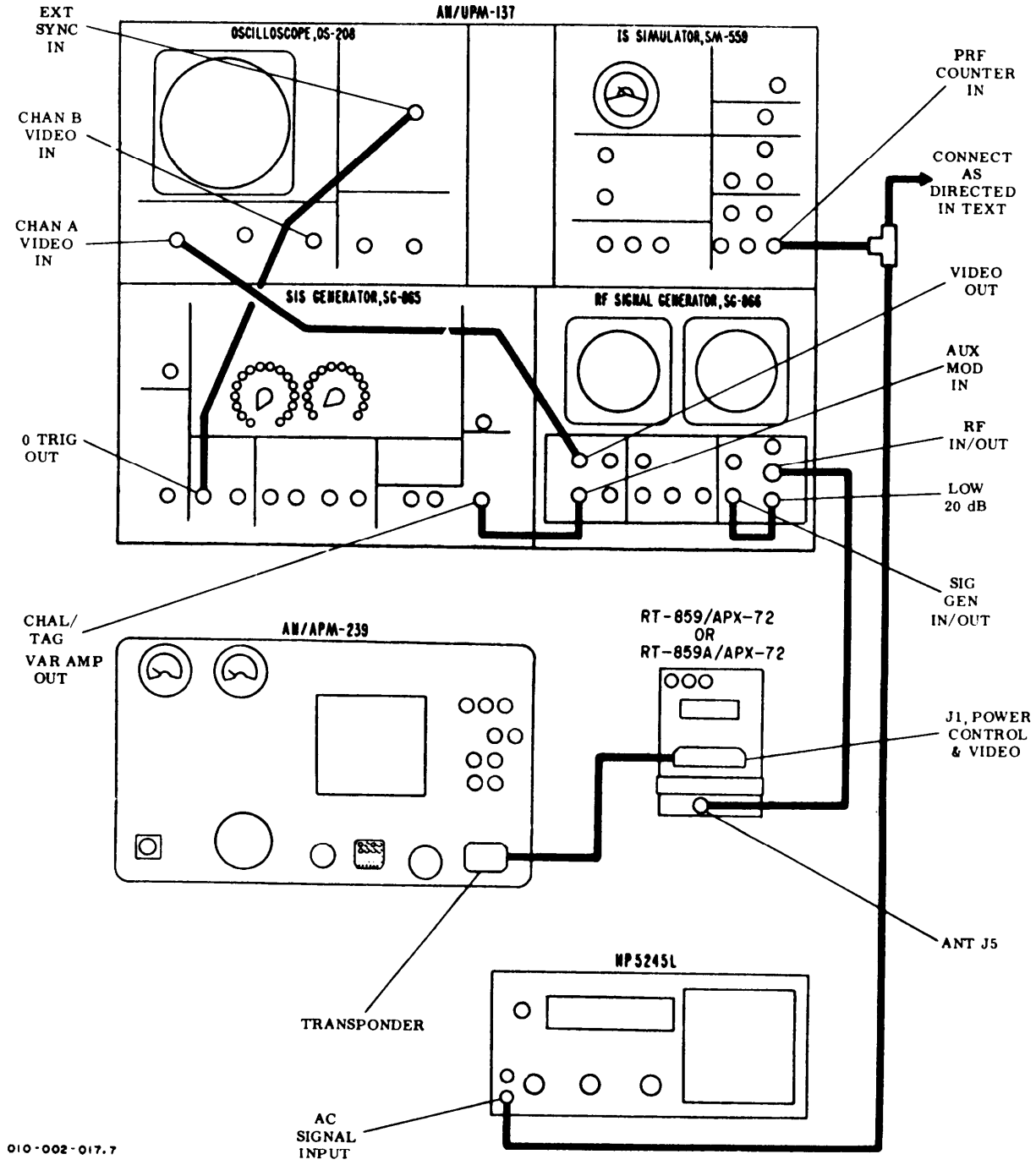


Figure 4-9. Modes 1, 2, 3/A, Test, and C Replies Tests, Test Setup

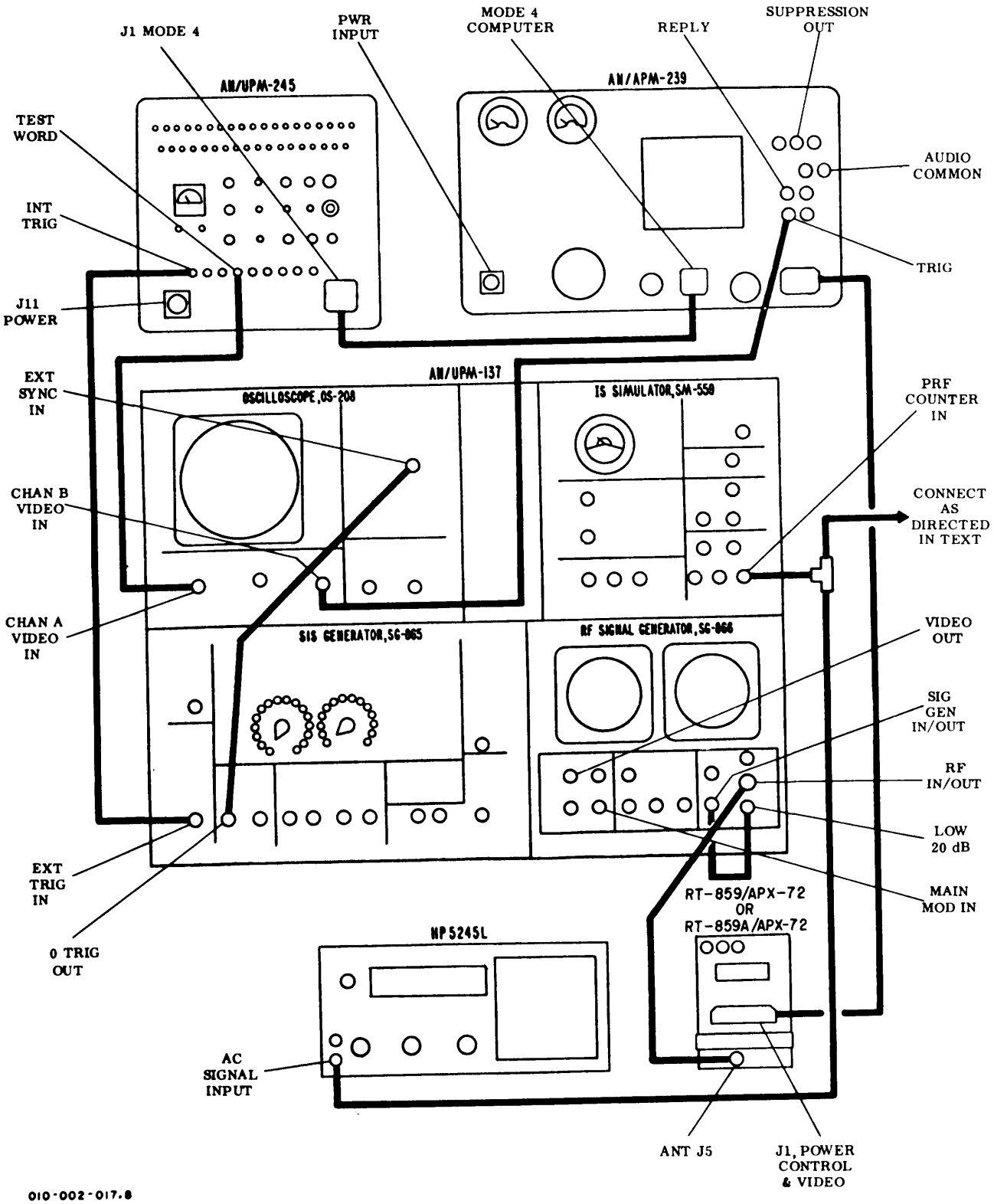


Figure 4-10. Mode 4 Tests, Test Setup

Table 4-20. Interrogation Side Lobe Suppression, Minimum Performance-Standards Using AN/UPM-137

STEP	PROCEDURE	PERFORMANCE STANDARD
1. ISLS operation	a. Set the C-6280(P)/APX (AN/APM-239) MASTER switch to STBY and the TEST M-2 OUT switch to ON. On the AN/UPM-137, set the CHAL TAG/CODER MODE 2 switch to ON (up) and the MODE 1 switch to MODE 1 (off). On the AN/UPM-137 oscilloscope, set the CHAN A/ALT/CHAN B switch to CHAN A and the CHAN A 75 Ω switch to IN. 1. Check to assure that the CHAL/TAG SLS-A/B DISPARITY switch on the SIS Generator is set to SLS OUT. Adjust the oscilloscope TRIG LEVEL and STABILITY controls to synchronize the Channel A sweep with the O TRIG output. Adjust the CHAN A VOLTS/DIV switch, and the TIME/DIV and SWEEP DELAY controls, to display the detected MODE 2 challenge pulses. 2. Verify that the P1 and P3 pulse widths are set to 0.8 ±0.1 microsecond (adjust with the CHAL/TAG WIDTH control) , and set the P2 pulse width to 0.8 ±0.1 microsecond using the SLS WIDTH control. Adjust the AUX ATTEN +3 -60 dB dial so that the P2 pulse and the P1 pulse are the same amplitude. b. Connect the electronic counter to the O TRIG OUT jack on the SIS generator. Make connection at "T" connector on PRF COUNTER IN. Adjust PRF MULT 1-11 control to obtain a reading of 500 ±3 on the counter. Disconnect the cable from O TRIG OUT jack and connect to SUPPRESSION OUT jack on the AN/UPM-239. Temporarily disconnect cable from AUX MOD IN jack on the RF signal generator. c. Adjust OUTPUT ATTEN 0-100 dBm dial on AN/UPM-137 to obtain an	

Table 4-20. Interrogation Side Lobe Suppression, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. ISLS operation (Cont)	average count of 450 suppressions on counter. Note indicator on OUTPUT ATTEN dial; this is reference MTL for this procedure. NOTE In following procedure, allow sufficient time (one sampling period) for the electronic counter to respond to selected values within the attenuation range.	
	d. Reconnect the cable to AUX MOD IN and observe counter for 0 to a maximum of 5 suppressions while interrogating the receiver-transmitter over an attenuation range 3 dB to 50 dB lower than OUTPUT ATTEN indication defined as reference MTL.	0 to 5 (maximum) replies on counter.
2. ISLS 9 dB below interrogation	Increase the AUX ATTEN attenuation by 9 dB. Observe counter for a minimum of 495 replies averaged over a ten-second interval while interrogating the receiver-transmitter over an attenuation range 3 dB to 50 dB lower than OUTPUT ATTEN indication defined as reference MTL.	Read 495 suppressions minimum on counter averaged over a ten-second interval.

Table 4-21. Suppression, Minimum Performance Standards Using AN/UPM-137

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Internal suppression	a. Set the SIS generator - MIXED VID SEL switch to ALL SIF, the CHAL/TAG CODER - MODE 1 switch to MODE 1 (off), and the MODE 2 switch to ON (up), the SIF 2 CODER - SUBST PULSE SEL switch to C2, the SIF 2 - ABCD switches to 0020, and the oscilloscope CHAN B 75 Ω switch to IN. Set the C-6280(P)/	

Table 4-21. Suppression, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Internal suppression (Cont)	APX (AN/APM-239) M1 - TEST/ON OUT switch to OUT and the M2 - TEST/ON/OUT switch to ON, and the MASTER switch to NORM. b. Temporarily disconnect the cable to the MAIN MOD IN jack on the rf signal generator of the AN/UPM-137 and connect it to the CHAIN B VIDEO IN jack on the oscilloscope. Set the CHAN A/ALT/CIIAN B switch to CHAN B, and adjust the TRIG LEVEL and STABILITY controls to synchronize the sweeps. Adjust the TIME/DIV and SWEEP DELAY controls to display the SIF 2 train. 1. Adjust the SIF 2 - CODER - WIDTH ADJ to set the pulse width of the pulses in the train to 0.8 µs. Also, adjust the SIF 2 CODER - SUBST PULSE POSN control to space the C2 pulse 5.0 µs (leading edge-to-leading edge) after the F_1 pulse of the SIF 2 train. (The first two pulses of the train will be used as a MODE 2 interrogation, with the F_2 pulse present, but not used). 2. Remove the cable from the CHAN B VIDEO IN jack and reconnect it to the MAIN MOD IN jack. Set the CHAN A/ALT/CHAN B switch to CHAN A. c. Set the oscilloscope TIME/DIV control to 20 USEC and the DLY RANGE MULT to OFF. Adjust the OUTPUT ATTEN 0-100 dBm dial to display the MODE 2 reply. Increase the SIS generator SIF DELAY control (CW) until the second set of replies just appear on the display. Vary the oscilloscope SWEEP DELAY controls to position the	

Table 4-21. Suppression, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Internal suppression (Cont)	leading edge of the F_2 pulse of the first reply train to the first vertical line of the grid of the display.	
	d. Measure and record the time delay between the first vertical line on the display and the leading edge of the F_1 pulse (F_1 of SIF 2 train) of the second interrogation.	75-100 µs
2. External suppression	a. Connect SUPPRESSION OUT jack of AN/APM-239 test set to the CHAN B VIDEO IN jack on the AN/UPM-137 oscilloscope. Set the CHAN A/ALT/CHAN B switch to CHAN B. Adjust the oscilloscope TIME\DIV and SWEEP DELAY controls to display the suppression pulse on the display. Measure and record pulse amplitude and set oscilloscope CHAN B 75 Ω switch to OUT.	18 volts minimum
	b. Disconnect the cable from the SIS generator - SIF 2 jack. Set the oscilloscope CHAN A/ ALT/CHAN B switch to ALT. If necessary, decrease the OUTPUT ATTEN setting to display the reply pulses and increase the AUX ATTEN setting by the same amount.	Verify and record that the suppression pulse (Channel B) reaches a minimum of 18 volts by the time F_1 (Channel A) reaches 10% of its amplitude and remains at 18 volts or greater until the F_2 pulse has decayed to the 10% level, and that the suppression level is less than 5 volts, 5 µs after the F_2 pulse decays to the 10% level.

Table 4-21. Suppression, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
2. External suppression (Cont)	1. Connect cable from suppressor out jack on SIG generator to suppression in jack on AN/APM-239. Slowly increase suppressor width control from its extreme CCW position to CW.	Verify that the reply train is suppressed.
	2. Turn width control to max CCW	Verify that pulse reply trains reappear.

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-137

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Frame spacing	a. On AN/UPM-137 check the OUTPUT ATTEN 0-10.0 dBm control for a setting of -47 dBm. Set the AUX ATTEN +3 -60 dB control to 0. On the C-6280(P)/APX (AN/APM-239), set the MASTER switch to NORM and the M1-TEST/ON/OUT switch to ON and check that the M2-TEST/ON/OUT switch is OUT.	
	1. Connect the PRF COUNTER IN jack to electronic counter (HP5245L) and to the AN/APM-239 SUPPRESSION OUT (using a "T" connector). The PRF COUNTER METER should indicate 500 (the electronic counter should indicate 500) (detected challenge tags are being counted). Set AUX ATTEN +3 -60 dB dial reading to -30 dB, and the counters should read 0.	
	2. Decrease OUTPUT ATTEN 0-100 dBm dial (CW) until 450 replies per second (90%) are	

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Frame spacing	indicated on the PRF COUNTER METER. Observe the dial setting for reference MTL. Set the OUTPUT ATTEN 0-100 dBm dial 3 dB lower than this dial setting. b. On the AN/UPM-137 oscilloscope, set the CHAN A/ALT/CHAN B switch to ALT, and the XTAL MARK (USEC) switch to 1.45. Set the C-6280 (P)/APX 141-TEST/ON/OUT switch to OUT and the M2-TEST/ON/OUT switch to ON. On the SIS generator, set the CHAL/TAG CODER MODE 1 switch to MODE 1 (off), and the M0DE 2 switch to ON (up). c. Adjust the oscilloscope TRIG LEVEL and STABILITY controls to synchronize the oscilloscope sweeps with the O TRIG output. Adjust the XTAL MARK - LEVEL control to conveniently display the 1.45 µs crystal markers on the Channel B sweep (approxi mately one-cm amplitude) 1. Adjust the TIME/DIV switch and the SWEEP DELAY controls to display the transponder reply (F_1 and F_2 pulses) on the Channel A sweep. Vary the OUTPUT ATTEN 0-100 dBm dial as required (readjust AUX ATTEN +3 -60 d3 dial in opposite direction to correspond with OUTPUT ATTEN dial change) 2. Expand and delay sweep using the TIME/DIV, VARIABLE, and SWEEP DELAY controls until the F_1 pulse is at the left end of the Channel A sweep, and the F_2 pulse is at the right end of the sweep. 3. Vary the SWEEP DELAY - MULT 1-11 control (XTAL MARK POSN control of AN/UPM-137A) and the	

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minumum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Frame spacing (Cont)	VERT POSN controls (for Channel B) to align the leading edge of a 1.45 µs crystal marker with the leading edge of the F_2 pulse, keeping both pulses (F_1,F_2) on the display. Select CHAN A, CHAN B, and ALT positions of oscilloscope to conveniently display these pulses. This alignment must be done as precisely as possible.	
	4. Measure and note the bracket spacing (T) to 1.45 µs accuracy by counting the number of 1.45 µs markers between the F_1 and F_2 pulse (do not count marker nearest F_1 and multiplying by 1.45. Expand the sweep by setting the TIME/DIV control to .1 USEC, and the VARIABLE control to CAL (fully Cw).	
	5. Measure and note the spacing (t) between the peak of the crystal marker nearest F_1 and the 50% point on the leading edge of F_1.	
	d. Compute and record bracket spacing using the formula Bracket Spacing = T - t if the crystal marker nearest F_1 is to the left of F_1; the formula Bracket Spacing = T + t if the crystal marker nearest F_1 is to the right of F_1.	20.3 ±0.05 µs
	e. Set MODE 2 code switches on receiver-transmitter to 0007, repeat the measurement of step C, verify correct spacing, and record results.	20.3 ±0.05 µs

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFOMANCE STANDARD
1. Frame spacing (Cont)	f. Set C-6280(P)/APX (AN/APM-239) IDENT-MIC switch to IDENT and release. View I/P reply (following F_2 pulse) on oscilloscope for timing duration of appearance.	15 to 30 seconds
	g. Referring to step l.d., align F_1 pulse with a marker. Count to 18th marker (include first marker in count) and initiate I/P as above. Pulse F_3 should be aligned with 18th marker.	24.65 ±0.05 µs
	h. Increase the PRF to assure that PRF COUNTER METER indicates a PRF of 1000.	
2. Pulse width	On the AN/UPM-137 oscilloscope, measure width of F_1 pulse at the 50% amplitude point.	0.45 ±0.1 µs
3. Rise time	On AN/UPM-137 oscilloscope, set SYNC switch to INTL +, CHAN A 75 Ω switch to IN, and readjust HORIZONTAL controls as required. Observe and measure rise time of F_1 pulse. Measure from 10% to 90% amplitude points on leading edge of pulse. Amplitude of P1 pulse may be varied, as required, using OUTPUT ATTEN 0-100 dBm dial.	0.05 to 0.1 µs
4. Fall time	On the AN/UPM-l37 oscilloscope, observe and measure fall time of F_1 pulse. Measure from 90% amplitude point to 10% amplitude point on trailing edge of pulse. Set SYNC switch to EXT DC + and adjust HORIZONTAL controls as required.	0.05 to 0.2 µs
	NOTE Decrease the PRF to 500.	
5. Mode 2 replies	a. On the receiver-transmitter, rotate MODE 2 code select dials in sequence and observe appearance of proper code pulses	Verify F_1, C_1, A_1, C_2, A_2; C_4, A_4, B_1, D_1, B_2, D_2, B_4, D_4, and

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
5. Mode 2 replies (Cont)	on the AN/UPM-137 oscilloscope with each change.	F_2 pulses appear in proper sequence (See figure 2-5.)
	b. On AN/APM-239, place SPECIAL in X PULSE and observe that X pulse appears in proper location in reply train. Return SPECIAL to CAUTION LIGHT RESET.	(See figure 2-6.)
	c. Set C-6280 (P)\APX MASTER switch to STBY.	Verify reply pulses not present.
	d. Set C-6280(P)/APX MASTER switch to NORM, M2-TEST/ON/OUT switch to OUT.	Verify reply pulses not present.
	NOTE During the testing of each mode, make sure all other modes are set to the ON position on the C-6280(P)/APX Panel and all other mode codes are maximized. At the beginning of each mode check, set the selected mode code to 0000 and verify that only the frame pulses are present.	
6. Mode 1 replies	a. On the AN/UPM-137, set the CHAL/TAG/CODER MODE 2 switch to MODE 2 (off) and the MODE 1 switch to ON (up). On C-6280(P)/APX, set M1-TEST/ON/OUT switch to ON and rotate MODE 1 code select dials in sequence observing appearance of proper code pulses with each change on the AN/UPM-137 oscilloscope.	Verify that F_1, A_1, A_2, A_4, B_1, B_2, and F_2 pulses appear in proper sequence. (See figure 2-5.)
	b. On AN/APM-239, place SPECIAL in X PULSE and observe that X pulse appears in proper location in	(See figure 2-6.)

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
6. Mode 1 replies (Cont)		reply train. Return SPECIAL to CAUTION LIGHT RESET.	
	c.	Set the oscilloscope TIME/DIV control to observe one reply train on left half of the oscilloscope display (TIME/DIV control to 5 µSEC) . Set C-6280 (P)/APX MODE 1 CODE to 73, IDENT-MIC to IDENT and release.	Verify that two reply pulse trains are present for a period of 15 to 30 seconds. (See figure 2-6.)
	d.	Set C-6280(P)/APX MASTER switch to EMER.	Verify one normal reply pulse train and three sets of framing pulses are present. (See figure 2-6.)
	e.	Set C-6280(P)/APX MASTER switch to NORM, M1-TEST/ON/OUT switch to OUT.	Verify reply pulses not present.
		NOTE During the testing of each mode, make sure all other modes are set to the ON position on the C-6280(P)/APX Panel and all other mode codes are maximized. At the beginning of each mode check , set the selected mode code to 0000 and verify that only the frame pulses are present.	
7. Mode 3/A replies	2.	On the AN/UPM-137, set the CHAL/TAG CODER MODE 1 switch to MODE 1 (off) and the MODE 3/A switch to ON (up) and TIME/DIV control to 2 µSEC. On C-6280(P)/APX, set M3-TEST/ON/OUT switch to ON and rotate MODE 3/A code select dials in sequence observing appearance of, proper code pulses with each change on AN/UPM-137 oscilloscope.	Verify $F_1, C_1, A_1, C_2, A_2, C_4, A_4, B_1, D_1, E_2, D_2, B_4, C_4$, and F_2 pulses appear in proper sequence. (See figure 2-5.)

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
7. Mode 3/A replies (Cont)	b. On AN/APM-239, place SPECIAL in X PULSE and observe that X pulse appears in proper location in reply train. Return SPECIAL to CAUTION LIGHT RESET. NOTE On AN\UPM-239A, return SPECIAL to OFF.	(See figure 2-6.)
	c. Adjust the TIME/DIV control of oscilloscope to 5 µSEC. Set C-6280(P)/APX MODE 3/A CODE to 7777, IDENT-MIC to IDENT and release.	Verify that a normal reply pulse train and an F_3 pulse are present. (See figure 2-6.)
	d. Set C-6280(P)/APX MASTER switch to EMER.	Verify that F_1 A_1, A_2, A_4, B_1, B_2, B_4, F_2, F_3, F_4, F_5, F_6, F_7, and F_8 only are present. (See figure 2-6.)
	e. Set C-6280(P)/APX MASTER switch to NORM, M3-TEST/ON\OUT switch to OUT. Set the XTAL MARK (pSEC) switch of oscilloscope to OFF. NOTE During the testing of each mode, make sure all other modes are set to the ON position on the C-6280 (P)/APX Panel and all other mode codes are maximized. At the beginning of each mode check, set the selected mode code to 0000 and verify that only the frame pulses are present.	

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
8. Test mode replies	a. Set the CHAN B 75 Ω IN/OUT switch to IN. Connect the MIXED VIDEO-VAR AMPL jack on the SIS generator to CHAN B VIDEO IN jack of oscilloscope. Set MIXED VID SEL switch to SIF 1; SIF 1 CODER - FUNCTION SEL switch to N, and SIF 1 CODER - SUBST PULSE SEL switch to A_2.	

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
8. Test mode replies (Cont)	1. Adjust the MIXED VIDEO VAR AMPL control to midrange and set the SIF 1 CODER A to 2. Adjust SUBST PULSE POSN control for 6.5 µs - leading edge of F_1 to leading edge of A_2 as viewed on Channel B of the oscilloscope. Adjust MIXED VIDEO - VAR AMPL control for a 5.0 Volt pulse amplitude. Adjust the SIF 1 CODER - WIDTH ADJ control for a pulse width of 0.8 µs.	
	2. Disconnect cable between AUX MOD IN jack of the rf generator and the CHAL/TAG - VAR AMPL jack on the SIS generator. Disconnect cable from CHAN B VIDEO IN jack of oscilloscope and connect to MAIN MOD IN jack of rf generator.	
	3. Set CHAN B 75Ω IN/OUT switch to OUT. Verify that 0.8 µs modulation pulse is present on oscilloscope Channel A.	
	b. Set MODE 3/A code (C-6280(P)/APX to 7777. Hold RAD TEST-MON to RAD TEST. Adjust OUTPUT ATTEN 0-100 dBm dial on AN/UPM-137 as required to observe replies on oscilloscope Channel A.	Verify F_1, C_1, A_1, C_2, A_2, C_4, A_4, B_1, D_1, B_2, D_2, B_1, D_4, and F_2 pulses are present. (See figure 2-5.)
	c. Set RAD TEST-MON to OUT.	Verify reply pulses not present.
	d. Disconnect cable from MIXED VIDEO VAR AMPL jack of SIS generator and connect to CHAL/TAG - VAR AMPL jack. Set the MIXED VID SEL switch to TAG RESET. Verify presence of modulation (in any mode) on oscilloscope Channel A.	

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
	NOTE During the testing of each mode, make sure all other modes are set to the ON position on the C-6280(P)/APX Panel and all other mode codes are maximized. At the beginning of each mode check, set the selected mode code to 0000 and verify that only the frame pulses are present.	
9. Mode C replies	a. Verify that step 8.d has been performed. On the SIS generator, set the CHAL/TAG CODER MODE 3/A switch to MODE 3/A (off) and the MODE C switch to ON (up) . Set MC-TEST/ON/OUT switch (C-6280(P)/APX) to ON.	Verify that F_1, F_2, and all other pulses, except X, D_1 and D_4, are present. (See figure 2-5.)
	1. Set MODE C ENCODER SIMULATOR (AN/APM-239) to C_1, A_1, C_2, A_2, C_4, A_4, B_1, B_2, D_2, and B_4 observing appearance of each pulse on AN/UPM-137 oscilloscope as it is switched on.	
	b. Set AN/APM-239 MODE C ENCODER SIMULATOR switch to D_4.	Verify that in addition to pulses above, D_4 and SPI (F_3) pulses appear. (See figure 2-6.)
	NOTE On the RT-859A/APX-72 transponder, the SPI pulse does not appear.	
	c. Set AN/APM-239 MODE C ENCODER SIMULATOR switches to OUT.	Verify that only F_1 and F_2 pulses are present.

Table 4-22. Mode 1, 2, 3/A, Test, and C Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
9. Mode C replies (Cont)	d. Set C-6280(P)/APX IDENT-MIC to IDENT and release.	Verify no effect on mode C reply.
	e. Set C-6280(P)/APX MASTER switch to EMER.	Verify no effect on mode C reply.
	f. Set C-6280(P)\APX MASTER switch to NORM, MC-TEST/ON/OUT switch OUT.	Verify no reply pulses present.
	NOTE During the testing of each mode, make sure all other modes are set to the ON position on the C-6280(P)/APX Panel and all other mode codes are maximized. At the beginning of each mode check, set the selected mode code to 0000 and verify that only the frame pulses are present.	
10. Auxiliary trigger	a. Disconnect cable from MAIN MOD IN of rf generator and connect to CHAN B VIDEO IN jack of oscilloscope. Set CHAN B 75 Ω IN/OUT switch to IN. Turn on any mode. Adjust the CHAL/TAG VAR AMPL control full cw and verify that Channel B pulse is 18 Volts minimum in amplitude. Disconnect cable from CHAN B VIDEO IN jack and connect to AUX TRIG jack on AN/APM-239.	Verify that two pulses are present on oscilloscope Channel A.

Table 4-23. Mode 4 Replies, Minimum Performance Standards Usinq AN/UPM-137

STEP	PROCEDURE	PERFORMANCE STANDARD
l.Trigger level	a. Disconnect electronic counter from O TRIG OUT of AN/UPM-137 SIS generator and connect it to SUPPRESSION OUT on the AN/APM-239. On AN/UPM-137, set CHAN A/ALT/CHAN B switch B to CHAN B and VOLT/DIV switch of Channel B to 1.0. Decrease OUTPUT ATTEN 0-100 dBm dial (cw) until trigger pulse appears on oscilloscope.	

Table 4-23. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
1. Trigger level (Cont)	b. On AN/APM-239 remove cable connection from TRIG and connect to REPLY on the AN/APM-245. Set the CHAN B 75 Ω switch on AN/UPM-137 oscilloscope to IN. Set MODE 4 REPLY switch on AN/APM-245 to ON. On AN/APM-245, adjust MODE 4 REPLY AM for a five-volt reply pulse amplitude on B trace of AN/UPM-137 oscilloscope (reply pulses are at t_0 +150 µs to +200 µs. Return cable connection from REPLY to TRIG on the AN/APM-239. Set the CHAN B 75 Ω switch to OUT.	
	c. Increase OUTPUT ATTEN 0-100 dBm dial on AN/UPM-137 to obtain an average suppression count of 90% of previously recorded PRF reading in the preliminary procedures. Reduce OUTPUT ATTEN 0-100 dBm dial setting 3 dB. Observe B trace on AN/UPM-137 oscilloscope for trigger pulse characteristics. Adjust oscilloscope controls (SWEEP, TIME/DIV, and DELAY RANGE) as necessary to observe the trigger pulse.	Trigger pulse characteristics : Amplitude: 1.5 to 5 v Pulse width: 0.5 to 3.0 µs
2. Video output (RT-859/APX-72)	Remove cable from MODE 4 TRIG (AN/APM-239) and connect to MODE 4 INTRR. View pulse characteristics on B trace of AN/UPM-137. Set TEST WORD (AN/APM-245) 5 through 37 to up position one at a time. Observe that A and B displays on the AN/UPM-137 contain 37 pulses. Set TEST WORD 5 through 37 to down position.	Video pulse characteristics : A display: Equals number of pulses compared with B display. B display: Amplitude: 1.5 to 5 v Pulse width: 0.5 +0.1 µs

Table 4-23. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
2A. Video output (RT-859A/APX-72)	Remove cable from MODE 4 TRIG (AN/APM-239) and connect to MODE 4 INTRR. View pulse characteristics on B trace of AN/UPM-137. Set TEST WORD (AN/APM-245) 5 through 37 to up position one at a time. Observe that A display on the AN/UPM-137 contains 37 pulses, and B display contains 35 pulses. Set TEST WORD 5 through 37 to down position.	Video pulse characteristics : A display: Contains two more pulses than B display. B display: Amplitude: 1.5 to 5 v pulse width: 0.5 +0.1 µs
	NOTE Increase the PRF to 1000 using the INT PRF FREQ ADJ control of the AN/APM-245.	
3. Replies	a. Set MODE 4 AUDIO-LIGHT (C-6280 (P)/APX) on AN/APM-239 to LIGHT. Three mode 4 reply pulses should appear on A display of AN/UPM-137 (reply pulses are at t_0 +150 µs to +200 µs. If necessary, decrease OUTPUT ATTEN 0-100 dBm dial of AN/UPM-137 to display pulses. Set CHAN A 75 Ω switch to IN. Measure rise time and decay time between 10% and 90%.	Verify that REPLY light comes on. Reply pulse characteristics : Duration: 0.45 to 1.0 µs Risetime: 0.05 to 0.1 µs Decay time: 0.05 to 0.2 µs Amplitude jitter: 5% or less .
	NOTE Decrease the PRF to 500.	
	b. Set C-6280(P)/APX IDENT-MIC to IDENT and release.	Verify no effect on mode 4 reply.
	c. Set C-6280(P)/APX MASTER switch to EMER.	Verify no effect on mode 4 reply.

Table 4-23. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
3. Replies (Cont)	d.	Set C-6280(P)/APX MASTER switch to STBY. CAUTION light is on, and REPLY light is off.	Verify no mode 4 reply.
	e.	Set C-6280(P)/APX MASTER switch to NORM. CAUTION light is off, and REPLY light is on.	Verify mode 4 reply appears.
4. Reply light	a.	Set the PRF SEL switch of the AN/APM-245 to INT-L. Adjust the INT PRF FREQ ADJ of the AN/APM-245 for an electronic counter indication of 91 ±2. On the AN/APM-245, set GO/NO-GO switch to GO and wait for REPLY light on C-6280(P)/APX to go out. Press GO/NO-GO pushbutton. REPLY light lights momentarily. Set GO/NO-GO switch to OFF.	Verify REPLY light comes on for a period of 2 to 5 seconds .
	b.	Using above procedure, adjust PRF to obtain a counter indication of 61 ±2. Set GO/NO-GO switch to NO-GO and wait for REPLY light to go out. Press GO/NO-GO pushbutton. REPLY light on C-6280(P)/APX does not light.	Verify REPLY light remains off.
5. Caution light	a.	Set GO/NO-GO switch to OFF. Adjust the INT PRF FREQ ADJ of the AN/APM-245 for a counter indication of 91 ±2. Set MODE 4 REPLY on AN/APM-245 to OFF, set GO/NO-GO switch to GO and wait for CAUTION light on AN/APM-239 to go out. Press GO/NO-GO pushbutton. CAUTION light on AN/APM-239 comes on momentarily. Set MODE 4 REPLY switch to ON and then set GO/NO-GO switch to OFF.	Verify CAUTION light comes on for a period of 2 to 5 seconds.
	b.	Using above procedure, adjust PRF to obtain a counter indication of 61 ±2. Set MODE 4 REPLY to OFF. Set GO/NO-GO switch to NO-GO and wait for CAUTION light to go out. Press GO/NO-GO pushbutton. CAUTION light on AN/APM-239	Verify CAUTION light does not light when GO/NO-GO pushbutton is pressed.

Table 4-23. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP		PROCEDURE	PERFORMANCE STANDARD
5. Caution light (Cont)		remains off. Return Go/NO-GO switch to OFF. (CAUTION light comes on.)	
6. Audio output	a.	On AN/APM-239, remove cable from MODE 4 INTRR jack, add a coax tee to tablet and COnneCt it to AUDIO jack. Connect 150 0 load on open end of coax tee. Set C-6280(P)/APX AUDIO-OUT-LIGHT to AUDIO. Remove electronic counter connection from SUPPRESSION OUT jack of ANIAPM-239 and connect to O TRIG on AN/UPM-137. Set the PRF SEL switch on AN/APM-245 to INT-MED. Adjust the INT PRF FREQ ADJ of the AN/APM-245 for a counter indication of 500±20. Reconnect electronic counter connection to SUPPRESSION OUT on AN/APM-239. Observe audio signal on B trace of AN/UPM-137 oscilloscope.	Audio signal characteristics: Width of negative part of pulse 500 PS minimum with a pulse amplitude of 3 V P-P minimum.
	b.	Set AN/APM-245 MODE 4 DISPARITY to DL-1 and if audio is present on AN/UPM-137 oscilloscope, adjust DL-1 clockwise until audio disappears.	
	c.	Set AN/APM-245 MODE 4 DISPARITY to OFF.	Verify audio signal present.
	d.	Set C-6280(P)\APX AUDIO-OUT LIGHT to OUT. Set MODE 4 REPLY (AN/APM-245) to ON.	Verify audio signal not present.
7. Limiter	a.	Observe the replies on the A trace of the AN/UPM-137 oscilloscope. Adjust oscilloscope controls as necessary to observe the replies.	

Table 4-23. Mode 4 Replies, Minimum Performance Standards Using AN/UPM-137 (Cont)

STEP	PROCEDURE	PERFORMANCE STANDARD
7. Limiter (Cont)	b. Set the PRF SEL switch on the AN/APM-245 to INT-H. Increase INT PRF FREQ ADJ on AN/APM-245 until electronic counter indication stops increasing. This indicates point at which mode 4 limiter begins operation.	Rate 1500 to 2500 replies per second.
8. MTL	Set the PRF SEL switch to AN/APM-245 to INT-MED. Adjust the INT PRF FREQ ADJ on the AN/APM-245 until the electronic counter indicates 500 ±20. Note average counter reading. Increase OUTPUT ATTEN 0-100 dBm dial on AN/UPM-137 until counter indication drops to 400 average. Decrease attenuation until counter indication averages 90% of above noted reading. Compute MTL using formula found in earlier part of starting procedure.	-77 dBm ±3.

(b) Set TEST WORD switches (AN/APM-245) 1 through 4 to up position and adjust TEST WORD AM for an 8-volt amplitude on AN/UPM-137 oscilloscope Channel A.

(c) Disconnect cable from CHAN A VIDEO IN of AN/UPM-137 oscilloscope and connect to MAIN MOD IN of AN/UPM-137 rf generator.

(d) Connect VIDEO OUT of rf generator to CHAN A VIDEO IN of oscilloscope.

(e) Set C-6280(P)/APX (AN/APM-239) MASTER switch to STBY for 1 minute then to NORM and MODE 4 to ON.

(f) On electronic counter, adjust sensitivity control as necessary to trigger counter.

(g) Readjust INT PRF FREQ ADJ for an indication of 500 ±20 on the electronic counter. Observe average reading on electronic counter and record for use in the performance procedures.

4-13. TROUBLESHOOTING .

4-14. The intermediate, direct, and general maintenance procedures in this manual supplement the procedures described in the organizational manual (NAVSHIPS 0967-217-4010 and TM1l-5895-490-20). The

systematic troubleshooting procedure, which begins with the operational checks that can be performed at an organizational level, is prepared for a higher level of maintenance in this manual. Sectionalizing, localizing, and isolating techniques and test equipment used in the troubleshooting procedure are more complex.

4-15. SYSTEM TROUBLESHOOTING. Performance of system troubleshooting procedures requires access to the test points on the power supply and other subassemblies of the receiver-transmitter. This requires depressurization and disassembly (refer to paragraph 4-17) and use of jumper type test cable assemblies supplied with AN/APM-239 as illustrated in figure 4-11. To troubleshoot the system using the AN/UPM-98A test set and associated equipment, first follow the test setup procedures in step a. below. To troubleshoot the system using the AN/UPM-137 test set and associated equipment, first follow the test setup procedures in paragraphs 4-12a. and 4-12b. After the initial setups are made, trouble shooting is then performed using the procedures stated in paragraph b. below. Table 4-24 is an alphanumeric listing of test points and adjustments for the receiver-transmitter with corresponding schematic and waveform references. Location of test points and adjustment controls are illustrated in figure 4-13. Table 4-1 lists test equipment required.

WARNING

Lethal voltages are present when power is applied to the test setup. These dangerous voltages are present at exposed points; identified by red cables and pins, which indicate 1000 V dc connections. High voltage locations are shown in figure 4-13.

a. Bench Test Setup. To prepare the receiver-transmitter and associated test equipment for troubleshooting procedures using the AN/UPM-98A test set, assemble the equipment as illustrated in figure 4-12 and proceed as follows:

1. Receiver-Transmitter

(a) Repressurize and disassemble this equipment as described in paragraph 4-17.

(b) Join units together as shown in figure 4-12. (A typical test jig can be made by welding two flange coupler (part number 4023417-0701) together and clamping the two sections of the receiver-transmitter in this jig supporting the rf section with a wood block.)

(c) Connect plug T2P1 of rf test cable (see figure 4-11) to jack AR3J1 (see figure 4-13) on the video detector and amplifier.

(d) Connect jack T2J1 of rf test cable to plug P3, the coaxial lead from the digital and power supply section.

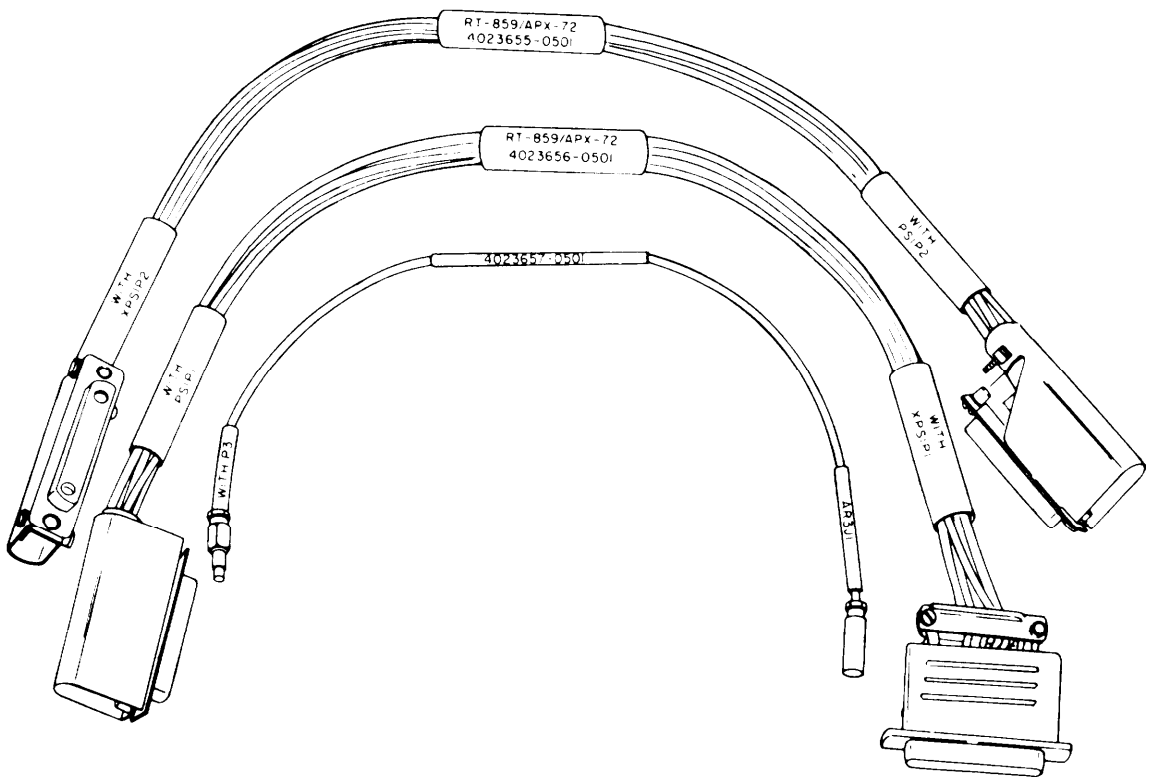


Figure 4-11. Typical Test Cable Assemblies

(e) Connect the power supply test cable (see figure 4-11) between PSIJ1 in the rf section and PS1P2 on the power supply.

(f) Connect ANT. J5 to HP IN on AN/UPM-98A.

(g) Connect POWER, CONTROL & VIDEO J1 to TRANSPONDER power and control on AN/APM–239.

2. Test Set, Transponder AN/APM-239.

(a) Connect PWR INPUT to 115 vat, 400-Hz power source.

(b) Connect MODE 4 COMPUTER to AN/APM-245 J1 MODE 4.

(c) Ensure TRANSPONDER power and control is connected to POWER, CONTROL & VIDEO J1 on receiver-transmitter.

(d) Terminate AUDIO COMMON with attached termination.

(e) Terminate REPLY with a 50-Ohm termination.

(f) Set all controls and switches as directed in table 4-2.

3. Test Set, Simulator AN/APM-245.

(a) Connect Jll POWER to 115-vat, 60-Hz voltage source.

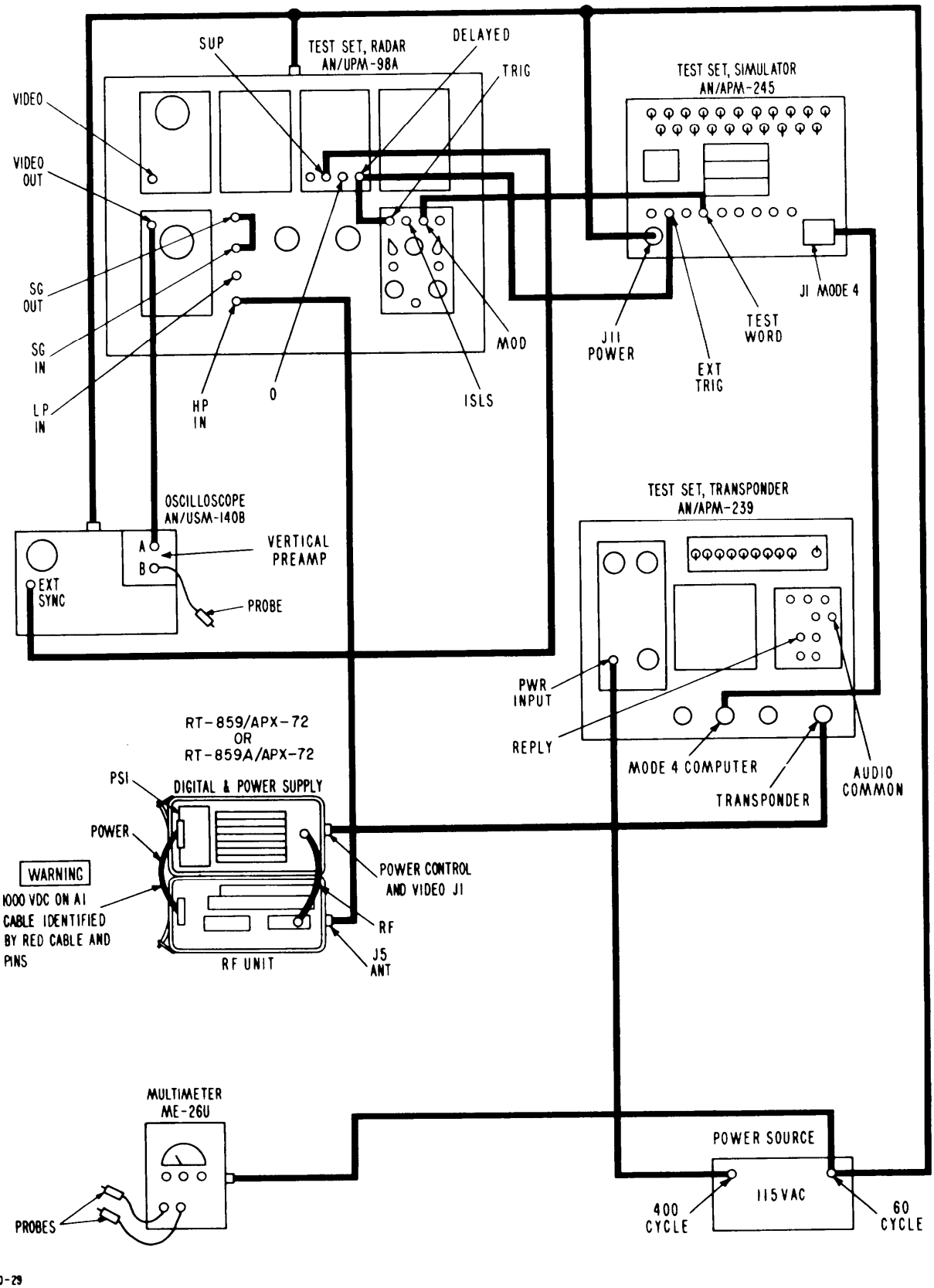


Figure 4-12. Receiver-Transmitter Troubleshooting Test Setup

(b) Ensure that J1 MODE 4 is connected to MODE 4 COMPUTER on AN/APM-239.

(c) Connect TEST WORD to input A on VERTICAL AMPLIFIER AN/USM-140B.

(d) Connect EXT TRIG to one end of coax tee connected to DELAYED TRIGGERS (XTAL MARK & SYNC) on AN/UPM-98A.

(e) Set all controls and switches as directed in table 4-13.

4. Test Set, Radar AN/UPM-98A.

(a) Connect power cord to 115-vac, 60-Hz source.

(b) Connect a coax tee on DELAYED TRIGGERS (XTAL MARK & SYNC) jack.

(c) Connect a cable between one end of coax tee on DELAYED TRIGGERS and TRIG (INTERROGATION CODER) .

(d) Ensure one end of coax tee DELAYED TRIGGERS is connected to EXT TRIG on AN/APM-245.

(e) Connect a jumper cable from SG IN to SG OUT.

(f) Terminate LP IN with dummy load plug 8P15 attached.

(g) Ensure HP IN connected to ANT. J5 on receiver-transmitter.

(h) Connect SUP TRIGGERS (XTAL MARK & SYNC) to EXT SYNC on AN/USM-140B.

(i) Set all controls and switches as directed in table 4-5.

5. Oscilloscope, AN/USM-140B.

(a) Connect power cord to 115-vac, 60-Hz source.

(b) Ensure that input A VERTICAL AMPLIFIER is connected to TEST WORD on AN/APM-245.

(c) Ensure that EXT SYNC is connected to SUP TRIGGERS (XTAL MARK & SYNC) on AN/UPM-98A.

(d) Attach a probe to input B VERTICAL AMPLIFIER.

(e) Set POWER ON.

(f) Set all controls and switches to obtain a presentation on oscilloscope.

6. Multimeter, ME-26/ or Electronic Voltmeter, ME-202( )/u. Connect power cord to 115-vac, 60-Hz power source and set for voltage measurements.

7. Preliminary Procedures.

(a) Set TEST WORD switches (AN/APM-245) 1 through 4 to up position and adjust TEST WORD AM. for a 20-volt amplitude on A trace of AN/USM-140B.

(b) Disconnect cable from input A on VERTICAL AMPLIFIER AN/USM-140B and connect to MOD (INTERROGATION CODER) on AN/UPM-98A.

(c) Connect VIDEO OUT (CAL-CONTROL) on AN/UPM-98A to input A on VERTICAL AMPLIFIER AN/USM-140B.

(d) Set TRIGGER (CAL-CONTROL) to obtain a full scale meter indication.

(e) Switch METER SELECT to 500 PRF and TRIGGER to INT.

Table 4-24. Test Points and Adjustments

TEST POINT OR ADJUSTMENT	FUNCTIONAL DESCRIPTION	SCHEMATIC AND WAVEFORM REFERENCE
	PROCESSOR	
A1R6	-3-dB Subtracter	Figure 6-4 or 6-5
A1R10	Ditch Length Adjust (RT-859/APX-72) or Wide pulse Adjust (RT-859A/APX-72)	
A1R22	-93-dBV Threshold Adjust	
A1R25	-90-dBV Threshold Adjust	
AITP1	Processed Video Out	
A1TP2	Width Processor	
A1TP3	Delayed Video	
A1TP4	SLS Ditch	
A1TP5	Amplitude Processor Out	
A1TP6	Log Video Input	
	DECODER	
A2R51	Duty Cycle Adjust	Figure 6-8 or 6-9
A2R89	Reply Rate Adjust	
A2TP1	Suppression Output	
A2TP2	Automatic Overload Control Bias (+ Voltage)	
A2TP3	Mode 4 Suppression Out	
A2TP4	Mode 2 Decode	
A2TP5	Side Lobe Suppression Generator Out	
A2TP6	Duty Cycle Integrator Out	
A2TP7	Mode 2 Decode Strobe (0.1 µs)	
A2TP8	Internal Suppression Gate	
	MODE 4 (PART NO. 4028683-0502)	
A3R29	Mode 4 AOC Adjust	Figure 6-10 or 6-11
A3R89	Audio Adjust	
A3R215	90 µs Timer Adjust (RT-859A/APX-72 only)	
A3R224	300 µs Timer Adjust (RT-859B/APx-72 only)	

Table 4-24. Test Points and Adjustments (Cont)

TEST POINT OR ADJUSTMENT	FUNCTIONAL DESCRIPTION	SCHEMATIC AND WAVEFORM REFERENCE
	MODE 4 (Cont)	
A3TP1	Audio	
A3TP2	No Disparity, No Reply (Negative Pulse)	
A3TP3	Caution Light Gate	
A3TP4	Reply Pulse	
A3TP5	Reply Gate	
A3TP6	Inhibit SIF Decode	
A3TP7	Mode 4 Decode	
A3TP8	Positive 290 μs Pulse After Decode	
	MODE 4 (PART NO. 116104-1)	
A3R1	Mode 4 AOC Adjust	Figure 6-11A
A3R2	Audio Adjust	
A3TP1	Reply Rate Integrator	
A3TP2	Ditch Lock	
A3TP3	Audio Pulse	
A3TP4	222.222-kHz Square Wave	
A3TP5	No Disparity, No reply	
A3TP6	Mode 4 Decode	
A3TP7	Reply Transmitted	
	ENCODER CLOCK	
A4C1	Gated Oscillator Adjust	Figure 6-12
A4TP1	CW Clock Enable	
A4TP2	Mode 3 Decode	
A4TP3	Clock Gate	
A4TP4	Modulation Trigger	
A4TP5	Separation Monostable Multivibrator	
A4TP6	Bi-phase Clock Strobe	
A4TP7	2° Input	
A4TP8	-3V Reference (Compensated Voltage)	
A4TP9	Ground	

Table 4-24. Test Points and Adjustments (Cont)

TEST POINT OR ADJUSTMENT	FUNCTIONAL DESCRIPTION	SCHEMATIC AND WAVEFORM REFERENCE
	ENCODER CONTROL	
A5TP1	E-1 Input	Figure 6-13
A5TP2	C_1/D_1 Pulses	
A5TP3	A_1/B_2 Pulses	
A5TP4	A_2/B_4 Pulses	
A5TP5	C_4/D_4 Pulses	
A5TP6	Emergency Gate	
A5TP7	F_1/B_l Pulses	

Table 4-24. Test Points and Adjustments (Cent]

TEST POINT OR ADJUSTMENT	FUNCTIONAL DESCRIPTION	SCHEMATIC AND WAVEFORM REFERENCE
	ENCODER CONTROL (Cont)	
A5TP8	C_2/D_2 Pulses	
A5TP9	2^4 - 1 Gate	
A5TP10	A_4/F_2 Pulses	
	ENCODER GATING	
A6TP1	Emergency Gate Output	Figure 6-14 or 6-15
A6TP2	External SIF Emergency Enable	
A6TP3	I/P Control	
A6TP4	E-1 Output	
A6TP5	Reset Generator “1” Side	
A6TP6	2^5 - 1 Gate	
A6TP7	2^6 - 0 Gate	
A6TP8	Auxiliary Reset Trigger	
A6TP9	2^3 - 1 Gate	
A6TP10	2^4 - 1 Gate	
	MODULATOR	
A7R4	Transmitter Pulse Width Adjust	Figure 6-16
	SENSITIVITY	
A8R5	Low	Figure 6-3
A8R6	Normal	
	RF AMPLIFIER	
AR1C1	Bandpass Adjust	
AR1C2	Bandpass Adjust	
AR1C3	Bandpass Adjust	
	POWER AMPLIFIER	
AR2C1	Output Power Adjust	

Table 4-24. Test Points and Adjustments (Cont)

TEST POINT OR ADJUSTMENT	FUNCTIONAL DESCRIPTION	SCHEMATIC AND WAVEFORM REFERENCE
	DETECTOR AND VIDEO AMPLIFIER (PART NO. 4023409-0501 AND 4023409-0502 ONLY)	
AR3J1	Video Out	Figure 6-1
AR3R73	+4.5 v Adjust	
AR3R76	-4.5 v Adjust	
AR3TP1	Detected Video Input	
AR3TP2	+4.5 vdc Voltage Level	
AR3TP3	-4.5 vdc Voltage Level	
AR3TP4	Log Video Output	
	DETECTOR AND VIDEO AMPLIFIER (PART NO. 4023409-0503)	
AR3J1	Video Output	Figure 6-2
AR3TP1	Detected Video Input	
AR3TP2		
AR3TP3		
AR3TP4	+6.2 Voltage Level	
	POWER SUPPLY	
PS1TP1	Ground	Figure 6-17
PS1TP2	+6.3 v Return	
PS1TP3	+6.3 vdc	
PS1TP4	+6 vdc	
PS1TP5	+12 vdc	
PS1TP6	+25 vdc	
PS1TP7	-6 vdc	
PS1TP8	-80 vdc	
PS1TP9	-110 vdc	
PS1TP10	+1000 vdc Divided by 100	

Table 4-24. Test Points and Adjustments (Cont)

TEST POINT OR ADJUSTMENT	FUNCTIONAL DESCRIPTION	SCHEMATIC AND WAVEFORM REFERENCE
	PRESELECTOR	
Z1C1	Bandpass Adjust	
Z1C2	Bandpass Adjust	
Z1C3	Bandpass Adjust	
	OSCILLATOR	
Z2C1	Frequency Adjust	

(f) Adjust PRF (XTAL MARK & SYNC) for a meter indication of 500 PRF.

(g) Set VIDEO OUT (CAL-CONTROL) to SIG MON.

(h) Adjust AN/USM-140B to view an interrogation pulse pair (four pulses for mode 4) and adjust pulse for a width of 0.8 ±0.1 µs by rotating CODE WIDTH control on AN/UPM-98A.

(i) ISLS SELECT (INTERROGATION CODER) to 2 µSEC. (8 µSEC for mode 4)

(j) Adjust ISLS pulse width to 0.8 ±0.1 µs by rotating ISLS WIDTH control.

(k) ISLS SELECT to CHECK.

(l) Adjust SG FREQUENCY for 1030 MHz by zero-beating the first interrogation pulse with precision 1030 ISLS pulse. (SIF modes only)

(m) Set ISLS SELECT (INTERROGATION CODER) to OUT.

(n) Adjust ATTENUATION for a -60-dBV signal at ANT. J5 of receiver-transmitter. Refer to paragraph 4-11.3.(1).

(o) Set VIDEO OUT (CAL-CONTROL) to SHAPE.

b. Troubleshooting Procedures. Preliminary to troubleshooting the receiver-transmitter, verify or determine through the checkout procedures (paragraph 4-6) the failure symptoms or abnormal conditions that have been observed in the operation of the equipment. Having determined the general trouble symptoms, proceed as follows:

1. Ensure circuitboard assemblies are inserted in assigned chassis connectors by checking color coding and key alignment.

2. Ensure circuitboard assemblies are properly seated to make good electrical contact.

CAUTION

To prevent damage to equipment ensure that C-6280(P)/APX MASTER switch is OFF before removing any circuitboard or component subassembly.

3. Measure power supply voltages as directed in table 4-25.

4. Enter column titled Symptoms in table 4-26 and select the symptom that describes the condition of the receiver-transmitter being tested. Perform the indicated troubleshooting procedures listed in Action column.

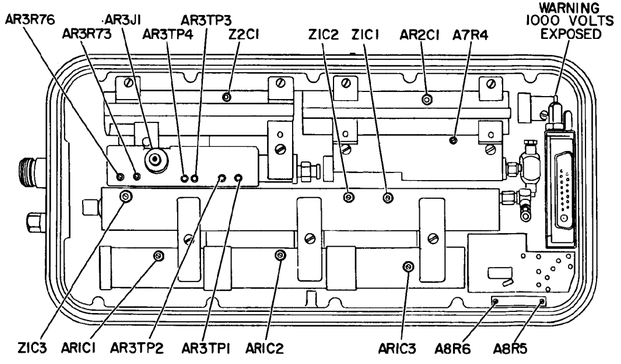
(a) Use of System Troubleshooting Chart. Table 4-26 is divided into three columns. Symptom, which describes the condition of the receiver-transmitter being tested, is in column one. Adjacent to the symptom, in the second column is listed one or more causes that would produce this symptom. For each probable cause listed, a parallel course of action is described in column three, which, when performed, will correct the equipment malfunction.

(b) Use of Comprehensive Troubleshooting Charts. Tables 4-27 and 4-28 are comprehensive troubleshooting charts designed to localize trouble to a circuitboard or component subassembly by observing the waveform structure at selected test points. To use table 4-27, set up test equipment, selecting settings for mode 2 operation. Apply the interrogation signal to the receiver-transmitter and the test probe of the oscilloscope to the test points in table 4-27 in sequence. If the waveform observed is correct (refer to table 4-24 and referenced schematics) proceed in the direction of the YES arrow to the next test point. If the waveform is incorrect, proceed in the direction of the NO arrow. Table 4-28 is used in the same manner as above using a mode 4 interrogation pulse.

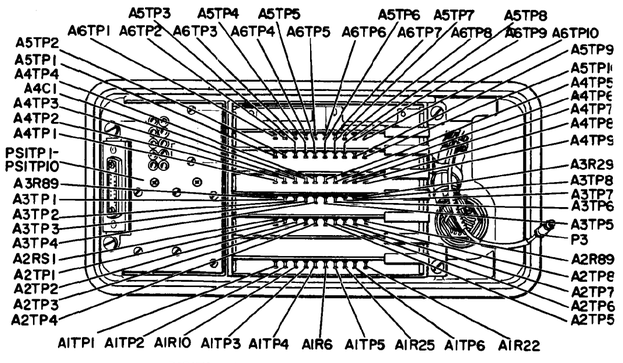
5. Replace suspected subassembly with a known good replacement, return test setup to operational status, and recheck waveform at same test point. (Adhere to the foregoing CAUTION on removal and replacement of circuit board or component subassemblies.)

6. Reassemble the receiver-transmitter. (Refer to disassembly instructions of paragraph 4-17.) Apply heat sink compound (as directed) and return for checkout testing. The faulty circuitboard or component subassemblies shall be subjected to the subassembly troubleshooting procedures of paragraph 4-16.

4-16. SUBASSEMBLY TROUBLESHOOTING. For troubleshooting purposes, the receiver-transmitter subassemblies are divided into three categories: a) removal circuitboard subassemblies which require the use of extender boards for in-circuit troubleshooting, b) circuitboard and component subassemblies which can be inspected without removal from the circuit, and c) circuitboard and component subassemblies which must be removed from circuit for troubleshooting. General troubleshooting procedures include: referring to applicable wiring diagrams for component location, pin numbering, and general orientation, observing waveforms at test points and comparing them with those shown on applicable schematics referenced in table 4-24; comparing pin voltage measurements with standards



RF SECTION



DIGITAL AND POWER SUPPLY SECTION

Figure 4-13. Test Point and Adjustment Locations

Table 4-25. Power Supply, Minimum Performance Standards

STEP	PROCEDURE	MEASURE
1.	Using bench test setup of figure 4-4 or 4-12, place AN/APM-239 TRANSPONDER PWR INPUT to DC ONLY, METER SELECTION to DC and adjust DC OUTPUT CONTROL for 27.5 vdc. Set the C-6280()(P)/APX MASTER Control to NORMAL.	
2.	Connect negative lead of ME-26U multimeter to TP2 (+6.3v RET) and positive lead to TP3 (+6.3 VDC).	6.3 ±0.19 vdc
3.	Disconnect ME-26U leads. Connect negative to TP1 (GRD) and positive lead to TP3 (+6.3 VDC).	6.3 ±0.19 vdc
4.	Disconnect ME-26U positive lead from TP3 (+6.3 VDC) and connect to TP4 (+6 VDC).	6.0 ±0.18 vdc
5.	Disconnect ME-26U positive lead from TP4 (+6 VDC) and connect to TPS (+12 VDC).	12.0 ±0.36 vdc
6.	Disconnect ME-26U positive lead from TP5 (+12 VDC) and connect to TP6 (+25 VDC).	25.0 ±0.75 vdc
7.	Disconnect ME-26U leads. Connect positive lead to TP1 (GRD) and negative to TP7 (-6 VDC).	-6.0 ±0.18 vdc
8.	Disconnect ME-26U negative lead from TP7 (-6 VDC) and connect to TP8 (-80 VDC).	-80 ±2.4 vdc
9.	Disconnect ME-26U negative lead from TP8 (-80 VDC) and connect to TP9 (-110 VDC).	-110 to -115.5 vdc (-110 vdc nominal)
10.	Disconnect ME-26U leads. Connect positive lead to TP1O (+1000 VDC) and negative lead to TP1 (GRD).	9.6 vdc
11.	Disconnect ME-26U positive and negative leads from power supply. Place AN/APM-239 TRANSPONDER PWR INPUT AC/DC, METER SELECTION to AC and adjust AC OUTPUT CONTROL for 115 volts. Repeat steps 2 through 10.	

Table 4-26. System Troubleshooting Procedures Chart

SYMPTOM	PROBABLE CAUSE	ACTION
1. No replies any mode	a. Power supply failure	Measure power supply voltage as directed in table 4-25. Replace power supply, if defective, and repeat measurement procedures. (Refer to paragraph 4-16.b.5. and 6.)
	b. Circuit failure	Perform comprehensive troubleshooting procedures of table 4-27 to isolate trouble. Replace defective subassembly and repeat test procedures. (Refer to paragraph 4.15.b.5. and 6.)
2. No replies in modes 1, 2, 3/A, test, and C. Mode 4 replies correct.	Circuit failure	Perform comprehensive troubleshooting procedures of table 4-27 steps 5 through 10. Replace defective subassembly and repeat test procedures. (Refer to paragraph 4-15.b.5. and 6.)
3. No replies in mode 4. Modes 1, 2, 3/A, test and C correct.	Circuit failure	Perform comprehensive troubleshooting procedures of table 4-28 or 4-28A. Replace defective subassembly and repeat test procedures. (Refer to paragraph 4-15.b.5 and 6.)
4. Incorrect replies in modes 1, 2, 3/A, test, and C. Mode 4 replies correct.	a. Encoder control failure	Change mode of operation and interrogation from mode 2 to mode 3/A. If mode 3/A replies are correct, replace encoder control circuitboard. (Refer to paragraph 4-15.b.5. and 6.)
	b. Encoder clock failure	If mode 3/A replies are incorrect in item 4.a. , above, replace encoder clock circuitboard. (Refer to paragraph 4-15.b.5. and 6. and repeat mode 2 and 3/A tests.) If replies are correct, original encoder clock circuitboard is malfunctioning.
	c. Encoder gating failure	If replies in item 4.b., above, are still incorrect, replace encoder gating circuitboard (refer to paragraph 4-15.b.5. and 6. and repeat

Table 4-26. System Troubleshooting Procedures Chart (Cont)

SYMPTOM	PROBABLE CAUSE	ACTION
4. (Cont)		mode 2 and 3/A tests) . If replies are correct, original encoder gating circuitboard is malfunctioning.
	d. Internal or external wiring failure	If results of tests in items 4.a., b., and c. are negative, check internal and external wiring. (See figures 6-20 and 6-21 or 6-22.)
5. Incorrect or no replies in emergency operation in modes 1, 2, or 3/A.	a. Encoder gating failure	Observe waveforms at test points A6TP1 and A6TP5 on the encoder gating circuitboard and A5TP1, A5TP6, and A5TP9 on the encoder control circuitboard. If incorrect waveforms are observed, replace encoder gating circuitboard (refer to paragraph 4-15.b.5. and 6.) and repeat test procedures. If correct waveforms were originally observed, proceed to item 5.b.
	b. Encoder control failure	Replace encoder control circuitboard (refer to paragraph 4-15. b.5. and 6.) and observe waveform at test point A4TP1 on encoder clock control circuitboard. If correct, original encoder control circuitboard is malfunctioning. If incorrect, proceed to item 5.c.
	c. Encoder Clock failure	Replace encoder clock circuitboard (refer to paragraph 4-15.b.5. and 6.) and observe waveform at test point A4TP4 on encoder clock circuitboard. If correct, original encoder clock circuitboard is malfunctioning. If incorrect, check internal and external wiring. (See figures 6-20 and 6-21.)

Table 4-26. System Troubleshooting Procedures Chart (Cont)

SYMPTOM	PROBABLE CAUSE	ACTION
6. Incorrect or no replies in I/P operation in modes 1, 2, or 3/A.	a. Encoder gating failure	Observe waveforms at test points A6TP3, A6TP9, and A6TP5 on the encoder gating circuitboard and test points A4TP6 and A4TP7 on the encoder clock circuitboard. If incorrect waveforms are observed, replace encoder qating circuitboard (refer to paragraph 4–15.b.5. and 6.) and repeat test procedures. If correct waveforms were originally observed, proceed to item 6.b.
	b. Encoder clock failure	Replace encoder clock circuitboard (refer to paragraph 4-15.b.5. and 6.) and observe waveform at test point A4TP4 on encoder clock circuitboard. If correct, oriqinal encoder clock circuitboarcl is malfunctioning. If incorrect, check internal and external wiring. (See figures 6-20 and 6-21 or 6-22.)

Table 4-27. Modes 1, 2, 3/A, Test, and C Comprehensive Troubleshooting Chart

STEP	CIRCUIT	TEST POINT	FAILED CIRCUIT
1.	Detector and Video Amplifier	AR3TPl — No →	Receiver Zl/ARl Failure
		Yes	
2.	Detector and Video Amplifier (Part No. 4023409-0501 and 4023409-0502) (Part No. 4023409-0503)	AR3TP4 AR3Jl — No →	Video Amplifier Failure
		Yes	
3.	Processor	AlTP6 — No →	Video X7 Amplifier Failure
		Yes	

Table 4-27. Modes 1, 2, 3/A, Test, and C Comprehensive Troubleshooting Chart (Cont)

STEP	CIRCUIT	TEST POINT	FAILED CIRCUIT
4.	Processor	A1TP2 — No →	Processor Circuitboard Failure in Area of Integrated Circuit A1
		Yes ↓	
5.	Decoder/Delay Line	A2TP7 — No →	Delay Line Failure of 1.5 μsec Section
		Yes ↓	
6.	Decoder	A2TP4 — No →	Decoder Circuitboard Failure
		Yes ↓	
7.	Encoder Clock	A4TP3 — No →	Clock Circuitboard Failure
		Yes ↓	
8.	Encoder Clock	A4TP6 — No →	Clock Circuitboard Failure
		Yes ↓	
9.	Encoder Clock/Gating	A6TP5 — No →	Gating Circuitboard Failure Clock Circuitboard Failure
		Yes ↓	
10.	Encoder Clock	A4TP4 — No →	Clock Circuitboard Failure
		Yes ↓	
11.	RF Unit	Modulator A7 or Transmitter	

Table 4-28. Mode 4 (Part No. 4028683-0502)
Comprehensive Troubleshooting Chart

STEP	CIRCUIT	TEST POINT	FAILED CIRCUIT
1.	Mode 4	A3TP7	No → Delay Line Failure No → Mode 4 Failure No → Decoder Failure Yes
2.	Mode 4	A3TP4	No → Mode 4 Failure Yes
3.	Encoder Clock	A4TP4	No → Encoder Clock Failure Yes → Internal or External Wiring

Table 4-28A. Mode 4 (Part No. 116104-1)
Comprehensive Troubleshooting Chart

STEP	CIRCUIT	TEST POINT	FAILED CIRCUIT
1.	Mode 4	A3TP6	No → Delay Line No → Mode 4 No → Decoder Yes
2.	Mode 4	A3TP7	No → Mode 4 Yes
3.	Encoder Clock	A4TP4	No → Encoder Clock Yes → Internal or External Wiring

shown in table 4-30; and measuring resistance when indicated in applicable tables. Functional troubleshooting tables 4-31 through 4-32 are presented for circuitboard and power supply subassemblies.

a. Extender Board Procedure. The removable circuitboard subassembly is prepared for troubleshooting by mounting it in applicable extender board (see figure 4-14) listed in table 4-29. The circuitboard and extender board is then substituted in the applicable chassis connector of a known serviceable receiver-transmitter establishing the basis that all inputs to the malfunctioning circuitboard are norms 1. The test setup used is shown in figure 4-12 and described in paragraph 4-15a. Functional troubleshooting table 4-31 describes the troubleshooting procedures for the removable circuitboard subassemblies.

b. In-Circuit Procedure. The test and terminal points of A7 Modulator, A8 Sensitivity, AR1 RF Amplifier, AR2 Power Amplifier, and Z2 Oscillator subassemblies are readily available for troubleshooting without the need for disassembly or removal from the circuit. Set up receiver-transmitter and allied test equipment as shown in figure 4-12 and described in paragraph 4-15, and proceed with troubleshooting procedures of table 4-32.

c. Out of Circuit Procedure. Detector and Video Amplifier AR3, Delay Line DL1, and Power Supply PS1 must be removed from the

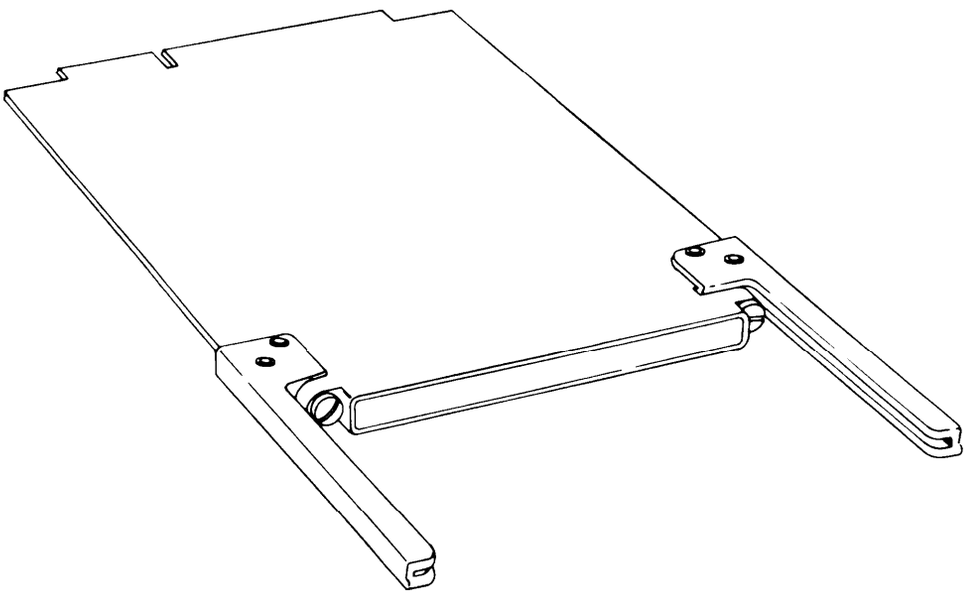


Figure 4-14. Typical Extender Board Assembly

Table 4-29. Extender Boards for Removable Subassemblies

TITLE	TYPE	PART NUMBER	CONNECTOR PART NUMBER
Al Processor (RT-859/APX-72)	44 pin	4023635-0501	4023569-0705
Al Processor (RT-859A/APX-72)	44 pin	4023635-0505	4023569-0705
A2 Decoder	66 pin	4023496-0502	176-112-07
A3 Mode 4 (RT-859/APX-72)	44 pin	4023635-0502	4023569-0705
A3 Mode 4 (RT-859A/APX-72)	44 pin	4023635-0506	4023569-0705
A4 Encoder Clock	44 pin	4023635-0503	4023569-0705
A5 Encoder Control	66 pin	4023496-0501	176-112-07
A6 Encoder Gating	44 pin	4023635-0504	4023569-0705

receiver-transmitter to perform troubleshooting procedures prescribed in table 4-33.

1. Setup AR3 for troubleshooting as follows.

(a) Perform disassembly procedures of paragraph 4-19 and steps a. and b. of paragraph 4-21.

(b) Loosen cable connection (20, figure 4-17).

(c) Disconnect cable connection (21, figure 4-17) from preselector Z1 using a l/4-inch open–end wrench.

(d) Remove screws 1, 2, 3, and associated clamps (figure 4-17).

(e) Remove Z1.

(f) Remove screws 9, 12, and associated clamp (figure 4-17).

(g) Remove AR3 and connecting cable (figure 4-17).

(h) Replace Z1 and fasten with screws 2 and associated clamp (figure 4-17).

(i) Reconnect cable (1, figure 4-15) to Z1.

(j) Remove screw (2, figure 4-15).

(k) Insert plastic shims (3, figure 4-15) between each side of cover (4, figure 4-15) and circuitboard of AR3 and remove cover.

(1) Place AR3 in position shown in figure 4-15 and tighten cable connection (5, figure 4-15).

(m) Connect receiver-transmitter into circuit shown in figure 4-12 and perform troubleshooting procedures of table 4–33.

2. Replace AR3 after trouble shooting as follows:

(a) Remove receiver-transmitter from test setup of figure 4-12.

(b) Loosen cable connection (5, figure 4-15).

(c) Place plastic shims (3, figure 4-15) over circuit boards of AR3 and slide cover (4, figure 4–15) into place.

(d) Remove plastic shims and secure cover with screw (2, figure 4-15).

(e) Disconnect cable (1, figure 4-15) from Z1.

(f) Remove screw and associated clamp (6, figure 4-15) and remove Z1.

(g) Replace AR3 and connecting cable securing with screws 9, 12, and associated clamp (figure 4-17).

(h) Apply a thin coat of heat conducting compound (refer to paragraph 4-27a.2.(d)) to Z1 and replace with screws (1, 2, 3, figure 4-17).

(i) Reconnect cable connection (21, figure 4-17) to Z1.

(j) Tighten cable connection (20, figure 4-17).

(k) Perform assembly procedures of step u. paragraph 4-32 and paragraph 4-34.

3. Remove DL1 by performing procedures of paragraph 4-19 and step b. of paragraph 4–21. Place DL1 in a suitable jig or holder to prevent damage to circuit-board and make resistance measurements as described in table 4-33 to determine serviceability. Replace DL1 by inserting circuit-board into card cage connector XDL1P1 , identified by red color coding (see figure 4-18) . Reassemble receiver–transmitter as described in paragraph 4-34.

4. Remove PS1 by performing procedures of paragraph 4-20 and step d. of paragraph 4-21. Use a Tester-Dummy Load TS-3243/APM to set up PS1 for troubleshooting as follows:

(a) Make sure that TS-3243/APM POWER and RESERVE LOAD switches are OFF. Connect TS-3243/APM power plug to 107-122 vat, 400 ±20 Hz power source. Verify that POWER indicator is not lit.

(b) Connect P1 and P2 of TS-3243/APM to PSIP1 and PS1P2, respectively.

WARNING

Lethal voltages are present in tester and PS1 when primary power is applied. Caution is necessary.

(c) Place tester POWER switch to ON. Verify that POWER and CONTINUITY indicators are lit. This indicates proper operation of transformer Tl, RF1 filter FL1, and rectifiers CR1 and CR2 in PS1. Also, all signal and control lines in PS1 are good.

(d) Perform steps 2. through 10. of table 4-25 to ensure that PS1 minimum performance standards are met.

(e) Connect differential voltmeter (Mil-V-9989) between TP1 (+) and TP2 of tester and measure 310, +16, -6 vdc.

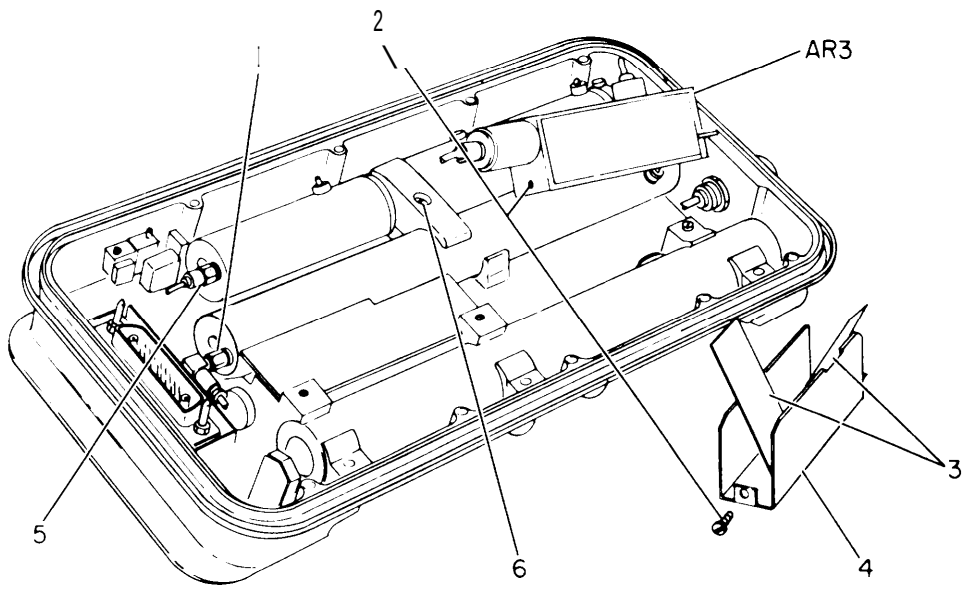


Figure 4-15. Disassembly for Troubleshooting, Detector and Video Amplifier AR3

(f) Place tester POWER switch to OFF and disconnect P1 and P2 of tester from PS1P1 and PS1P2, respectively.

(g) If PS1 does not comply with steps (c) , (d), or (e) above, perform steps 1. and 2. of paragraph 4-21 and step (h) below.

(h) Reconnect P1 and P2 of tester to PS1P1 and PS1P2 and perform troubleshooting procedures of table 4-33.

(i) Should the TS-3243/APM Tester-Dummy Load not be available for maintenance of PS1, the load bank described in Section III may be used along with the following procedures:

(1) Set up PS1 for voltage measurements by separating receiver-transmitter assemblies as described in paragraph 4-19 and connecting into circuit described in paragraph 4-15a., and shown in figure 4-12. Measure voltages as described in table 4-25 to ensure minimum performance standards are met. Should PS1 fail to meet minimum performance standards, perform steps (2) through (11) below.

(2) Set C-6290(P)/APX (AN/APM-239) MASTER to OFF.

(3) Disconnect power cable (part number 4023655-0501, figure 4-11) from PS1P2 and XPS1P2 in troubleshooting setup of figure 4-12.

(4) Perform step d. of paragraph 4-21 and remove PS1.

(5) Perform steps 1. and 2. of paragraph 4-21 ac. , remove cover and clamp from PS1.

(6) Connect load bank (figure 3-1) to PS1P2 using power cable disconnected in step (3) above.

(7) Connect load bank ground to PS1TP1 ground.

(8) Connect cable assembly, power supply test (part number 4023656-0501, figure 4-11) between PS1P1 and XPS1P1.

(9) Connect differential voltmeter, MIL-V-9989 to TP1 and TP2 of load bank (figure 3-1) .

WARNING

Lethal voltages are present in PS1 and load bank when primary power is applied. These voltages are present on Al of P2 in load bank and the associated resistors, wiring, and on terminal Al of the open power supply.

(10) Set C-6280(P)/APX (AN/APM-239) MASTER to STBY for 1 minute then to NORM.

(11) Perform troubleshooting procedures of table 4-33.

(j) To reassemble and/or replace PS1, use procedures of paragraph 4-332., steps 44. and 45., and paragraph 4-33aa.

Table 4-30. Circuitboard Subassemblies Voltage Measurements

CIRCUIT \ PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
A1 PROCESSOR	NC	*	NC	NC	NM	+25V DC	NC	NC	GND	NC	NM	GND	KEY	GND	NC	NC	NC	NC	*	NC	NC	NM	--	--	--	--	--	--	--	--	--	--	--
A2 DECODER	NM	NM	NM	NM	NC	NC	NC	NC	NC	NC	NC	NC	KEY	NC	NM	NM	GND	NC	NC	NM	NM	NC	NC	NM	NM	NC	NC	NC	GND	NC	NM	NC	NC
A3 MODE 4	NM	GND	NM	+12V DC	NC	*	NC	NC	+12V DC	NC	NC	NM	NC	GND	NC	NC	NC	NM	NC	NM	KEY	GND	--	--	--	--	--	--	--	--	--	--	--
A4 ENCODER CLOCK	NM	NM	NM	NM	KEY	NM	NM	GND	NM	NM	NM	NM	NM	NM	NM	NC	NM	NM	NC	-3V	NC	GND	--	--	--	--	--	--	--	--	--	--	--
A5 ENCODER CONTROL	GND	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	+12V DC	NM	KEY	NC	NM
A6 ENCODER GATING	GND	NC	NC	NC	NC	NM	KEY	NC	NM	NM	NM	GND	NM	NM	NM	NM	NM	NC	NM	NM	NM	GND	--	--	--	--	--	--	--	--	--	--	--

CIRCUIT \ PIN	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z											
A1 PROCESSOR	NC	NM	-6V DC	NM	NM	NM	+12V DC	+6V DC	NM	NC	NC	NC	KEY	NC	NC	NC	NC	NC	NC	NC	NM	NM											
A2 DECODER	GND	NM	NM	NM	GND	NM	NC	NM	NC	NM	+25V DC	NC	KEY	NM	NC	NC	NM	-6V DC	NC	NC	NM	NC	--	--	--	--	--	--	--	--	--	--	--
A3 MODE 4	+12V DC	NM	-6V DC	NM	NC	+6V DC	+28V DC	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	*	NM	KEY	NM	+6V DC	NM	NM	+12V DC	NM	NM	NM	NM	NC	NC	NC
A4 ENCODER CLOCK	NM	NM	NM	NM	KEY	NM	-6V DC	-3V DC	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NC	NM	NC	NM	--	--	--	--	--	--	--	--	--	--	--
A5 ENCODER CONTROL	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	NC	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	--	--	--	--	--	--	--	--	--	--	--
A6 ENCODER GATING	GND	NC	+25V DC	NC	NC	NM	KEY	NM	NM	-6V DC	NM	GND	NM	+12V DC	NM	NM	NM	NC	NC	-3V DC	NM	GND	NC	NM	NM	NM	NM	NM	-6V DC	NM	KEY	NM	NM

NM - not measured
NC - no connection

*NC RT-859/APX-72
*NM RT-859A/APX-72

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure

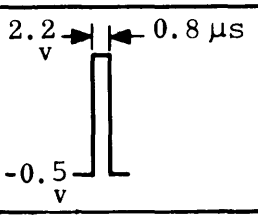
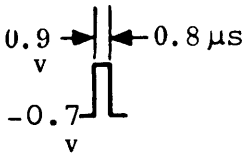
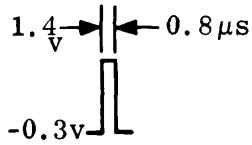
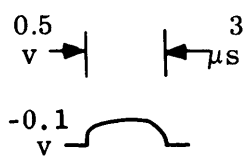
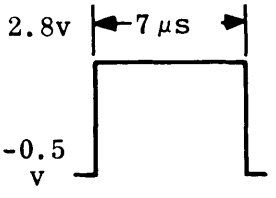
CIRCUIT CARD: Processor (A1) (RT-859/APX-72)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output TP2			OPERATIONS:	Mode C, Code 0000, MASTER to STBY, MTL-87 dbv
1.	A1TP2		No Signal Go to step 2	Go to step 5
2.	A1TP3		No Signal Go to step 3	Go to step 4
3.	A1TP6		No Signal Check transistors Q18, Q19, Q20, and associated circuitry	Check 0.280 µsec delay DL1 and diode CR3
4.	A1TP4		No Signal Check transitors Q1, Q2, Q3, Q5, Q26, Q28, Q29, Q30, Q31, and associated circuitry	Signal normal and TP3 > TP4 Check µA 710 A1 and transistor Q15
5.	A1TP5		No Signal Go to step 6	Go to step 8

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

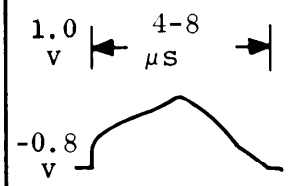
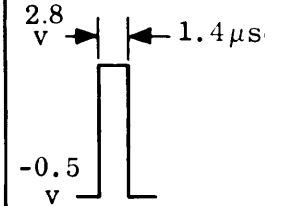
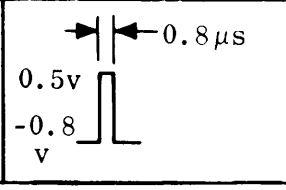
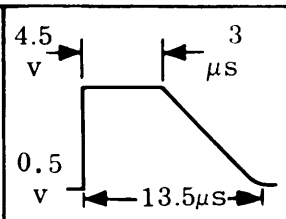
CIRCUIT CARD: Processor (A1) (RT-859/APX-72) (Cont)					
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION		NORMAL INDICATION
FUNCTION/SYMPTOM: No Output TP2			OPERATIONS:		Mode C, Code 0000, MASTER to STBY, MTL-87 dBv
6.	μA 710 A3-2		No Signal Check transistors Q24, Q27, Q4, capacitor C23, zener diode VR2, and associated circuitry		
7.	μA 710 A3-3		Incorrect dc level Adjust resistor R25; check diodes CR12, CR13, and terminal Y μA 710 positive		Correct level with pin A3-2 > A3-3 Check μA 710 3A and transistor Q17
8.	μA 710 A2-7		No Signal Go to step 9		Go to A1TP1
9.	μA 710 A2-2		No Signal Check transistor Q16 and diodes CR7 and CR16		Signal with A2-2 > A1TP4 Replace μA 710 A2
FUNCTION/SYMPTOM: No Output TP1, TP2 OK			OPERATIONS:		Mode C, Code 0000, MASTER to STBY, MTL-40 dBv
1.	A1TP4		Incorrect Signal Go to step 2		Go to terminal 5

Table 4-31. Functional Troubleshooting Chart,
Extender Board Procedure (Cont)

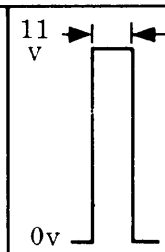
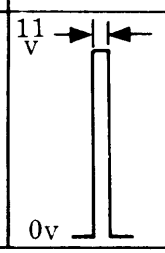
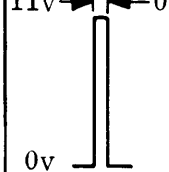
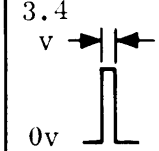
CIRCUIT CARD: Processor (A1) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output TP1, TP2 OK			OPERATIONS:	Mode C, Code 0000, MASTER to STBY, MTL-40 dbv
2.	Collector Q10		No Signal Go to step 3	Check diode CR6, transitor Q4, and resistor R10
3.	A1TP1		No Signal Check transistors Q9, Q11, Q12, and diode CR9	Check transistor Q10, diode CR4, and capacitor C10
FUNCTION/SYMPTOM: No Output Terminal 5, TP1 OK			OPERATIONS:	Mode C, Code 0000, MASTER to STBY, MTL-40 dbv
1.	Terminal 5		No Signal Go to step 2	
2.	Collector Q23		No Signal Check transistors Q21, Q22, Q23, and diode CR1	Check transistors Q13, and Q14

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

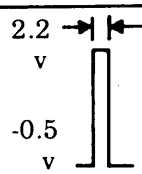
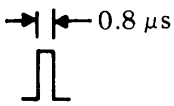
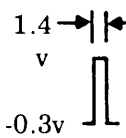
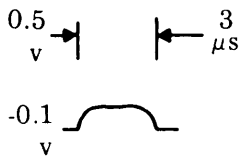
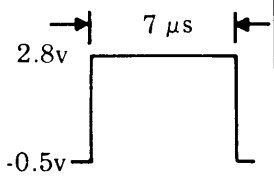
CIRCUIT CARD: Processor (A1) (RT-859A/APX-72)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output TP1			OPERATIONS:	Mode C, Code 0000, MASTER to STBY, MTL-87 dBv
1.	A1TP2		No signal Go to step 2.	Go to step 5.
2.	A1TP3		No signal Go to step 3.	Go to step 4.
3.	A1TP6		No signal Check A1, Q1, and associated circuitry.	Check DL1, CR3, and CR4.
4.	A1TP4		No signal Check A2, Q2, Q5, Q6, Q9 through Q14, Q31, and associated circuitry.	Signal normal and TP3 > TP4 in relative voltage Check A3, and A5.
5.	A1TP5		No signal Go to step 6.	Go to step 8.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

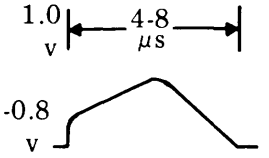
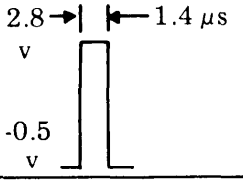
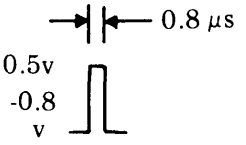
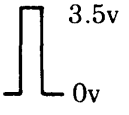
CIRCUIT CARD: Processor (A1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output TP1			OPERATIONS:	Mode C, Code 0000, MASTER to STBY, MTL-87 dBv
6.	A4-12		No signal Check Q7, Q8, Q12, Q15, and associated circuitry.	Go to step 7.
7.	A4-13		Incorrect dc level Adjust R25; check diodes CR17, CR18, and terminal Y.	Correct level with pin A3-2 >A3-3. Check A4 and A5.
8.	A3-8		No signal Go to step 9.	Go to step 10.
9.	A3-5		No signal Check CR7 and CR8.	Signal with A2-2 > A1TP4 Replace A3.
10.	A6-11		No signal Check appropriate segments of A5, A6, and A7.	Go to next sequence of tests.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

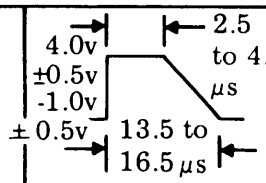
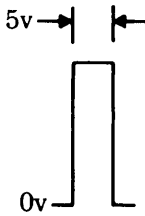
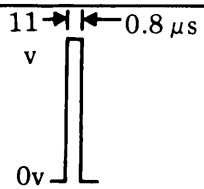
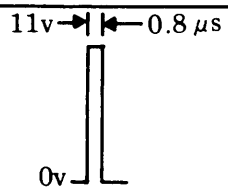
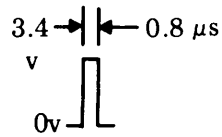
CIRCUIT CARD: Processor (A1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output TP1, TP2 OK			OPERATIONS:	Mode C, Code 0000, MASTER to STBY, MTL-40 dBv
1.	A1TP4		Incorrect signal Go to step 2.	Go to step 3.
2.	Collector Q28		No signal Go to step 3.	Check appropriate parts of A5, A7, CR24, CR25, Q11 and Q12.
3.	A1TP1		No signal Check Q29, and Q30.	Check Q28, C11, CR21.
FUNCTION/SYMPTOM: No Output Terminal 5, TP1 OK			OPERATIONS:	Mode C, Code 0000, MASTER to STBY, MTL-40 dBv
1.	Terminal 5		No signal Go to step 2.	
2.	Collector Q21		No signal Check Q19, Q20, Q21, CR16, CR23, CR26, and Q17.	Check Q23, and Q24.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

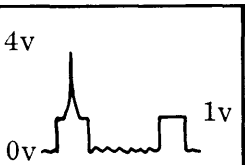
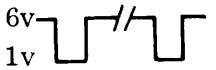
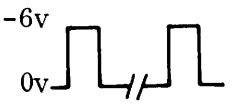
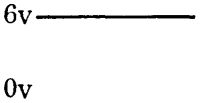
CIRCUIT CARD: Decoder (A2)			Reference figures 6-8 and 6-28 or 6-9 and 6-29	
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Mode Decode Strobe			OPERATIONS:	Mode 2 and as required Code 7777, MASTER to STBY
1.	A2TP4 or collectors of Q2, Q20, Q22, or Q31		No signal at A2TP4. Check collectors of other mode inputs interrogating in corresponding mode. Go to step 2.	Go to step 3.
2.	Collectors Q8, Q1, Q19, Q21, or Q30		No signal Replace Q8, Q1, Q19, Q21, or Q30 as applicable.	Replace Q9, Q2, Q20, Q22, or Q31 as applicable.
3.	A2TP8		No signal in mode being interrogated. Go to step 4.	Go to step 14.
4.	A2TP5		8.0 vdc Go to step 5.	Go to step 6.
5.	Collector Q23 (Momentarily ground A2TP5)		Ground Replace transistor Q23.	Replace transistor Q24.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Mode Decode Strobe			OPERATIONS:	Mode 2 and as required Code 7777, MASTER to STBY
6.	A2TP3	0.2v 0v	8.0 vdc Go to step 7.	Go to step 8.
7.	Collector Q42	6.4v 0v	0.2 vdc Go to step 8.	Replace transistor Q43.
8.	Base Q42	0.7v -1.0v	Positive vdc Go to step 9.	Replace transitor Q42.
9.	A2TP1	24v 0v	24 vdc Go to step 10.	Go to step 12.
10.	Base Q41	24.6v 0v	24 vdc Go to step 11.	Replace transistor Q41.
11.	Base Q40	25v 24.3v	25 vdc Replace transistor Q37, capacitor C43 as applicable.	Replace transitor Q40.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Mode Decode Strobe			OPERATIONS:	Mode 2 and as required Code 7777, MASTER to STBY
12.	Collector Q26	0.2v 0v	11.5 vdc Go to step 13.	
13.	Base Q26	0.7v -5.0v	No signal Replace capacitor C27 or transistor Q25.	Replace transitor Q26.
14.	Base Q32	0.7v -0.5v	No signal Go to step 15.	Replace transistor Q32.
15.	Collector Q45	8v 0v	No signal Replace transistor Q45.	Check diodes CR31, CR32, CR39, resistor R108 and replace as required.
16.	A2TP7	6v 0v	No signal Go to step 17.	Replace diodes CR25 through CR29 as applicable.
17.	Base Q33	0.7v -4.2v	No signal Replace transistor Q34.	Replace transistor Q33.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

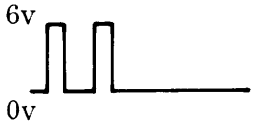
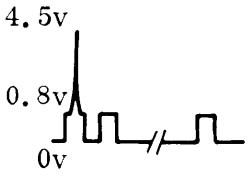
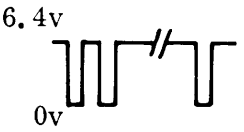
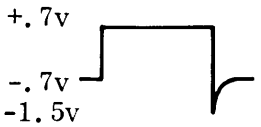
CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Suppression With ISLS Input			OPERATIONS:	Mode 2, Code 0000, ISLS Pulse, MASTER to NORM
1.	A2TP5		No signal Go to step 3.	Go to step 2.
2.	Collector Q32		No signal Go to step 3.	Replace diodes CR40 through CR43 as applicable.
3.	Collector Q36		No signal Go to step 4.	Go to step 5.
4.	Collector Q35		No signal Replace transistor Q35.	Replace transistor Q36.
5.	Base Q23		No signal Replace diode CR15, capacitor C22, or resistor R66 as applicable.	Replace transistors Q23, Q24, or Q44 as applicable.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

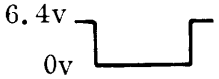
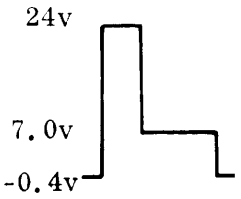
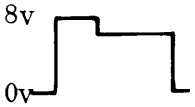
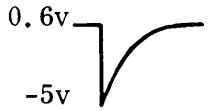
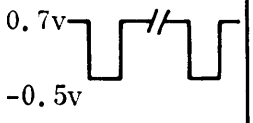
CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Generation of Internal Suppression During Replies (Modes 1,2,3/A,C and test)			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
1.	A2TP3		No signal Go to step 2.	Go to step 6.
2.	Collec-Q42		No signal Go to step 3.	Replace transistor Q43.
3.	Junction CR35, CR36, and CR37		No signal Go to step 4.	Replace transistor Q42.
4.	Collec-tor Q26		No signal Go to step 5.	Replace diode CR35.
5.	Base Q26		No signal Replace transistor Q25, capacitor C27 or diode CR16 as applicable	Replace transistor Q26.
6.	Base Q32		No signal Replace diode CR32.	Replace transistor Q32 or diodes CR40 through CR43 as applicable.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Generation of External Suppression During Replies (Modes 1,2,3/A,C and test)			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
1.	A2TP1	24v 0v	No signal Go to step 2.	
2.	Collector Q40	25v 0v	No signal Go to step 3.	Replace transistor Q41.
3.	Base Q40	25v 24.3v	No signal Replace transistor Q37.	Replace transistor Q40.
FUNCTION/SYMPTOM: No Generation of Internal and External Suppression (Mode 4 Replies)			OPERATIONS:	Mode 4 Replies
1.	A2TP3	8v 0v	No signal Go to step 2.	
2.	Collector Q42	6.4v 0v	No signal Go to step 3.	Replace transistor Q43.
3.	Junction CR35, CR36, and CR37	24v 7.0v -0.4v	No signal Go to step 4.	Replace transistor Q42 or resistor R130.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Generation of Internal and External Suppression (Mode 4 Replies)			OPERATIONS:	Mode 4 Replies
4.	A2TP1	24v 0v	No signal Go to step 5.	Replace diode CR36.
5.	Collector Q40	25v 0v	No signal Go to step 6.	Replace transistor Q41.
6.	Base Q40	25v 24.3v	No signal Go to step 7.	Replace transistor Q40.
7.	Emitter Q38	12v 0v	No signal Replace transistor Q38.	Replace transistor Q39.
FUNCTION/SYMPTOM: No AOC Bias Output From Reply Rate Integrator			OPERATIONS:	Mode 2, Code 0000, STBY, PRF 3000 pps MTL-84 dBv
1.	A2TP2	8v 0v	No signal Go to step 2.	
2.	Base Q18	8.0v 0v	Ground Replace diode CR12 or resistors R57, R58 as applicable	Go to step 3.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

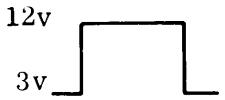
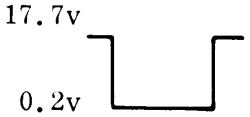
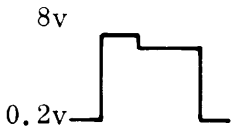
CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC Bias Output From Reply Rate Integrator			OPERATIONS:	Mode 2, Code 0000, STBY, PRF 3000 pps MTL-84 dBv
3.	Base Q17	Dc voltage more negative than base of Q18.	9.5 vdc Go to step 4.	Replace transistor Q17 or Q18 as applicable.
4.	Collector Q28	Dc voltage more negative than base of Q18.	9.5 vdc Go to step 5.	Replace diode CR11.
5.	Base Q29	Adjustable dc 1 to 8 VDC	Ground R89 not effective. Replace diode CR44, resistors R88, R89, R90 or transistor Q29 as applicable.	Go to step 6.
6.	Base Q28	Dc voltage more positive than base Q29.	No Go to step 7.	Replace transistors Q28 or Q29 as applicable.
7.	Collector Q27		No signal Go to step 8.	Replace transistor Q49, capacitor C28, or resistor R83 as applicable.
8.	Collector Q47		No signal Go to step 9.	Replace transistor Q27.
9.	Collector Q26		No signal Go to step 10.	Replace Transistor Q47.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

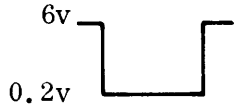
CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC Bias Output From Reply Rate Integrator			OPERATIONS:	Mode 2, Code 0000, STBY, PRF 3000 pps, MTL-84 dBv
10.	Collector Q25		No signal Replace transistor Q25.	Replace transistor Q26.
FUNCTION/SYMPTOM: No AOC Bias Output From Duty Cycle Integrator			OPERATIONS:	Mode 2, Code 7777, NORM PRF 1800 pps, MTL-84 dBv
1.	A2TP2		No signal Go to step 2.	
2.	Base Q18		Ground Replace diode CR12 or resistors R57, R58, as applicable.	Go to step 3.
3.	Base Q17	Dc voltage more negative than base of Q18.	No Go to step 4.	Replace transistor Q17 or Q18 as applicable.
4.	Collector Q15	Dc voltage more negative than base of Q18.	No Go to step 5.	Replace diode CR9.
5.	Base Q16	Adjustable dc 1 to 8 VDC.	Ground R89 not effective. Replace diode CR10, resistors R50, R51, R52, or transistor Q16 as applicable.	Go to step 6.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

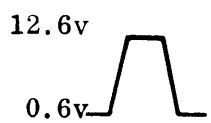
CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC Bias Output From Duty Cycle Integrator			OPERATIONS:	Mode 2, Code 7777, NORM PRF 1800 pps, MTL-84 dBv
6.	Base Q15	Dc voltage more positive than base of Q16	No Go to step 7.	Replace transistor Q15.
7.	A2TP6		No signal Replace transistor Q13 or associated component as applicable.	Replace transistor Q14.
FUNCTION/SYMPTOM: No AOC Bias Output From SLS Rate Integrator			OPERATIONS:	Mode 2, Code 0000, STBY *PRF 8000 pps, MTL-87 dBv, ISLS Input
1.	A2TP2		No signal Go to step 2.	
2.	Base Q18		Ground Replace diode CR12 or resistor R57 as applicable.	Go to step 3.
3.	Base Q17	Dc voltage more negative than base Q18.	9.7 vdc Go to step 4.	Replace transistors Q17 or Q18 as applicable.
4.	Collector Q11	Dc voltage more negative than base Q18.	9.7 vdc Go to step 5.	Replace diode CR8.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

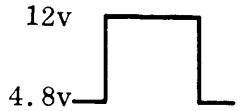
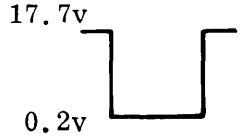
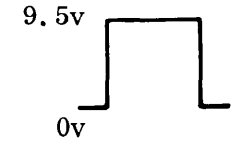
CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC Bias Output From SLS Rate Integrator			OPERATIONS:	Mode 2, Code 0000, STBY *PRF 8000 pps, MTL-87 dBv, ISLS Input
5.	Base Q12		Ground Replace diode CR3, resistors R39, R40 as applicable.	Go to step 6.
6.	Emitter Q48	Dc voltage more positive than base Q12.	No Go to step 7.	Replace transistors Q11 or Q12 as applicable.
7.	Collector Q10		No signal Go to step 8.	Replace transistor Q48, capacitor C15, or resistor R35 as applicable.
8.	Collector Q46		No signal Go to step 9.	Replace transistor Q10.
9.	A2TP5		No signal Follow procedures for NO SUPPRESSION WITH ISLS INPUT.	Replace transistor Q46.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Decoder (A2) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC Bias Output From SLS Rate Integrator			OPERATIONS:	Mode 2, Code 0000, STBY *PRF 8000 pps, MTL-87 dBv, ISLS Input

*Note: To obtain a PFR of 8000 ±300 pps using the AN/UPM-98A, modify the troubleshooting test setup of figure 4-12 as follows:

1. Disconnect cable to TEST WORD (AN/APM-239) and connect to AN/UPM-98A,VARI OUTPUT (SIF CODER); disconnect cables at both ends of coax tee on DELAYED TRIGGERS (XTAL MARK & SYNC); connect two jumper cables to this coax tee: connect end of one jumper cable to 0 TRIGGER and connect end of second cable to trigger input (SIF CODER). Connect probe of AN/UPM-140B to A2TP5 on RT-859/APX-72.

2. On SIF CODER set CODE A to 1, CODES B, C, +D to 0, SUB PULSE SELECT to A1, SUP PULSE POS to -1.0, FUNCTION to N, LEVEL to LO. On XTAL MARK &SYNC set SYNC SELECT to INT, TRIGGER DELAY RANGE TO 50-750. On INTERROGATION CODER set FUNCTION SELECT to MOD LOW.

3. Adjust PRF control on AN/UPM-98A for a pulse spacing of 120 to 130 us as observed on AN/USM-140B.

4. Return test setup to configuration of figure 4-12 upon completion of procedures in this table.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72)				Reference figures 6-10 and 6-30
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: Incorrect Coder/Decode Start Pulse			OPERATIONS: Mode 4	
1.	A3TP7	4.8v 0v 	5 vdc no pulse Go to step 2.a.	Go to step 5.
2.a.	A2-3 (946)	3.6v 0v 	Go to step 2.b.	
2.b.	A2-6	3.6v 0v 	Go to step 2.c.	
2.c.	A2-8	3.6v 0v 	Go to step 2.d.	
2.d.	A2-11	3.6v 0v 	Go to step 3.a.	Replace A3.
3.a.	A1-3 (141)	4.7v 3.7v 0v 	Go to step 3.b.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

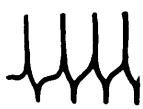
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: Incorrect Coder/Decode Start Pulse			OPERATIONS: Mode 4	
3.b.	A1-7	3.6v 0v 	Go to step 3.c.	
3.c.	A1-11	3.6v 0v 	Go to step 3.d.	
3.d.	A1-14	4.2v 3.6v 0v 	Go to step 4.a.	Replace A2.
4.a.	A1-1 (141)	4.4v 0v 1v 	Check capacitor C1 and resistors R1 and R2. Replace as required. Go to step 4.b.	
4.b.	A1-5	1.6v 0v 	Check capacitor C2 and resistors R3 and R4. Replace as required. Go to step 4.c.	
4.c.	A1-8	1.6v 0v 	Check capacitor C3 and resistors R5 and R6. Replace as required. Go to step 4.d.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

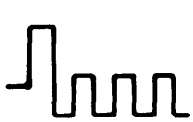
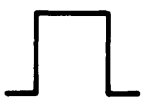
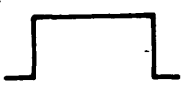
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: Incorrect Coder/decode Start Pulse			OPERATIONS: Mode 4	
4.d.	A1-12	1.6v 0.5v 0v 	Check capacitor C4 and resistors R7 and R8. Replace as required. Go to step 4.e.	Replace A1.
4.e.	A1-9	4.6v 0v	Replace A3.	
4.f.	A1-13	4v  0v	Go to step 6.	
5.	Collector Q34	9v  0v	Check transistors Q33, Q34, and associated components. Replace as required.	Go to step 6.
6.	Collector Q1	2.8v  0v	Check transistor Q1 and associated components. Replace as required.	Go to step 7.
7.	Collector Q8	4.7v  0v	Check transistor Q8 and associated components. Replace as required.	Go to step 8.
8.	Collector Q9	4.5v  0v	Check transistor Q9 and associated components. Replace as required.	Replace transistor Q10.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

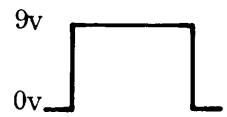
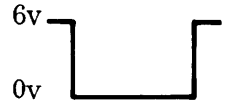
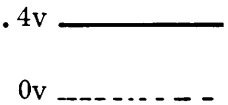
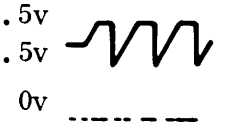
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC Output OPERATIONS: Mode 4, PRF 2300				
1.	A3TP6		Ground Replace transistor Q2.	Go to step 2.
2.	Collector Q3		6 vdc Replace transistor Q3.	Go to step 3.
3.	Collector Q4		Ground Replace transistor Q4.	Go to step 4.
4.	Collector Q5		Ground or slightly positive. Check transistor Q3, capacitor C2, diode CR3. Replace as required.	Go to step 5.
5.	Collector Q6		12 vdc Check transistor Q6, Q7, and diode CR5. Replace as required.	Check diode CR4. Replace as required.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

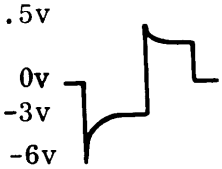
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Challenge Video			OPERATIONS: Mode 4	
1.	Collector Q17	4.5v 0v 	Go to step 2.	Replace transistor Q18.
2.	Collector Q16	5.5v 0.5v 	Check capacitor C22, resistors R55, R56, and diode CR7. Replace as required.	Check capacitors C23, C24, resistor R60, and transistor Q17. Replace as required.
FUNCTION/SYMPTOM: No Mode 4 Replies			OPERATIONS: Mode 4	
1.	Collector Q35	12v 2v 	12 vdc Check transistor Q35, diode CR17, and μL 951 (A12). Replace as required.	Check diode CR6. Replace as required.
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
1.	A3TP1	3.5v 0v -3v -6v 	Collector Q22 at 5 or 3 vdc. Go to step 2.	Check transformer T1 and associated components. Replace as required.
2.	Collector Q20	6.2v 0v 	Ground Go to step 3.	Check transistors Q21, Q22, and associated components. Replace as required.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

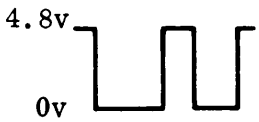
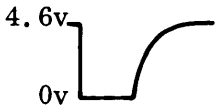
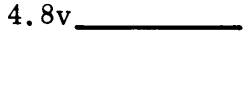
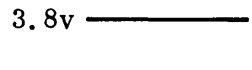
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
3.	A8-1 (951)		Ground Go to step 4.	Check transistors Q19, Q20, diode CR8, and associated components. Replace as required.
4.a.	A3TP2		Ground Go to step 4.b.	
4.b.	A3TP4		Go to step 5.a.	Replace μL 951 A8. Check associated components and replace as required.
5.a.	A3TP8		Ground Go to step 6.a.	Go to step 5.b.
5.b.	A7-11			Go to step 5.c.
5.c.	A7-10			Go to step 5.d.
5.d.	A7-8 A7-8 disconnected		4.6 vdc Replace μL 952 A7.	Go to step 5.e.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

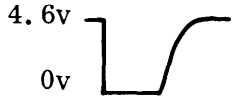
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS: Mode 4, MASTER to STBY, PRF 1000 pps	
5.e.	A3TP2 A9-5,6 disconnected		4.6 vdc Replace μL 950 A9	Go to step 5.f.
5.f.	A3TP2 A10-3 disconnected		4.6 vdc Replace μL 951 A10	Go to step 5.g.
5.g.	A3TP2 A8-3 disconnected		4.6 vdc Replace μL 951 A8	
6.a.	A4-6		Ground Go to step 6.b.	Go to step 6.c.
6.b.	A4-6 A4-1 disconnected		Ground Replace μL 951 A4.	Replace μL 950 A6. Go to step 7.a.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

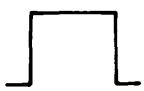
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
6.c.	A5-8 A5-8 disconnected	4.8v 0v 	Ground Replace μL 946 A5. Check capacitor C11, resistors R99, R110. Replace as required.	
7.a.	A3TP4	5v 0v 	Ground Go to step 8.a.	Go to step 7.b.
7.b.	A3TP3	5v 0v		Replace μL 951 A8.
8.a.	A12-3	4v 0v 		Go to step 8.b.
8.b.	A12-4	4.6v 0v 	5 vdc Check μL 946 A5 and associated components. Replace as required.	Go to step 8.c.
8.c.	A12-1 A12-1 disconnected	5v 0v 	5 vdc Check μL 951 A12 and associated components. Replace as required.	Go to step 8.d.

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
8.d.	A3TP4 A13-5,6 disconnected	5v 0v	5 vdc Replace μL 950 A13.	Go to step 8.e.
8.e.	A3TP4 A16-3 disconnected	5v 0v	5 vdc Replace μL 951 A16.	Go to step 8.f.
8.f.	A3TP4 A8-4 disconnected	5v 0v	6 vdc Replace μL 951 A8.	
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
1.	A3TP3 Single pulse 4 interrogations in 33 MS.	5v 0v	Ground Check diode CR12 and replace if required. Go to step 2.a.	Go to step 5.a.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

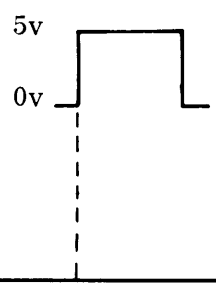
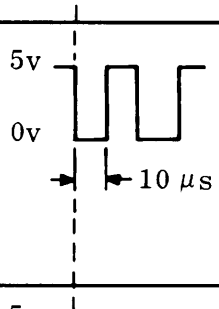
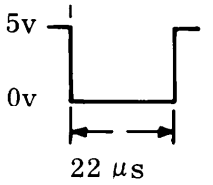
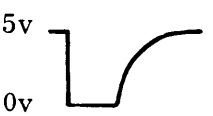
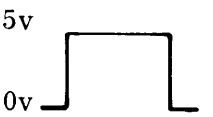
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
2.a.	A10-6 (951) Single pulse 4 interrogations in 33 MS.		Go to step 3. Ground	Go to step 2.b.
2.b.	A9-10,11 Single pulse 4 interrogations in 33 MS.		Go to step 2.c.	Go to step 2.c.
2.c.	A11-70,11 Single pulse 4 interrogations in 33 MS.		Ground Go to step 5.a.	Replace μL 951 A7.
3.	A3TP2			Go to step 4.
4.	A10-6 A10-6 disconnected.		Ground Replace μL 951 A10. Check associated components and replace as required.	

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

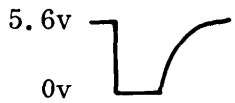
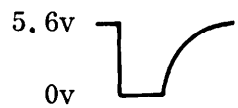
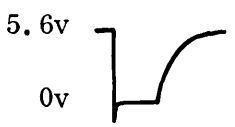
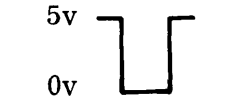
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
5.a.	Collector Q32		Ground Check transistor Q32 and associated components. Replace as required.	Go to step 5.d.
5.b.	Collector Q32 A11-1 disconnected		Ground Go to step 5.c.	
5.c.	Collector Q32 A9-1 disconnected			Replace μL 950 A9.
5.d.	A11-10, 11 A11-10, 11 disconnected		Ground Go to step 5.e.	
5.e.	A11-5,6			Replace μL 950 A11.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

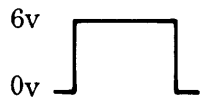
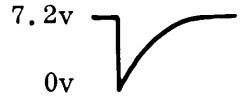
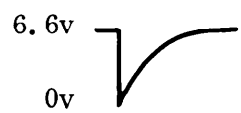
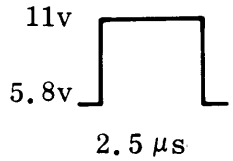
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
6.	Collector Q11		Ground Replace transistor Q11.	Go to step 7.
7.	Collector Q12 Single pulse 4 interrogations in 33 MS		7.2 vdc Check transitor Q12 and associated components. Replace as required.	Go to step 8.
8.	Emitter Q13 Single pulse 4 interrogations in 33 MS		Ground Replace transistor Q13.	Go to step 9.
9.	Collector Q14 Single pulse 4 interrogations in 33 MS		6 vdc Replace transistor Q14.	Go to step 10.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

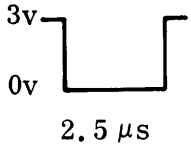
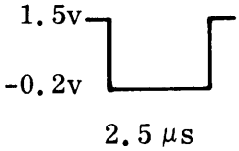
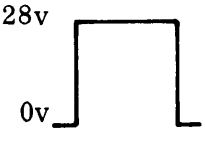
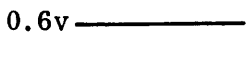
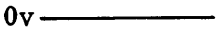
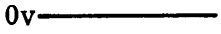
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
10.	Collector Q15 Single pulse 4 interrogations in 33 MS		2 vdc Replace transistor Q15.	Go to step 11.
11.	Emitter Q23 Single pulse 4 interrogations in 33 MS		Ground Replace transistor Q23.	Go to step 12.
12.	Collector Q24		Ground Replace transistor Q24.	Go to step 13.
13.	Collector Q15 ZERO M4		2 vdc Go to step 14	
14.	Cathode diode CR9		6 vdc Go to step 15.	Replace diode CR9.
15.	Terminal B			Replace inductor L1.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

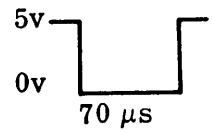
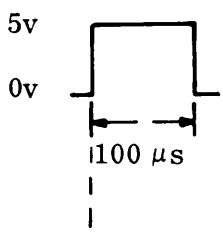
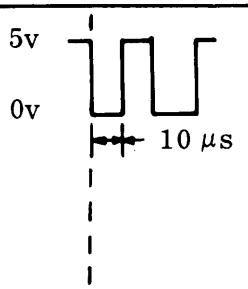
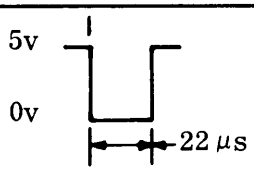
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
1.	A3TP5 Single pulse 4 interrogations in 33 MS		Ground Go to step 2.a.	Check diode CR11. Replace if required. Go to step 5.
2.a.	A16-6 Single pulse 4 interrogations in 33 MS		Ground Go to step 3.a.	Go to step 2.b.
2.b.	A13-10, 11 Single pulse 4 interrogations in 33 MS			Go to step 2.c.
2.c.	A14-10 11 Single pulse 4 interrogations in 33 MS		Ground or 5 vdc Go to step 4.a.	Replace μL 962 A7.
3.a.	A3TP4			Go to step 3.b.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

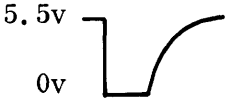
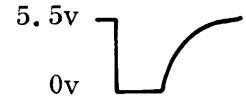
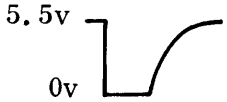
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
3.b.	A16-6 A16-6 disconnected		Ground Replace μL 951 A16. Check associated components and replace as required.	
4.a.	Collector Q31		Ground or 5.5 vdc Check transistor Q31 and associated components. Replace as required. Go to step 4.b.	Go to step 4.d.
4.b.	Collector Q31 A14-1 disconnected		Ground or 5.5 vdc Go to step 4.c.	
4.c.	Collector Q31 A9-1 disconnected			Replace μL 950 A13.
4.d.	A14-10, 11 A14-10, 11 disconnected		Ground or 5 vdc Go to step 4.e.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

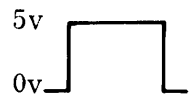
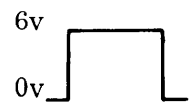
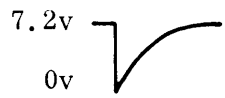
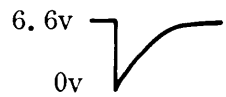
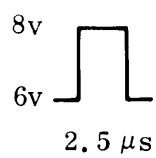
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
4.e.	A14-5,6 A14-10, 11 disconnected			Replace μL 950 A14.
5.	Collector Q25		Ground Replace transistor Q25.	Go to step 6.
6.	Collector Q26 Single pulse 4 interrogations in 33 MS		12 vdc Check transistor Q26 and associated components. Replace as required.	Go to step 7.
7.	Emitter Q27 Single pulse 4 interrogations in 33 MS		Ground Replace transistor Q27.	Go to step 8.
8.	Collector Q28 Single pulse 4 interrogations in 33 MS		6 vdc Replace transistor Q28.	Go to step 9.

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

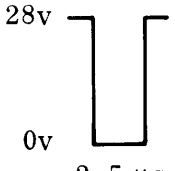
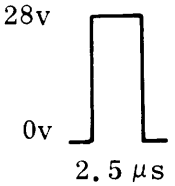
CIRCUIT CARD: Mode 4 (A3) (RT-859/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
9.	Collector Q29 Single pulse 4 interrogations in 33 MS		28 vdc Replace transistor Q29.	Go to step 10.
10.	Collector Q30 Single pulse 4 interrogations in 33 MS		Ground Replace transistor Q30.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

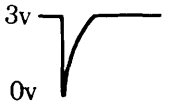
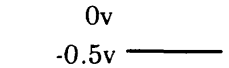
CIRCUIT CARD: Mode 4 (A3) (RT-859A/APX-72)				Reference Figures 6-11 and 6-31
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: Incorrect Decode Strobe			OPERATIONS: Mode 4	
1.	A3TP7		3.5 vdc, no pulse Go to step 2.	Go to next sequence of tests.
2.	A201-5		No pulse, or insufficient amplitude. Check R201, R202, and C201. Go to step 3.	Go to step 4.
3.	A202-12		+2v or higher. Check A204-8 (+6v) VR201, R240.	Check A202, and A201.
4.	A201-4		No pulse or insufficient amplitude. Check R203, R204, R205, and Q201.	Go to step 5.
5.	A201-1		No pulse or insufficient amplitude. Check R206, R207, R208, and Q202.	Go to step 6.
6.	A201-2		No pulse or insufficient amplitude. Check R209, R210, R211, and Q203.	Replace A201.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

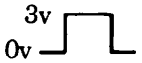
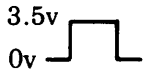
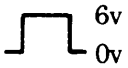
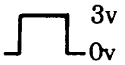
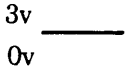
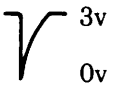
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Enable Trigger			OPERATIONS: Mode 4	
1.	Pin 20		No signal Go to step 2.	Go to next sequence of tests.
2.	Collector Q9		No signal Go to step 3.	Check Q10 and associated circuit.
3.	Collector Q8		No signal Go to step 4.	Check Q9, C9, and associated circuit.
4.	A202-3		No signal Go to step 5.	Check CR16, C7, Q8, and associated circuit.
5.	A202-1		No signal Check A203-8.	Go to step 6.
6.	A202-2		Improper level (0 vdc) Go to step 7.	Check A202.
7.	A6-1		No signal Check track.	Check A6 and associated circuit.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

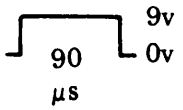
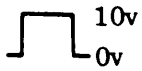
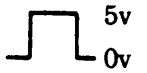
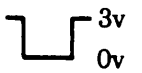
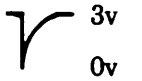
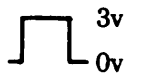
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: Incorrect SIF Suppression		OPERATIONS: Mode 4		
1.	Pin J		If improper width, adjust R215. No signal Go to step 2.	Go to next sequence of tests.
2.	Collector Q205		No signal Go to step 3.	Check Q206 and associated circuit.
3.	A203-6		No signal Check A203.	Check Q205 and associated circuit.
FUNCTION/SYMPTOM: Incorrect Three Pulse Decoder		OPERATIONS: Mode 4		
1.	A3TP6		No signal Go to step 2.	Go to next sequence of tests.
2.	A202-10		No signal Go to step 3.	Check A202 and associated circuit.
3.	A201-8		No signal Check A201.	Go to step 4. Check CR201.
4.	Collector Q213		No signal Check C202.	Check Q211.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

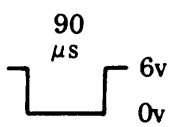
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC Output OPERATIONS: Mode 4				
1.	A202-3		Go to step 5, page 4-145. If improper width, adjust R215.	Go to step 2.
2.	Collector Q4		Ground Check Q4 and associated circuit.	Go to step 3.
3.	Emitter Q5		Ground, or slightly positive Check C2, CR3, Q5 and associated circuit.	Go to step 4.
4.	Collector Q6		12 vdc. Check Q6, Q7, CR5, and setting of R29	Check CR4.
FUNCTION/SYMPTOM: No Challenge Video OPERATIONS: Mode 4				
1.	A202-6		Too many pulses (4) Go to step 2. No signal, or 1v amplitude Go to step 3.	Check Q209, CR203 and associated circuit.
2.	A202-8		+5v Check A202-9 and 10.	Check CR207.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Challenge Video			OPERATIONS: Mode 4	
3.	A202-8		0 vdc Check A202.	Go to step 4.
4.	Collector Q207		No signal Go to step 5.	Check A202.
5.	Emitter Q210		No signal Go to step 6.	Check Q207, Q208, C207 and associated circuit.
6.	Base Q210		No Signal Check CR205,CR206, and A3DL1.	Check Q210
FUNCTION/SYMPTOM: No Mode 4 Replies			OPERATIONS: Mode 4	
1.	Collector Q35		12 vdc Check Q35, CR1, A12 and associated circuit.	Check CR6.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

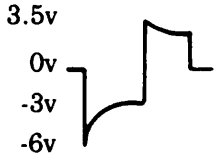
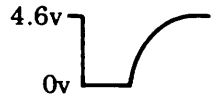
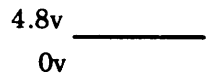
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
1.	A3TP1		Collector Q22 at 5 or 3 vdc Go to step 2.	Check transformer T1 and associated components. Replace as required.
2.	Collector Q20		Ground Go to step 3.	Check transistors Q21, Q22, and associated components. Replace as required.
3.	A8-1		Ground Go to step 4.	Check transistors Q19, Q20, diode CR8, and associated components. Replace as required.
4.	A3TP2		No signal Go to step 6.	Go to step 5.
5.	A3TP4		Go to step 6.	Replace A8. Check associated components and replace as required.
6.	A3TP8		Ground, no signal Go to step 13.	Go to step 7.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

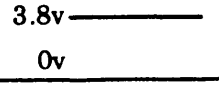
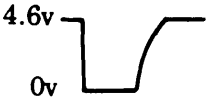
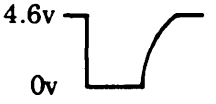
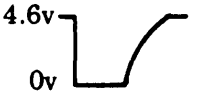
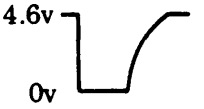
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
7.	A7-11		No signal Check A6 and interconnecting track.	Go to step 8.
8.	A7-10		No signal Check A15.	Go to step 9.
9.	A7-8 A7-8 disconnected		4.6 vdc Replace A7.	Go to step 10.
10.	A3TP2 A9-5,6 disconnected		4.6 vdc Replace A9.	Go to step 11.
11.	A3TP2 A10-3 disconnected		4.6 vdc Replace A10.	Go to step 12.
12.	A3TP2 A8-3 disconnected		4.6 vdc Replace A8.	Go to step 16.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

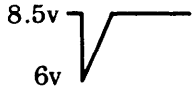
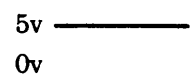
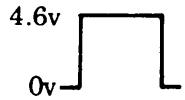
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
13.	A203-8		Ground Go to step 14.	Go to step 15.
14.	A203-1		Check C204, R222, R223 and associated components	Check A203 and associated components.
15.	A5-8 A5-8 disconnected		Ground Replace A5. Check capacitor C206, resistors R99 and R110. Replace as required.	N/A
FUNCTION/SYMPTON: No Audio Output			OPERATIONS:	Mode 4 MASTER to NORM, PRF 1000 pps
16.	A3TP4		No signal Go to step 18.	Go to step 17.
17.	A3TP2		N/A	Replace A8.
18.	A12-3		Examine track from terminal K.	Go to step 19.
19.	A12-4		Check A5 and associated components. Replace as required. Check for presence of modulation sample input.	Go to step 20.

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

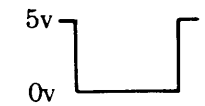
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
20.	A12-6 A12-6 disconnected		Check A12 and associated components. Replace as required.	Go to step 21.
21.	A3TP4 A13-5,6 disconnected		5 vdc Replace A13.	Go to step 22.
22.	A3TP4 A16-3 disconnected		Replace A16.	Go to step 23.
23.	A3TP4 A8-4 disconnected		Replace A8.	
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
1.	A3TP3 Single pulse 4 interrogations in 33 MS		Go to step 2.	Go to step 12.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

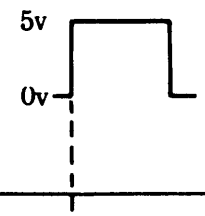
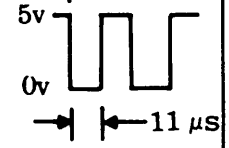
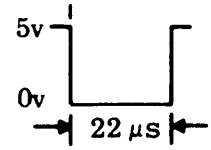
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
2.	A10-6 Single pulse 4 interrogations in 33 MS		Go to step 5.	Go to step 3.
3.	A9-10,11 Single pulse 4 interrogations in 33 MS		Go to step 4.	Go to step 4.
4.	A11-10,11 Single pulse 4 interrogations in 33 MS		Go to step 7.	Replace A7.
5.	A3TP2		N/A See previous procedures.	Go to step 6.
6.	A10-6 A10-6 disconnected		No signal Replace A10. Check associated components and replace as required.	Replace A7.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

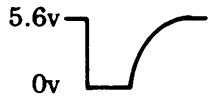
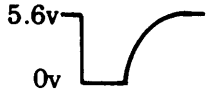
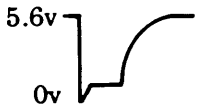
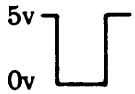
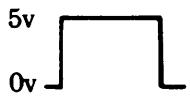
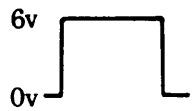
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
7.	Collector Q32		No signal Go to step 8.	Go to step 10.
8.	Collector Q32 A11-1 disconnected		Ground Go to step 9.	Replace A11.
9.	Collector Q32 A9-1 disconnected		Check Q32 and associated components.	Replace A9.
10.	A11-10,11 A11-10,11 disconnected		No signal Go to step 11.	Replace A7.
11.	A11-5,6		Replace A9.	Replace A11.
12.	Collector Q11		Ground Check CR12, Q11, and associated circuit.	Go to step 13.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

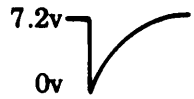
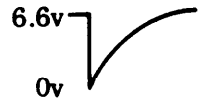
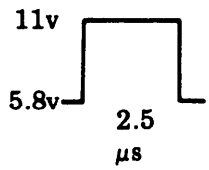
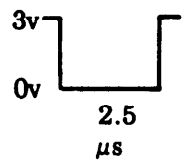
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
13.	Collector Q12 Single pulse 4 interrogations in 33 MS		7.2 vdc Check transistor Q12 and associated components. Replace as required.	Go to step 14.
14.	Emitter Q13 Single pulse 4 interrogations in 33 MS		Replace transistor Q13.	Go to step 15.
15.	Collector Q14 Single pulse 4 interrogations in 33 MS		Replace transistor Q14.	Go to step 16.
16.	Collector Q15 Single pulse 4 interrogations in 33 MS		2 vdc Replace transistor Q15.	Go to step 17.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

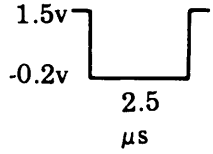
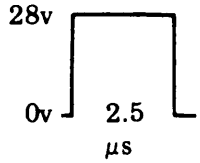
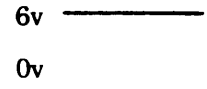
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS:	Mode 4, MASTER to STBY, PRF 1000 pps
17.	Emitter Q23 Single pulse 4 interrogations in 33 MS		Replace transistor Q23.	Go to step 18.
18.	Collector Q24		Ground Replace transistor Q24.	Go to step 19.
19.	Collector Q15 ZERO M4		2 vdc Go to step 20.	
20.	Cathode diode CR9		6 vdc Go to step 21.	Replace diode CR9.
21.	Terminal B			Replace inductor L1.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

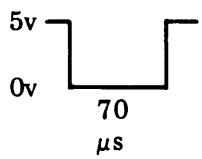
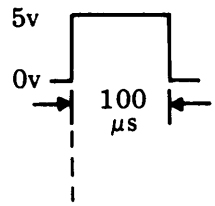
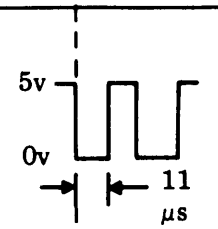
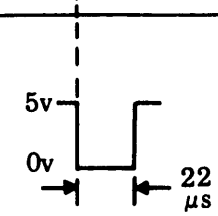
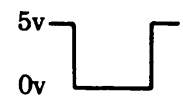
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
1.	A3TP5 Single pulse 4 interrogations in 33 MS		Go to step 2.	Go to step 12.
2.	A16-6 Single pulse 4 interrogations in 33 MS		Go to step 5.	Go to step 3.
3.	A13-10,11 Single pulse 4 interrogations in 33 MS		Go to step 5.	Go to step 4.
4.	A14-10,11 Single pulse 4 interrogations in 33 MS		Go to step 7.	Replace A7.
5.	A3TP4		N/A See previous procedures.	Go to step 6.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

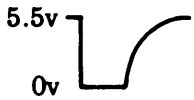
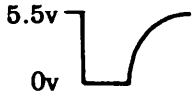
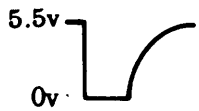
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
6.	A16-6 A16-6 disconnected		No signal Replace A16. Check associated components and replace as required.	Replace A7.
7.	Collector Q31		No signal Go to step 8.	Go to step 10.
8.	Collector Q31 A14-1 disconnected		No signal Go to step 9.	Replace A14.
9.	Collector Q31 A13-1 disconnected		Check Q31 and associated components.	Replace A13.
10.	A14-10,11 A14-10,11 disconnected		No signal Go to step 11.	Replace A7.
11.	A14-5,6		Replace A13.	Replace A14.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

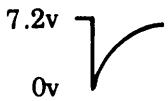
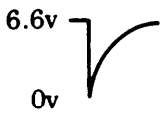
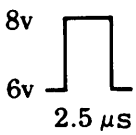
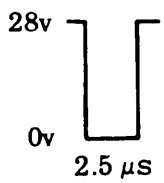
CIRCUIT CARD: Mode 4 (Part No. 4028683-0502) (A3) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
12.	Collector Q25		Ground Check CR11, Q25, and associated circuit.	Go to step 13.
13.	Collector Q26 Single pulse 4 interrogations in 33 MS		Check transistor Q26 and associated components. Replace as required.	Go to step 14.
14.	Emitter Q27 Single pulse 4 interrogations in 33 MS		Replace transistor Q27.	Go to step 15.
15.	Collector Q28 Single pulse 4 interrogations in 33 MS		Replace transistor Q28.	Go to step 16.
16.	Collector Q29 Single pulse 4 interrogations in 33 MS		28 vdc Replace transistor Q29.	Go to step 17.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

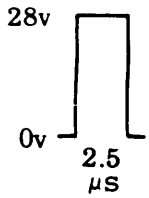
CIRCUIT CARD: Mode 4 (A3) (Part No. 4028683-0502) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS:	Mode 4, MASTER to NORM, PRF 1000 pps
17.	Collector Q30 Single Pulse 4 interrogations in 33 MS		Ground Replace transistor Q30.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

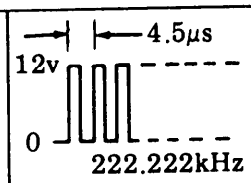
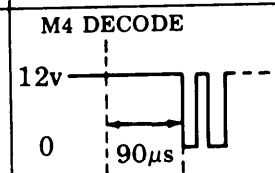
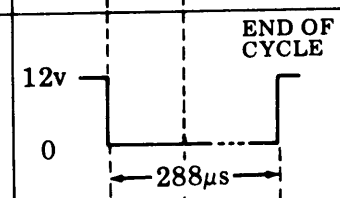
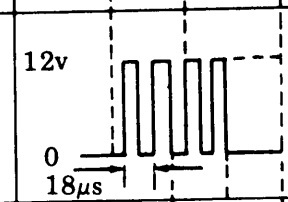
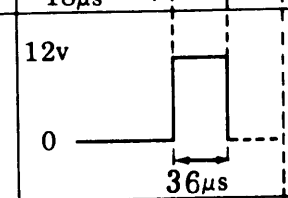
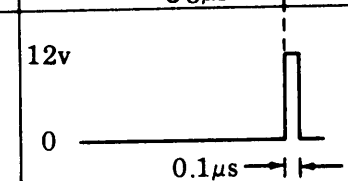
CIRCUIT CARD: Mode 4 (A3) (Part No. 116104-1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Mode 4 board Outputs.			OPERATIONS:	Mode 4, MASTER to STBY
1.	A3TP4		Check U16, Y1, C12, C13, R17, R26.	Go to step 2.
2.	U7D-11		Go to step 3.	Go to step 6.
3.	U8-2		Check U7, U15.	Go to step 4.
4.	U8-9		Check U8.	Go to step 5.
5.	U8-5		Check U8.	Check U7.
6.	A3TP5		Check U8.	Go to next sequence of tests.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

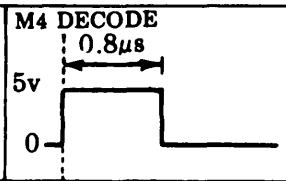
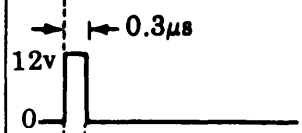
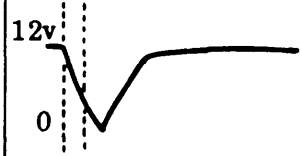
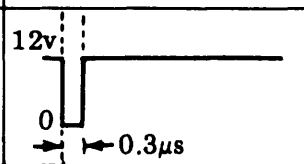
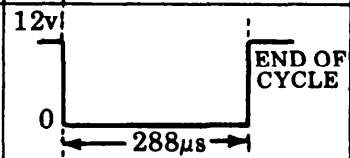
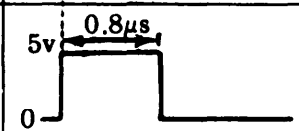
CIRCUIT CARD: Mode 4 (A3) (Part No. 116104-1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Enable Trigger			OPERATIONS:	Mode 4, MASTER to STBY
1.	Pin 20		Go to step 2.	Go to next sequence of tests.
2.	U18A-2		Go to step 3.	Go to step 4.
3.	U10D-8		Check U10, C10, R36.	Check U2, U10.
4.	A3TP6		Check U18, R34, R35, R41.	Go to step 5.
5.	A3TP8		Check U14, U18, U5, C6, R6.	Go to 6.
6.	U12E-11		Check U12, C5, R43.	Check Q8, R37, R51.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

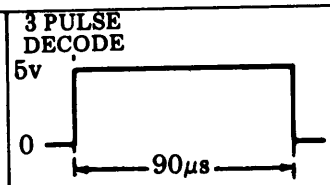
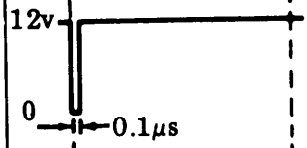
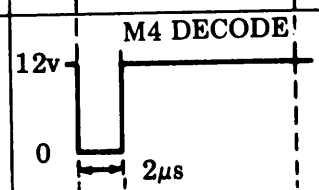
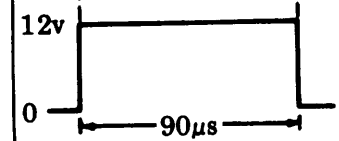
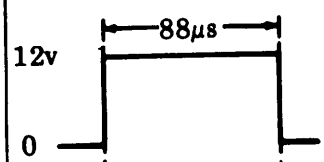
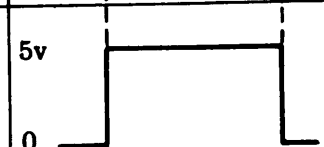
CIRCUIT CARD: Mode 4 (A3) (Part No. 116104-1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: Incorrect Ditch Lock			OPERATIONS:	Mode 4, MASTER to STBY
1.	Pin 6		Go to step 2.	Go to next sequence of tests.
2.	U4C-13		Check U4.	Go to step 3.
3.	U4C-11		Check U3.	Go to step 4.
4.	U4C-12		Check U15.	Go to step 5.
5.	A3TP2		Check U4.	Check U12, Q4, R22, R31.
FUNCTION/SYMPTOM: No SIF Suppression			OPERATIONS:	Mode 4, MASTER to STBY
1.	Pin J		Go to step 2.	Go to next sequence of tests.
2.	U7B-4		Check U7.	Check Q1, R9.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

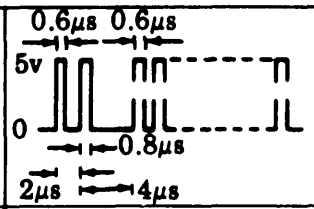
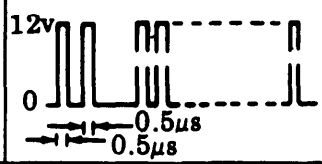
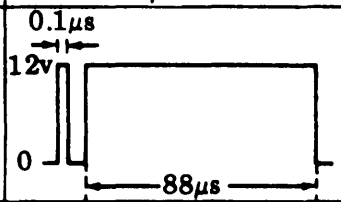
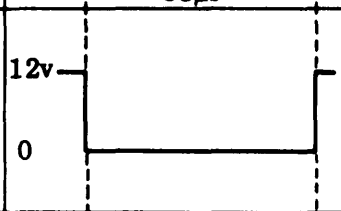
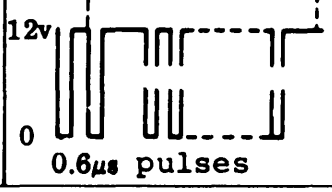
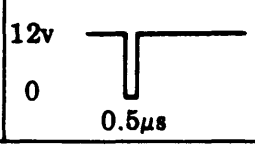
CIRCUIT CARD: Mode 4 (A3) (Part No. 116104-1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Challenge Video			OPERATIONS: Mode 4, MASTER to NORM	
1.	Pin V		Go to step 2.	Go to next sequence of steps.
2.	U14A-1		Check U13, U16, CR3, R24, R47.	Go to step 3.
3.	U14A-2		Go to step 4.	Go to step 5.
4.	U14B-6		Check U15.	Check U14.
5.	U3B-9		Check U3, C4, R5.	Check U4, U12, Q5, R32, R33, R50.
FUNCTION/SYMPTOM: No Response to Disparity			OPERATIONS: Mode 4, MASTER to NORM, DISPARITY to DL1	
1.	U13E-10		Check U13, R23, R25, CR3.	Check U15, U18.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Mode 4 (A3) (Part No. 116104-1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No AOC			OPERATIONS: Mode 4, MASTER to NORM, Interrogation rate to 2000 Hz	
1.	A3TP1	5.5v ———	Check U12, C11, R1, R12, R13.	Go to step 2.
2.	U11-10	7v ———	Check U11, R42, R44, VR2.	Check VR1, CR2, R39.
FUNCTION/SYMPTOM: No Replies			OPERATIONS: Mode 4, MASTER to NORM	
1.	Pin L	12v, 0, 4μs	Go to step 2.	Go to next sequence of tests.
2.	U2D-12	12v ———	Check U10, R45.	Go to step 3.
3.	U2D-11	12v, 0	Check U2, U13, U16, R16, R40, CR3.	Check U12.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

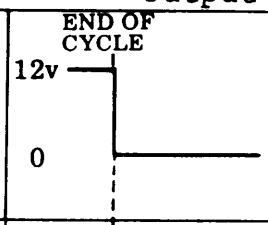
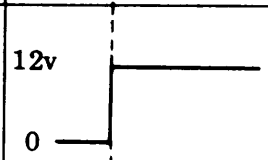
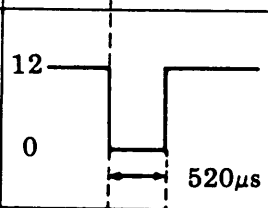
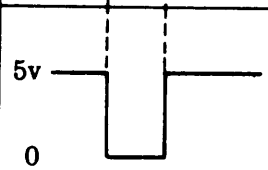
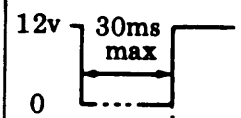
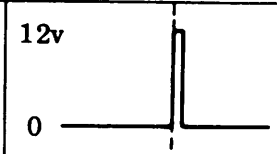
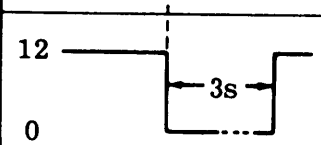
CIRCUIT CARD: Mode 4 (A3) (Part No. 116104-1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Audio Output			OPERATIONS: Mode 4, MASTER to STBY	
1.	U2D-8		Check U16.	Go to step 2.
2.	U5B-12		Check U2.	Go to step 3.
3.	A3TP3		Check U5, U13, R27, R14.	Go to step 4.
4.	BASE Q2		Check U12, R18, R19.	Check Q2, T1, C16, R1.
FUNCTION/SYMPTOM: No Caution Light			OPERATIONS: Mode 4, MASTER to STBY	
1.	U1A-7		Check U1, U10, C1, R3.	Go to step 2.
2.	U9B-11		Check U9.	Go to step 3.
3.	U2B-6		Check U2, U17, C15, R28.	Check U10, Q3, R21.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

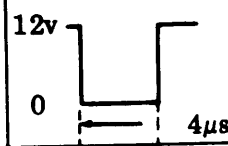
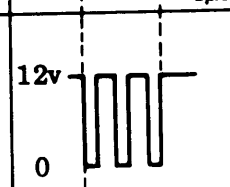
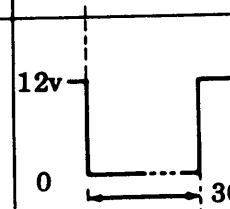
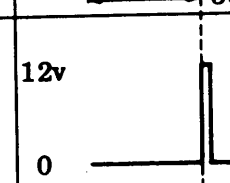
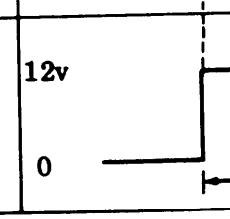
CIRCUIT CARD: Mode 4 (A3) (Part No. 116104-1) (RT-859A/APX-72) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reply Light			OPERATIONS: Mode 4, MASTER to NORM	
1.	A3TP7		Go to step 2.	Go to step 3.
2.	U6A-4		Check U13, CR1, R15, R49, VR2, CR3, R48.	Check U6, C8, C9, R7, R8.
3.	U1B-9		Check U1, U10, C2, R4.	Go to step 4.
4.	U9A-3		Check U9.	Go to step 5.
5.	U17A-6		Check U17, C14, R20.	Check Q6, Q7, R30, R38.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

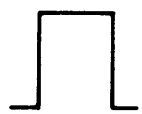
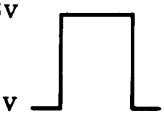
CIRCUIT CARD: Encoder Clock (A4)				Reference figures 6-12 and 6-32
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Modulator Trigger Output			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
1.	A4TP3	8v  0.8v	Ground Go to step 2.	Go to step 6.
2.	Base Q5	8v  1.5v	Ground Go to step 3.	Replace transistor Q5.
3.	A4TP1	1.5v  -6.0v -7.5v	Ground Go to step 4.	Check transistor Q4, diode CR77, resistor R10. Replace as required.
4.	Collector Q2	12v  1.8v	12 vdc Go to step 5.	Check transistor Q3, capacitor C5, diode CR4. Replace as required.

Table 4-31 Functional Troubleshooting Chart, Extender Borad Procedure (Cont).

CIRCUIT CARD: Encoder Clock (A4) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Modulator Trigger Output			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
5.	Collector Q16	12v 0.6v 	12 vdc Check transistor Q16 and associated components. Replace as required.	Check diodes CR1, CR10 as required.
6.	A4TP7	9v 8v 0v  29 pulses	Ground Go to step 7.	Go to step 10.
7.	Base Q7	0.6v .11v  30 pulses	Ground Check gated oscillator A4A1 or capacitor C7. Replace as required.	Go to step 8.
8.	Collector Q7	12v 0.6v  30 pulses	Ground Replace transistor Q7.	Go to step 9.
9.	Base Q9	7.8v 0v 	-0.5 vdc Replace transistors Q8, Q9, + dc Voltage. Check transistor Q14, capacitor C11, resistor R31. Replace as required.	Go to step 10.

Table 4-31. Functional Troubleshooting Chart
Extender Board Procedure (Cont)

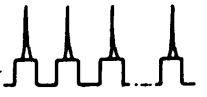
CIRCUIT CARD: Encoder Clock (A4) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Modulator Trigger Output			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
10.	A4TP6	12v  0.6v 15 pulses	Ground Go to step 11.	Go to step 13.
11.	Base Q11	0.6v  5.4v 15 pulses	Ground Go to step 12.	Replace transistor Q11.
12.	Collector Q18	11.1v  0.6v 15 pulses	Ground Isolate and check for a defective encoder counter. Replace as required.	Replace transistors Q10, Q11, capacitor C9. Replace as required.
13.	Emitter Q19	11v  0v 15 pulses	Ground Go to step 14.	Go to step 18.
14.	Base Q19	7v  0.8v 15 pulses	Ground Go to step 15	Replace transistor Q19.
15.	Collector Q25	11.1v  0.6v 8 pulses	Ground Check associated encoder counter and replace components as required.	Go to step 16.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

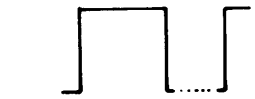
CIRCUIT CARD: Encoder Clock (A4) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Modulator Trigger Output			OPERATIONS:	Mode 2, Code 777, MASTER to NORM
16.	Collector Q35	11.1v  0.6v 4 pulses	Ground Check associated encoder counter and replace components as required.	Go to step 17. Go to step 17.
17.	Collector Q38	11.1v  0.6v 2 pulses	Ground Check associated encoder counter and replace components as required.	Check components associated with encoder matrix and replace as required.
18.	Base Q20	1.2v  -6v 15 pulses	Ground Check transistor Q20, resistor R60. Replace as required.	Go to step 19.
19.	Base Q21	0v -6v ———	Ground Check transistor Q21, resistor R62. Replace as required.	Go to step 20.
20.	Collector Q22	0.6v ——— 0v	12 vdc Go to step 21.	Check transistors Q20, Q21, diodes CR78, CR79. Replace as required.
21.	Collector Q40	12v ——— 0v	Ground Replace transistor Q40	Replace transistor Q22.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Encoder Clock (A4) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Decoded Mode Storage Output			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
1.	Terminal 4	11v ——— 0v	Ground Go to step 2.	
2.	Collector Q31	11.6v ——— 0v	Ground Go to step 3.	Check transistor Q27, resistors R88, R97, R101. Replace as required.
3.	Base Q31	0v ———	Positive voltage. Check transistors Q26, Q28, Q29, diode CR44, and capacitor C22. Replace as required.	Check transistor Q31, resistor R75. Replace as required.
FUNCTION/SYMPTOM: No Code Separation Pulse			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
1.	A4TP5	7.8v 0v 	Ground Go to step 2.	
2.	Base Q14	0.7v ——— 0v	6 VDC Go to step 3.	Replace transistor Q14.
3.	Collector Q12	6v ——— 0v	Ground	Replace capacitor C11.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Encoder Clock (A4) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Code Separation Pulse			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
4.	Base Q12	0v -6v ———	Ground Check transistor Q12, diodes CR7, CR8, CR31, and resistors R27, R28. Replace as required.	Go to step 5.
5.	Base Q13	0v -3v ———	Ground Check transistor Q13 and resistors R32, R33. Replace as required.	
FUNCTION/SYMPTOM: No X Pulse Other outputs Normal			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM TERMINAL L GROUNDED
1.	Collector Q39	12v ——— 0v	Ground Go to step 2.	Check diode CR24 and replace if required.
2.	Base Q39	0v ———	6 vdc Replace diode CR74 or CR76.	Replace transistor Q39.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

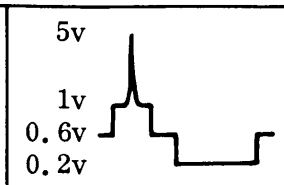
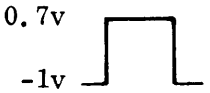
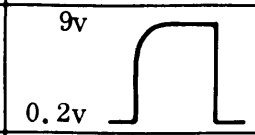
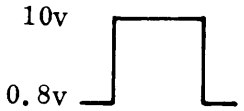
CIRCUIT CARD: Encoder Control (A5)				Reference figures 6-13 and 6-33
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No F1 Pulse			OPERATIONS:	Mode 2, Code 0000, MASTER to NORM
1.	A5TP7		0.2 vdc Go to step 2.	
2.	Base Q5		0.6 vdc Go to step 3.	Replace transistor Q5.
3.	A5TP1		1 vdc Check diodes CR6, CR7, CR8, CR9. Replace as required.	Go to step 4.
4.	Emitters Q2, A4Q1, Q4		Greater than 1 vdc Go to step 5.	
5.	Base Q2, A4Q1, Q4		9V pulse Check diodes CR19, CR28, and replace as required. Go to step 6.	Check transistors Q2, Q4, diodes CR4, CR36. Replace as required. Replace module A5A4.
6.	Emitter A2Q1		9 vdc Go to step 7.	
7.	Base A2Q1			Replace module A5A2.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

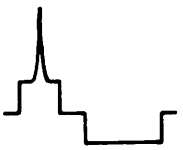
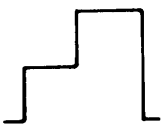
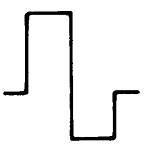
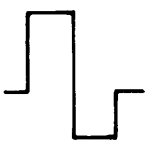
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Cl Pulse			OPERATIONS:	Mode 2, Code 0010, MASTER to NORM
1.	A5TP2	4.5v 1.4v 0.6v 0.2v 	0.2 vdc Go to step 2.	Check pin 59 (ground).
2.	Base Q6	0.7v -0.4v -0.7v 	0.6 vdc Go to step 3.	Check associated circuit components and transistor Q6. Replace as required.
3.	Emitters A3Q1, A4Q1, Q3, Q4	0.6v 0.2v 	Greater than 1 vdc or 9V pulse. Check diode CR30 and replace if required.	
4.	Base A3Q1, A4Q1, Q3, Q4	2.4v 0.8v 	+9V pulse Check diodes CR25, CR28 and replace if required.	Check transistors Q3, Q4. Replace module A5A3 or A5A4. Go to step 5.
5.	Emitter A1Q1	8v 0.8v 0.4v 	8.6 vdc Go to step 6.	
6.	Base A1Q1	9v 1.5v 1.0v 		Replace module A5A1. Go to step 7.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

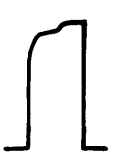
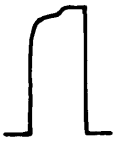
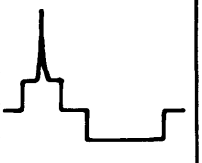
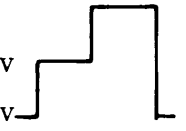
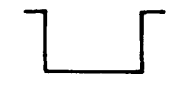
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No C1 Pulse			OPERATIONS:	Mode 2, Code 0010, MASTER to NORM
7.	Emitter A2Q1	9v  0.2v	8.6 vdc Go to step 8.	
8.	Base A2Q1	9.6v  0.8v		Replace module A5A2.
FUNCTION/SYMPTOM: No A1 Pulse			OPERATIONS:	Mode 2, Code 1000, MASTER to NORM
1.	A5TP3	4.5v  1.4v 0.6v 0.2v	0.2 vdc Go to step 2.	
2.	Base Q7	0.7v  -0.4v -0.7v	0.6 vdc Go to step 3.	Check transistor Q7 and associated circuit components. Replace as required.
3.	Emitters A3Q1, A4Q1,Q3, Q4, Q1, Q2	0.6v  0.2v	1 vdc or +9V pulse Check diodes CR31, CR37, CR1, CR5. Replace as required. Go to step 4.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

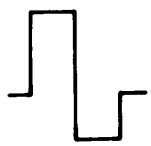
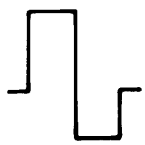
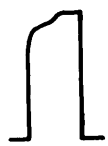
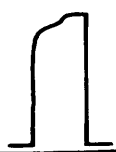
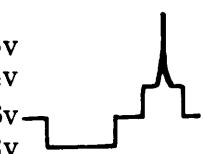
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No A1 Pulse			OPERATIONS:	Mode 2, Code 1000, MASTER to NORM
4.	Base A3Q1, A4Q1, Q3, Q4, Q1, Q2	2.4v 0.8v 	+9V pulse Check diodes CR25, CR28, CR10, CR19. Replace as required. Go to step 5.	Check transistors Q1, Q2, Q3, Q4. Replace module A5A3 or A5A4.
5.	Emitter A1Q1	8.0v 0.8v 0.4v 	Ground Go to step 6.	
6.	Base A1Q1	9.0v 1.5v 1.0v 		Replace module A5A1. Go to step 7.
7.	Emitter A2Q1	9.0v 0.2v 	Ground Go to step 8.	
8.	Base A2Q1	9.6v 0.8v 		Replace module A5A2.
FUNCTION/SYMPTOM: A2B4 Pulse Instead of B4 Pulse			OPERATIONS:	Mode 2, Code 0400, MASTER to NORM
1.	A5TP4	4.5v 1.4v 0.6v 0.2v 	 Go to step 2.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

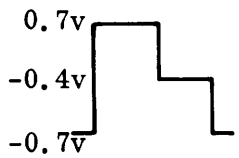
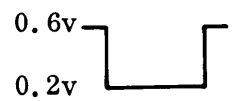
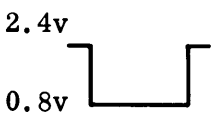
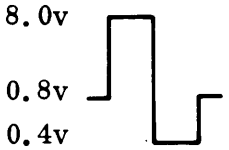
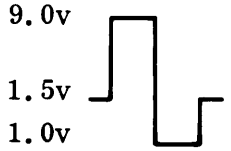
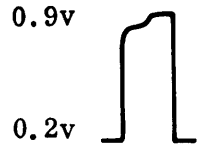
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: A2B4 Pulse Instead of B4 Pulse			OPERATIONS:	Mode 2, Code 0400, MASTER to NORM
2.	Base Q9		-1 vdc Go to step 5.	Check associated circuit components. Replace transistor Q9. Go to step 3.
3.	Emitters A3Q1, A4Q1, Q3, Q4, Q1, Q2		1 vdc or +9V pulse Check diodes CR33, CR39, Cr10, CR19. Replace as required. Go to step 4.	
4.	Base A3Q1, A4Q1 Q3, Q4 Q1, Q2		+9V pulse Check diodes CR25, CR28, CR10, CR17. Replace as required. Go to step 5.	Check transistors Q1, Q2, Q3, Q4. Replace module A5A3, or A5A4.
5.	Emitter A1Q1		Ground Go to step 6.	
6.	Base A1Q1		Ground Go to step 7.	Replace module A5A1.
7.	Emitter A2Q1		Ground Go to step 8.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

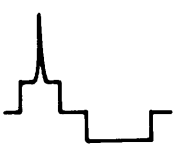
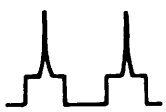
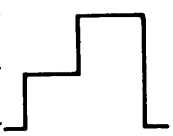
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: A2B4 Pulse Instead of B4 Pulse			OPERATIONS:	Mode 2, Code 0400, MASTER to NORM
8.	Base A2Q1	9.6v  0.8v		Replace module A5A2.
FUNCTION/SYMPTOM: C2D2 Pulse Instead of C2 Pulse			OPERATIONS:	Mode 2, Code 0020, MASTER to NORM
1.	A5TP8	4.5v 1.4v 0.6v 0.2v 	4.5v 1.0v 0.6v  Go to step 2.	
2.	Base Q8	0.7v -0.4v -0.7v 	1 vdc Go to step 5.	Check associated circuit components. Replace transistor Q8. Go to step 3.
3.	Emitters A3Q1, A4Q1, Q3, Q4, Q1, Q2	0.6v  0.2v	1 vdc or +9V pulse. Check diodes CR32, CR38. Replace as required. Go to step 4.	
4.	Base A3Q1, A4Q1, Q3, Q4, Q1, Q2	2.4v  0.8v	+9V pulse Check diodes CR25, CR28. Replace as required Go to step 5.	Check transistors Q1, Q2, Q3, Q4. Replace module A5A3 or A5A4.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

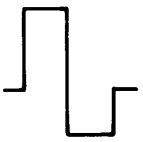
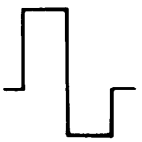
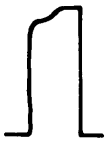
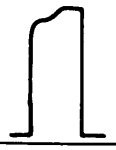
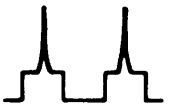
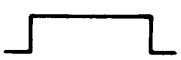
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: C2D2 Pulse Instead of C2 Pulse			OPERATIONS:	Mode 2, Code 0020, MASTER to NORM
5.	Emitter A1Q1	8.0v 0.8v 0.4v 	Ground Go to step 6.	Go to step 6.
6.	Base A1Q1	9.0v 1.5v 1.0v 		Replace module A5A1. Go to step 7.
7.	Emitter A2Q1	9.0v 0.2v 	Ground Go to step 8.	Go to step 8.
8.	Base A2Q1	9.6v 0.8v 		Replace module A5A2.
FUNCTION/SYMPTOM: C4D4 Pulse Appears When Not Enabled			OPERATIONS:	Mode 2, Code 0000, MASTER to NORM
1.	A5TP5	0.6v 0.2v 	 Go to step 2.	
2.	Base Q10	0.7v -0.7v 	-0.4 -0.7  Go to step 3.	Check associated circuit components. Replace transistor Q10.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: C4D4 Pulse Appears When Not Enabled			OPERATIONS:	Mode 2, Code 0000, MASTER to NORM
3.	Emitter A3Q1, A4Q1, Q3, Q4	0.6v 0.2v	1 vdc or +9V pulse Check diodes CR34, CR40. Replace as required. Go to step 4.	
4.	Base A3Q1, A4Q1, Q3, Q4	2.4v 0.8v	+9V pulse Check diodes CR25, CR28. Replace as required. Go to step 5.	Check transistors Q3, Q4. Replace module A5A3 or A5A4.
5.	Emitter A1Q1	8.0v 0.8v 0.4v	Ground Go to step 6.	
6.	Base A1Q1	9.0v 1.5v 1.0v		Replace module A5A1. Go to step 7.
7.	Emitter A2Q1	9.0v 0.2v	Ground Go to step 8.	
8.	Base A2Q1	9.6v 0.8v		Replace module A5A2.

Table 4-31. Functional Troubleshooting Chart
Extender Board Procedure (Cont)

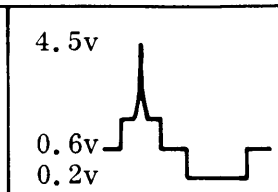
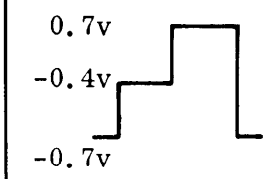
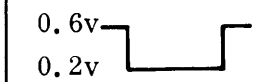
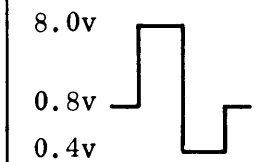
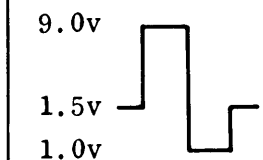
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No C4 Pulse			OPERATIONS:	Mode 2, Code 0040, MASTER to NORM
1.	A5TP5		0.2 vdc Go to step 2.	
2.	Base Q10		0.6 vdc Go to step 3.	Check associated circuit components. Replace transistor Q10.
3.	Emitters A3Q4, A4Q1, Q3, Q4,		1 vdc or +9V pulse Check diodes CR34, CR40. Replace as required. Go to step 4.	
4.	Base A3Q1, A4Q1, Q3, Q4		+9V pulse Check diodes CR25, CR28. Replace as required. Go to step 5.	Check transistors Q3, Q4. Replace module A5A3 or A5A4.
5.	Emitter A1Q1		8.6 vdc Go to step 6.	
6.	Base A1Q1			Replace module A5A1. Go to step 7.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No C4 Pulse			OPERATIONS:	Mode 2, Code 0040, MASTER to NORM
7.	Emitter A2Q1	9.0v 0.2v	8.6 vdc Go to step 8.	
8.	Base A2Q1	9.6v 0.8v		Replace module A5A2.
FUNCTION/SYMPTOM: No F2 Pulse			OPERATIONS:	Mode 2, Code 0000, MASTER to NORM
1.	A5TP10	4.5v 1.4v 0.6v 0.2v	0.2 vdc Go to step 2.	
2.	Base Q11	0.6v -0.7v	0.6 vdc Go to step 3.	Check associated circuit components. Replace transistor Q11.
3.	A5TP1	0v	1 vdc Check diodes CR6, CR7, CR8, CR9. Replace as required.	Go to step 4.
4.	Emitters Q1, A3Q1, Q3	0.8v 0.2v	1 vdc Go to step 5.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

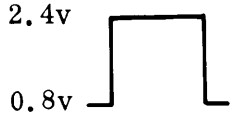
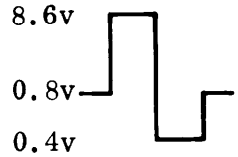
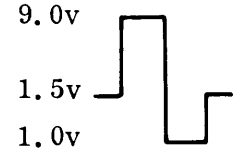
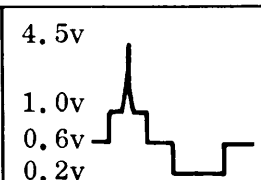
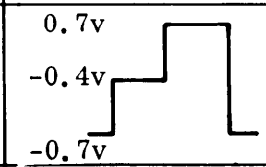
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No F2 Pulse			OPERATIONS:	Mode 2, Code 0000, MASTER to NORM
5.	Base Q1 A3Q1, Q3	2.4v 0.8v 	9V pulse Check diodes CR19, CR28. Replace as required. Go to step 6.	Check transistors Q1, Q3, diode CR3, CR35. Replace module A5A4.
6.	Emitter A1Q1	8.6v 0.8v 0.4v 	9 vdc Go to step 7.	
7.	Base A1Q1	9.0v 1.5v 1.0v 		Replace module A5A2.
FUNCTION/SYMPTOM: No C1 Pulse			OPERATIONS:	Mode C, C1 Pulse MASTER to NORM
1.	A5TP2	4.5v 1.0v 0.6v 0.2v 	0.2 vdc Go to step 2.	
2.	Base Q6	0.7v -0.4v -0.7v 	0.6 vdc Go to step 3.	Check transistor Q6 and associated components. Replace as required.
3.	Emitters A1Q1, A2Q1, A3Q1, A4Q1	0.6v 0.2v 	1 vdc or +9V pulse Go to step 4.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

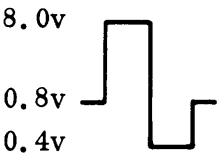
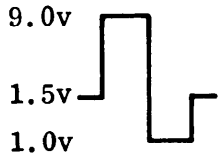
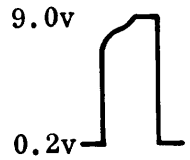
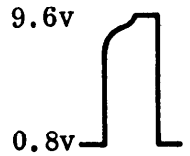
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No C1 Pulse			OPERATIONS:	Mode C, C1 Pulse MASTER to NORM
4.	Base A1Q1, A2Q1, A3Q1, A4Q1		+9V pulse Replace module A5A1, A5A2, A5A3, or A5A4	Go to step 5.
5.	Emitter Q3		8.6 vdc Check diodes CR31, CR35. Replace as required. Go to step 6.	
6.	Base Q3		8.6 vdc Check diode CR25. Replace transistor Q3.	Go to step 7.
7.	Emitter Q4		8.6 vdc Check diodes CR6, CR40. Replace as required. Go to step 8.	
8.	Base Q4		8.6 vdc Check diode CR28. Replace transistor Q4.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

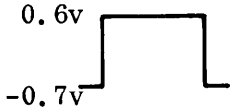
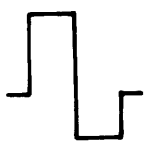
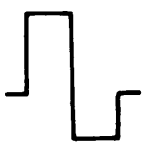
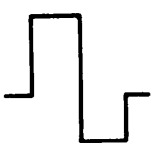
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: ClDl Pulse Appears No Input			OPERATIONS:	Mode C, No Code, MASTER to NORM
1.	A5TP2	0.6v 0.2v 	 Go to step 2.	
2.	Base Q6	0.6v -0.7v 	-0.7 vdc Check transistor Q6 and associated components. Replace as required. Go to step 3.	
3.	Emitter Q3	8.0v 0.8v 0.4v 	2 vdc Check diodes CR31-CR35, CR41. Replace as required. Go to step 6.	
4.	Base Q3	9.0v 1.5v 1.0v 	8.6 vdc Check transistor Q3, diode CR25. Replace as required	Go to step 5.
5.	Anode diode CR30	2.4v 0.3v 0.2v 	0.6 vdc Check capacitor C2. Replace as required.	Go to step 6.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

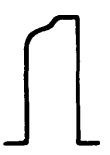
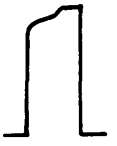
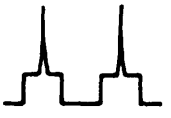
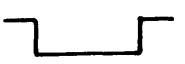
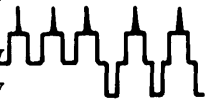
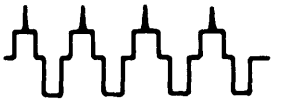
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: ClDl Pulse Appears No Input			OPERATIONS:	Mode C, No Code, MASTER to NORM
6.	Emitter Q4	9.0v  0.2v	2 vdc Check diodes CR31-CR35, CR48. Replace as required. Go to step 7.	
7.	Base Q4	9.6v  0.8v	8.6 vdc Check transistor Q4, diode CR28. Replace as required.	
FUNCTION/SYMPTOM: No 7700 Code In Emergency			OPERATIONS:	Mode 3/A, Code 0000, MASTER to EMER
1.	A5TP3 A5TP4	4.5v  1.4v 0.8v	0.6v 0.2v  Go to step 2.	
2.	A5TP7	4.5v  0.6v 0.2v	 Check diode CR24 and associated components. Replace as required.	Go to step 4.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

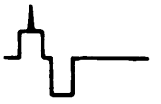
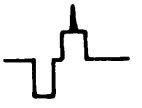
CIRCUIT CARD: Encoder Control (A5) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No 7700 Code In Emergency			OPERATIONS:	Mode 3/A, Code 0000, MASTER to EMER
3.	A5TP10	4.5v 0.6v 0.2v 	 Check diode CR23 and associated components. Replace as required.	Go to step 5.
4.	A5TP7 A5TP1	Same as step 2. 8.5v 0v  72 μs	 Check diodes CR7, CR8, CR24. Replace as required.	
5.	A5TP10 A5TP1	Same as step 3. Same as step 4.	 Check diodes CR6, CR9, CR23. Replace as required.	
FUNCTION/SYMPTOM: Code 7777 In Emergency			OPERATIONS:	Mode 3/A, Code 0000, MASTER to EMER
1.	A5TP2 A5TP8 A5TP5	0.2v  0v	 Go to step 2.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
CIRCUIT CARD: Encoder Control (A5) (Cont)				
FUNCTION/SYMPTOM: Code 7777 In Emergency			OPERATIONS:	Mode 3/A, Code 0000, MASTER to EMER
2.	A5TP6	8.6v ——— 0v	1 vdc Check encoder gating (A6)	Check resistors R81, R82, R83. Replace as required.
CIRCUIT CARD: Endocer Gating (A6)				Reference figures 6-14 or 6-15 and 6-34
FUNCTION/SYMPTOM: 2^4, 2^5, 2^6 Counters Inoperative			OPERATIONS:	Mode 2, Code 0000, STBY
1.	TP10	9.7v 0v	9.75 vdc Go to step 2.	Go to step 4.
2.	Base Q17	0v, 0.6v, 0.5v, -5.6v	-0.5 vdc Replace Q17.	Go to step 3.
3.	Collector Q16	9.7v 0.6v	Ground Check Q16 and associated components.	Go to step 4.
4.	Collector Q9	9v 0v	9 vdc Go to step 5.	Go to step 7.

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

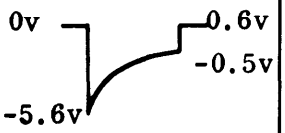
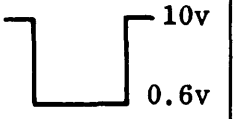
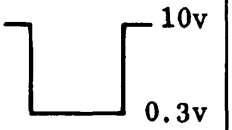
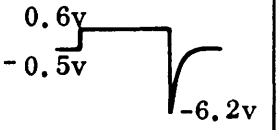
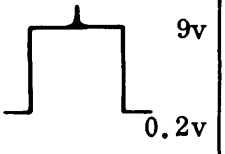
CIRCUIT CARD: Encoder Gating (A6) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: 2^4, 2^5, 2^6 Counters Inoperative			OPERATIONS:	Mode 2, Code 0000, EMER
5.	Base Q9		-0.5 vdc Replace Q9.	Go to step 6.
6.	Collector Q8		Ground Check Q8 and associated components.	Go to step 7.
7.	TP7		10 vdc Go to step 8.	Go to step 8.
8.	Base Q1		-0.5 vdc Replace Q8.	Go to step 9.
9.	Collector Q2		Ground Check Q2 and associated components.	

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

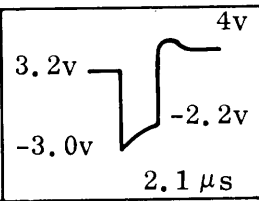
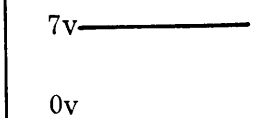
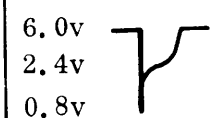
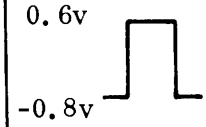
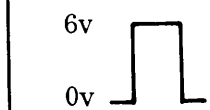
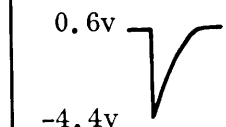
CIRCUIT CARD: Encoder Gating (A6) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Reset Pulse			OPERATIONS:	Mode 2, Code 0000, STBY Q8 at 10V, TP7 10V, TP8 11.8V
1.	TP5		0 vdc Go to step 2.	Go to step 2.
2.	ANODE CR41		7.9 vdc Go to step 3.	Check capacitor C7, diodes CR3, CR17, CR31, resistors R10, R13. Replace as required.
3.	Collector Q3		6 vdc Go to step 4.	Replace diode CR41.
4.	Base Q3		0.6 vdc Go to step 5.	Replace transistor Q3.
5.	Collector Q4		5 vdc Go to step 6.	
6.	Base Q4			Check transistor Q4 and associated components. Replace as required.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

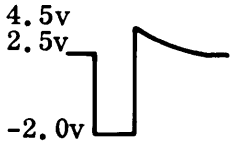
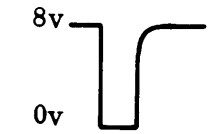
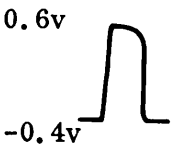
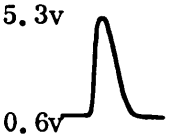
CIRCUIT CARD: Encoder Gating (A6) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Auxiliary Reset			OPERATIONS:	Mode 2, Code 0000, STBY Ground A4TP5, A6TP3
1.	A6TP8		11.8 vdc Go to step 2.	Check diode CR8. Replace if required.
2.	Collector Q18		12 vdc Go to step 3.	Check diode CR25, resistors R50, R51. Replace as required.
3.	Base Q18		Ground Check diodes CR33, CR35, resistors R67, R68. Replace as required.	Replace transistor Q18. Go to step 4.
4.	Collector Q10		8 vdc Go to step 5.	Check capacitor C15. Replace if required.
5.	Base Q10		-0.4 vdc Go to step 6.	Replace transistor Q10.
6.	Anode CR21		Ground Go to step 7.	

Table 4-31. Functional Troubleshooting Chart, Extender Board procedure (Cont)

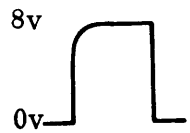
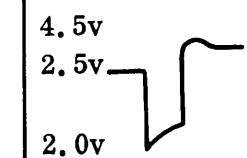
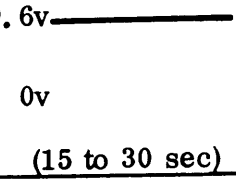
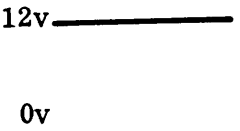
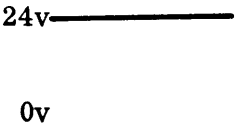
CIRCUIT CARD: Encoder Gating (A6) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Auxiliary Reset			OPERATIONS:	Mode 2, Code 0000, STBY Ground A4TP5, A6TP3
7.	Collector Q9		Ground Check 2^5 counter, transistors Q8, Q9, and associated components. Replace as required.	Check diode CR23, resistors R44, R45, R47. Replace as required. Go to step 8.
8.	A6TP8 Interrgate in M3/A		11.8 vdc Check diodes CR34, CR12. Replace as required.	
FUNCTION/SYMPTOM: No I/P Operation			OPERATIONS:	Mode 2, Code 0000, MASTER to STBY
1.	A6TP3		11.6 vdc Go to step 2.	
2.	Base Q19		Ground Go to step 3.	Replace transistor Q19.
3.	Cathode CR36		Ground Replace capacitor C9.	Go to step 4.
4.	Collector Q20		Ground Go to step 5.	

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

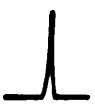
CIRCUIT CARD: Encoder Gating (A6 (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No I/P Operation			OPERATIONS:	Mode 2, Code 0000, MASTER to STBY
5.	Base Q20	0v -1v ———	0.6 vdc Go to step 6.	Replace transistor Q20.
6.	Collector Q2-	0v ——— (15 to 30 sec)	15.4 vdc Check transistor Q21 and associated components. Replace as required.	Check transistor Q22 and associated components. Replace as required.
FUNCTION/SYMPTOM: No Emergency Operation			OPERATIONS:	Mode 2 Steps 1-5, Mode 3/A Steps 6-9, Code 0000, EMER
1.	A6TP2 M-3/A	10v ——— 0v	Ground Go to step 2.	Go to step 4.
2.	Base Q5 M-3/A	0v -0.7v ———	0.6 vdc Go to step 3.	Replace transistor Q5.
3.	Cathode CR9 M-3/A	6v 0v 		Replace diode CR9.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

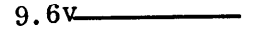
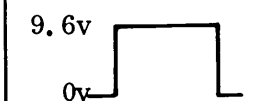
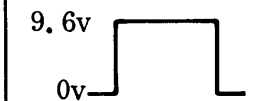
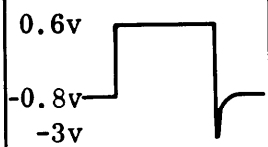
CIRCUIT CARD: Encoder Gating (A6) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Emergency Operation			OPERATIONS:	Mode 2 Steps 1-5, Mode 3/A Steps 6-9, Code 0000, EMER
4.	A6TP1 M-3/A		Ground Go to step 5.	Go to step 6.
5.	Base Q6 M-3/A		Ground Check diodes CR10, CR11, CR13. Replace as required.	Replace transistor Q6.
6.	A6TP1 M-2		Ground Go to step 7.	
7.	A6TP4 M-2		9.6 vdc Go to step 8.	Check transistor Q7, diode CR10. Replace as required.
8.	Collector Q15		9.6 vdc Go to step 9.	Check diode CR29 and replace if required.
9.	Base Q15		-0.5 vdc Check transistor Q14 and associated circuits. Replace as required.	Replace transistor Q15.

Table 4-31. Functional Troubleshooting Chart, Extender Board Procedure (Cont)

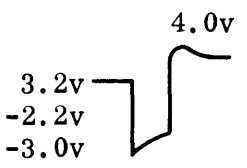
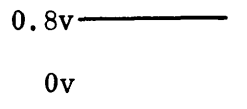
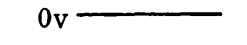
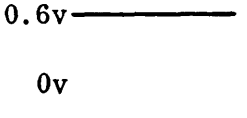
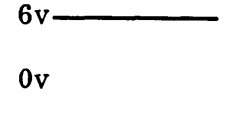
CIRCUIT CARD: Encoder Gating (A6) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No D4 Pulse In Mode C			OPERATIONS:	Mode C, Full Code, MASTER to STBY
1.	A6TP5		3.2 vdc Go to step 2.	
2.	Collector Q11		12 vdc Go to step 3.	Go to step 6.
3.	Collector Q12		20 vdc Go to step 4.	
4.	Base Q12		-0.5 vdc Go to step 5.	Replace transistor Q12. Go to step 6.
5.	Collector Q13		Ground Check transistor Q13 and associated components. Replace as required.	
6.	Base Q11		Ground Check resistors R53 and R55. Replace as required.	Replace transistor Q11.

Table 4-32. Functional Troubleshooting Chart, In-Circuit Procedure

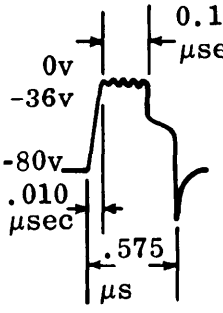
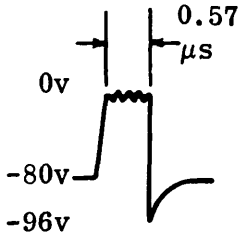
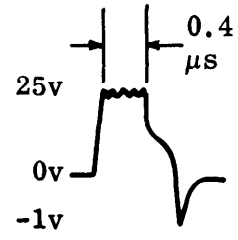
CIRCUIT CARD: Modulator (A7)			Reference figures 6-10 and 6-24	
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output			OPERATIONS:	Mode 2, Code 7777, MASTER to NORM
1.	Z2-2 (Oscillator input)		-1 vdc or ground Check resistors R15-R19, transistor Q5. Replace as required. -80 VDC Go to step 2.	
2.	Base Q5		-80 vdc Go to step 3.	
3.	Emitter Q4	 (Rise Time 30 ns)	25 vdc Replace transistor Q4. Ground Go to step 4.	Check transformer T1 and replace if required.

Table 4-32. Functional Troubleshooting Chart, In-Circuit Procedure (Cont)

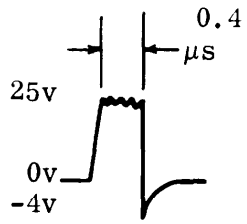
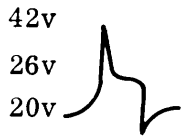
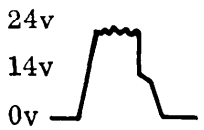
CIRCUIT CARD: Modulator (A7) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output			OPERATIONS: Mode 2, Code 7777, MASTER to NORM	
4.	Base Q4		Ground Check thermistor RT1, resistors R3, R5. Replace as required. Go to step 5.	Replace transistor Q4.
5.	Collector Q1		25 vdc Check transistor Q1, diodes CR1, CR2, capacitor C1. Replace as required. Ground Check resistor R1, capacitors C7, C8. Replace as required. Go to step 6.	Check transformer T2 and replace if required.
6.	Base Q1		0V Check resistors R1-R4. Replace as required.	
CIRCUIT CARD: Sensitivity (A8)			Reference figures 6-2 and 6-17	
FUNCTION/SYMPTOM: No Output STBY or NORM			OPERATIONS: Mode 2, Code 0000, -90 dbv, MASTER to STBY	
1a.	A8-1		Negative dc level Check capacitor C1. Replace if required.	Go to step 1b.
1b.	A8-3		28 vdc Check filter FL12. Replace if required.	Go to step 2a.

Table 4-32. Functional Troubleshooting Chart, In-Circuit Procedure (Cont)

CIRCUIT CARD: Sensitivity (A8) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Output STBY or NORM			OPERATIONS:	Mode 2, Code 0000, -90 dbv, MASTER to STBY
2a.	A8-6 A8-7 A8-8	0v -110v————	Ground Go to step 2b.	
2b.	A8-7	0v -109v————	Ground Go to step 2c.	
2c.	A8-8	0v -108.5v————	Ground Check resistors R1-R3, R6, capacitor C4, relay K1. Replace as required.	Go to step 3.
3.	A8-5 No jamming	0v -110v————	0V Go to step 4.	
Turn MASTER to OFF. Use ohmmeter for following test, observing polarities indicated.				
4.	A8-5^{+} to A8-4^{-}	100K Ohms	Less than 100K ohms. Check capacitors C2, C3. Replace as required.	Go to step 5.
5.	A8-5^{-} to A8-9^{+}	0.3 Megohm	Less than 0.3 Megohm to 0.6 Megohm. Check capacitor C4. Replace as required.	Go to step 6.

Table 4-32. Functional Troubleshooting Chart, In-Circuit Procedure (Cont)

CIRCUIT CARD: Sensitivity (A8) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
Turn MASTER to OFF. Use ohmmeter for following test, observing polarities indicated.				
6.	A8-4$^-$ to Anode CR2$^+$ A8-4$^+$ to Anode CR2$^-$	7.5K Ohms 60K Ohms	2.4K Ohms Check diode CR2. 35K Ohms Replace if required.	Go to step 7.
7.	A8-4$^-$ to Anode CR1$^+$ A8-4$^+$ to Anode CR1$^-$	2.4K Ohms 35K Ohms	0 Ohms. Check diode CR1. Replace if required.	Go to step 8.
8.	A8-1$^+$ to A8-4$^-$	200K Ohms	2.4K Ohms Check capacitor C1. Replace if required.	
FUNCTION/SYMPTOM: No Output in LOW			OPERATIONS: Mode 2, Code 0000, -90 dbv, MASTER to STBY	
1.	A8-3	28v —————— 0v	Ground Check relay K1 and diode CR3. Replace as required.	Go to step 2.
2.	A8-6 A8-7 A8-8	0v -110v ——————	Ground Check resistors R1, R2, R3, and R5. Replace as required.	

Table 4-32. Functional Troubleshooting Chart, In-Circuit Procedure (Cont)

RECEIVER [RF AMPLIFIER (AR1), PRESELECTOR (Z1)]
Reference figures 4-13, 6-16 & table 4-24

FUNCTION/SYMPTOM:	No Output or Low Gain	OPERATION:	Mode 2, Code 0000, MASTER to STBY

STEP	PROCEDURE		
1.	Check filament voltages	AR1-2 AR1-5 AR1-8	6.3 vdc 6.3 vdc 6.3 vdc
2.	Check grid voltage	AR1-7	-110 vdc
3.	Check grid voltage (no jamming)	AR1-1	-110 vdc
4.	Check cathode voltages	AR1-3 AR1-6 AR1-9	-110 vdc -109 vdc -108.5 vdc
5.	Align AR1 and 21 in accordance with procedures of table 4-43.		
6.	If receiver cannot be aligned, disconnect low pass filter (CP1) from J1 of 21. Connect J1 to SG-677/U, through an attenuator, and attempt to align 21 and AR1.		
7.	If alignment cannot be performed in step 6, check components CP1, Z3, W1, W2, and J5. Should these components be found serviceable, replace Z1 or AR1.		

NOTE

Determine defective Z1 or AR1 by substituting known serviceable part.

8. If Z1 and AR1 are properly aligned in step 5 but gain in normal operation is low, proceed as follows:

   a. Connect AN/URM-64A Signal Generator or equivalent through a 10-dB pad to ANT. J5.

   b. Adjust AN/URM-64A for a frequency of 1030 MHz and an output of -17 dBm.

   c. Connect AN/USM-140B probe to AR3TP1 and adjust AN/URM-64A frequency for maximum signal.

   d. Output pulse at AR3TP1 should be 1.5 volt minimum representing a receiver gain of 43 dB.

Table 4-32. Functional Troubleshooting Chart, In-Circuit Procedure (Cont)

RECEIVER [RF AMPLIFIER (AR1), PRESELECTOR (Z1)] Reference figures 4-13, 6-16 & table 4-24			
FUNCTION/SYMPTOM:	No Output or Low Gain	OPERATION:	Mode 2, Code 0000, MASTER to STBY

STEP	PROCEDURE
8. e.	If output pulse is not correct, disconnect W2 from Z1 and connect AN/URM-64A through 10-dB pad to input of Z1.
f.	Output pulse at AR3TP1 should increase approximately 0.3 volts .
g.	If increase in 8f is greater than 0.3 volts, check CP1, W2, Z3, W1, and J2.
h.	If pulse amplitude at AR3TP1 is less than 1.8 volts minimum, replace Z1 or AR1.
	NOTE Determine defective Z1 or AR1 by substituting known serviceable part.

TRANSMITTER [AMPLIFIER (AR2), OSCILLATOR (Z2)] Reference figures 4-13, 6-15, and table 4-24			
FUNCTION/SYMPTOM:	No Output or Low Output	OPERATION:	Mode 2, Code 7777, MASTER to NORM

STEP	PROCEDURE		
1.	Check filament voltages	Z2-3 Z2-4 AR2-1 AR2-2	6.3 vdc 6.3 vdc 6.3 vdc 6.3 vdc
2.	Check cathode voltages	AR2-3	25 vdc
3.	Check Z2-2 for a positive-going waveform from -80V to 0V.		
4.	Check plate voltage for 1000 vdc.		
5.	Align AR2 and Z2 in accordance with procedures of table 4-43.		
6.	If transmitter does not align properly, disconnect diplexer (CP1) lead from AR2 and connect AR2 to HP IN on AN/UPM-98A.		
7.	If transmitter can now be adjusted, check components CP1, ANT. J5, and W1. Replace if required.		
8.	If components are found serviceable, replace AR2 and Z2.		

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure

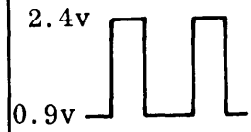
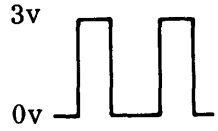
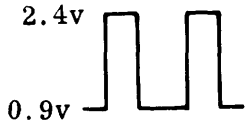
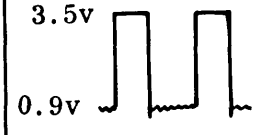
CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0501, 0502)				Reference figures 4-15, 6-1 and 6-23
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Log Video Output			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
1.	AR3TP1		Ground Go to step 2.	Go to step 3.
2.	Base Q1		Ground Check detector and replace if required.	Check transistors Q1 and Q2. Replace if defective.
3.	A5-7		Ground Check capacitor C15, resistor R51. Replace if defective.	Go to step 4.
4.	Base Q10		Ground Replace CA3005 A5.	Go to step 5.
5.	Emitter Q10		Ground Replace transistor Q10.	Go to step 6.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0501, 0502) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Log Video Output			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
6.	Emitter Q11	1.07v 0.9v 	Ground Check capacitor C17, resistors R57, R60, R61. Replace as required. Go to step 10.	Go to step 7.
7.	Collector Q11	1.79v 0.9v 	Ground Replace transistor Q11.	Go to step 8.
8.	Emitter Q12	1.74v 0.9v 	Ground Replace transistor Q12.	Go to step 9.
9.	AR3TP4	1.2v 1v 	Ground Replace transistor Q13.	
10.	Emitter Q7 Ground A4-7	0.3v 0v	Ground Go to step 11.	Go to step 12.

Table 4-33 Functional Troubleshooting Chart,
Out of Circuit Procedure (Cont)

CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0501, 0502) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Log Video Output			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
11.	Base Q7 Ground A4-7	1v —— 0v	Ground Replace CA3005 A4.	Replace transistor Q7.
12.	Emitter Q6 Ground A3-7	0.3v —— 0v	Ground Go to step 13.	Go to step 14.
13.	Base Q6 Ground A3-7	1v —— 0v	Ground Replace CA3005 A3.	Replace transistor Q7.
14.	Emitter Q5 Ground A2-7	0.3v —— 0v	Ground Go to step 15.	Go to step 16.
15.	Base Q5 Ground A2-7	1v —— 0v	Ground Replace CA3005 A2.	Replace transistor Q5.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0501, 0502) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Log Video Output			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
16.	Emitter Q4 Ground A1-7	0.3v 0v	Ground Go to step 17.	Go to step 18.
17.	Base Q4 Ground A1-7	1v 0v	Ground Replace CA3005 A1	Replace transistor Q4.
18.	Emitter Q3 Ground junction R29, R28, C11	0.3v 0v	Ground Go to step 19.	
19.	Base Q3 Ground junction R29, R28, C11	1v 0v	Ground Check transistors Q1, Q2. Replace as required.	Replace transistor Q3.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

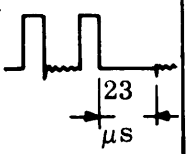
CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0501, 0502) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Bias Voltage			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
1.	AR3TP2	4.5v 0v	Ground Check transistor Q14, μL710 A6, and associated components. Replace as required.	
2.	AR3TP3	0v -4.5v	Ground Check transistor Q15, μL710 A7, and associated components. Replace as required.	
FUNCTION/SYMPTOM: No Anti-Jam			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
1.	Collector Q9	5v 2v 	Ground Go to step 2.	
2.	Emitter Q9	2.8v 0.3v 	Ground Go to step 3.	Replace transistor Q9.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

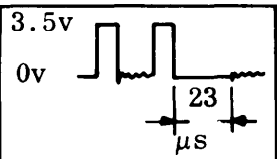
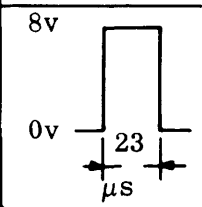
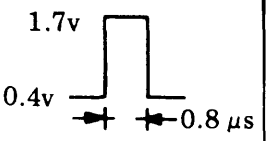
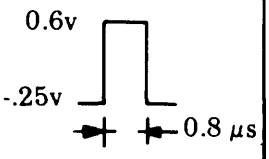
CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0501, 0502) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Anti-Jam			OPERATIONS:	Mode 2, Code 0000 MASTER to STBY
3.	Base Q8		Ground Check capacitor C11, resistor R40. Replace as required.	Replace transistor Q9. No 23 µsec blanking pulse go to step 4.
4.	Base Q16			Check transistor Q16 and diode CR2. Replace as required.
CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0503)				Reference figures 4-15, 6-2 and 6-24
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Log Video Output			OPERATIONS:	Mode 2, Code 0000 MASTER to STBY
NOTE Prior to performing step 1 adjust OUTPUT ATTEN 0-100 dBm control to 0. Increase attenuation only if observed pulses show saturation.				
1.	TP1		Go to step 2.	Go to step 3.
2.	E1		Check detector and replace if required.	Check transistor Q1 and associated components. Replace as required.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

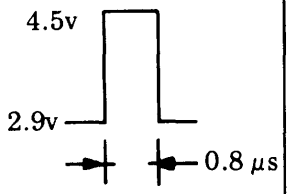
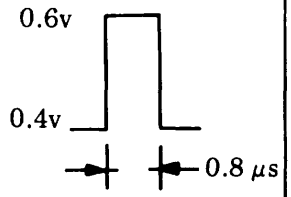
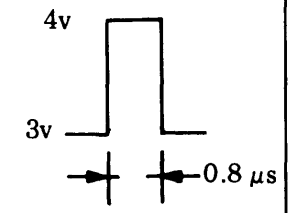
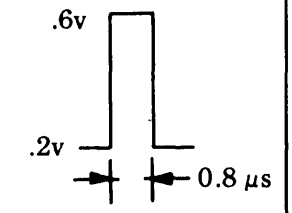
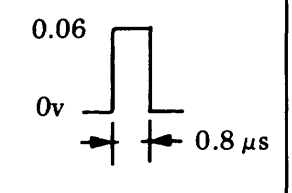
CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0503) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Log Video Output			OPERATIONS:	Mode 2, Code 0000 MASTER to STBY
3.	TP2		Go to step 4.	Go to step 5.
4.	U2-1		Check transistor Q2 and associated components. Replace as required.	Check U2 and associated components. Replace as required.
5.	TP3		Go to step 6.	Go to step 8.
6.	U3-1		Check transistor Q3 and associated components. Replace as required.	Check U3 and associated components. Replace as required.
7.	U1-4		Check resistors R2, R3, and R4. Replace as required.	Go to step 8.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

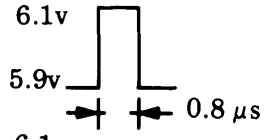
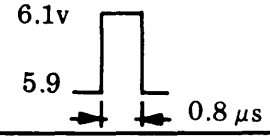
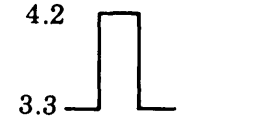
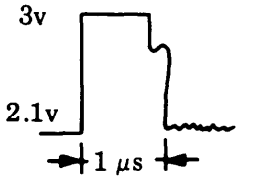
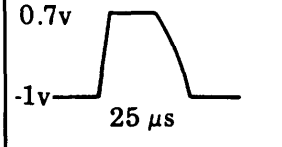
CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0503) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Log Video Output			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
8.	U1-5		Replace U1.	Go to step 9.
	U1-11		Replace U1.	
9.	U5-8		Replace U5.	Go to step 10.
10.	J1		Replace U5.	
FUNCTION/SYMPTOM: No Anti-Jam			OPERATIONS: Mode 2, Code 0000 MASTER to STBY	
1.	U5-3		Check resistors R20 and R22. Replace as required.	Go to step 2.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

CIRCUIT CARD: Detector and Video Amplifier (AR3) (Part No. 4023409-0503) (Cont)				
STEP	MEASURE	SIGNAL	ABNORMAL INDICATION	NORMAL INDICATION
FUNCTION/SYMPTOM: No Anti-Jam			OPERATIONS:	Mode 2, Code 0000 MASTER to STBY
2.	U5-5	Train of random pulses 0V to 2.5V. Ground (no pulses during time of suppression pulse).	Replace U5.	Go to step 3.
3.	U4-7	Same as U5-5 0V to 2V	Check U4. Replace if defective.	Check resistor R21 and diode CR3. Replace as required.
CIRCUIT CARD: Delay Line (DL1)				
DELAY LINE (DL1)				Reference figure 6-6 or 6-7

Make the following resistance measurements with multimeter ME-26/U.

PIN	to	PIN	MEASUREMENT	PIN	to	PIN	MEASUREMENT
1		4	16Ω	8		11	34Ω
1		6	10Ω	8		12	43Ω
1		7	4.7Ω	8		13	52Ω
1		3	8.0Ω	8		14	56Ω
8		22	160Ω	8		15	68Ω
8		9	15Ω	1		16	300Ω
8		10	25Ω	22		16	300Ω

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

POWER SUPPLY (PS1)	Reference figures 4-22 to 4-28, and 6-11

The power supply (PS1), part numbers 2073404-0704 and -705, is tested using the Tester-Dummy Load TS-3243/APM (or load bank assembly) and the procedures in paragraph 4-16c.4. When problems are encountered, the troubleshooting procedures presented in this table should be used to find the cause of the problem. The circuit-board assemblies in the power supply are non-repairable and must be replaced as an assembly should a fault be traced to one of them. Also, when repairs are required on a 2073404-0704 power supply, the 21435 overcurrent assembly should be replaced with a 21435-1 assembly and the alignment and adjustment procedures of table 4-43, step 14 be performed.

WARNING

Lethal voltages are present when power is applied to test setup using tester (or Load Bank Assembly). These voltages are present on red A1 wire, on terminal E5 of the Tester, and on terminal A1 in the open power supply.

SYMPTOM	PROCEDURE
1. Power supply fails continuity test.	a. Place the tester POWER switch at the OFF position. b. Disconnect tester connectors P1 and P2 from the power supply. c. Using the ME-26U multimeter, measure continuity (nominally zero ohms) between the following points of the power supply. A high resistance reading on any of these lines indicates a broken wire or faulty connection between the points referenced. PS1P1 pin 1 to PS1P2 pin 1 PS1P1 pin 6 to PS1P2 pin 6 PS1P1 pin 10 to PS1P2 pin 10 PS1P1 pin 11 to PS1P2 pin 11 PS1P1 pin 12 to PS1P2 pin 2 PS1P1 pin 15 to PS1P2 pin 3 PS1P1 pin A2 to PS1P2 pin A2 PS1P1 pin 9 to Ground (TP1 of power supply)

Table 4-33. Functional Troubleshooting Chart, out of Circuit procedure (Cont)

POWER SUPPLY (PS1)	Reference figures 4-22 to 4-28, and 6-11
SYMPTOM	PROCEDURE
1. (Cont)	d. If continuity is obtained between each of the points indicated in the preceding step, connect the positive lead of the ME-26U multimeter to TP5 and the negative lead to TP1 (ground).
	e. Reconnect P1 and P2 of the tester to the power supply.
	f. Place the multimeter scale switch to a range sufficient to measure +12 vdc.
	g. Place the POWER switch at the ON position.
	h. If +12 vdc is present at TP5, the connection between pin 7 of PS1P1 and pin 1 of inductor L1 is open and must be repaired.
	i. If no voltage is present at TP5, the problem is in subassembly 22375-2, 22653, or transformer T1 of the power supply.
2. Power supply fails to start.	a. Check for continuity between terminal 7 and collectors of transistors Q1 and Q2.
	b. Check for presence of dc voltage at terminal 2 of transformer T3. If no dc voltage, check transistors Q1 and Q2 for open. If transistors Q1 and Q2 are good, replace regulator board 21431 or 21431-1 with replacement part 21431-1 and overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

POWER SUPPLY (PS1)	Reference figures 4-22 to 4-28, and 6-11
SYMPTOM	PROCEDURE
2. (Cont)	c. If dc voltage is present at terminal 2 of transformer T3, and inverter does not start (this can be verified by checking for square waves at collectors of transistors Q15 and Q16), Q14 is probably open. Replace inverter drive assembly 21443 or 21443-1 with replacement part 21443-1 and overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment proce–dures of table 4-43, step 14.
3. Power supply short circuit protection circuits trip under no-load conditions.	a. Check to see if output voltages come up. If all voltages come up but one, remove assembly 21473 and isolate fault, using an ohm-meter. Replace appropriate sub-assembly 21447 or 21447-1, or 21451, or 21472, and overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.
	b. Turn off power supply, remove wire from E11 of subassembly 21146 or 22146-1 and turn on power supply. If problem is solved, replace subassembly 22146 or 22146-1 with replacement part 22146-1 and overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.

Table 4-33. Functional Troubleshooting Chart, out of Circuit Procedure (Cont)

POWER SUPPLY (PS1)	Reference figures 4-22 to 4-28, and 6-11
SYMPTOM	PROCEDURE
3. (Cont)	c. If step 2.b. does not solve the problem, turn off power supply and reconnect wire to E11. Turn on power supply and check for presence of square waves at collector of transistors Q15 and Q16. If output of collector of either transistor Q15 or Q16 remain at ground, check for short and replace, if required. If transistors Q15 and Q16 are active when short occurs, transformer T2 is probably open. Replace inverter drive assembly 21443 or 21443-1 with replacement part 21443-1 and overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.
	d. If steps 2a. through 2.c. do not locate fault, replace overcurrent assembly 21435 or 21435-1 if not replaced as part of above procedures. Perform alignment and adjustment procedures of table 4-43, step 14.
4. Power supply will not regulate.	a. Check transistors Q1 and Q2 for short circuit. If defective, replace filter capacitor assembly 21494 and overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.
	b. Check for continuity between terminal 9 of subassembly 21435 or 21435-1 and point E9 of the -6 volt output. Repair wire or solder joint, if required.

Table 4-33. Functional Troubleshooting Chart, Out of Circuit Procedure (Cont)

POWER SUPPLY (PS1)	Reference figures 4-22 to 4-28, and 6-11
SYMPTOM	PROCEDURE
4. (Cont)	c. If no fault is found in steps 3a. and 3.b., replace regulator assembly 21431 or 21431-1 with 21431-1 and overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.
5. Power supply fails to start (blows fuses) .	a. Check to see if terminal 7 (PS1P1) is shorted to ground. If grounded, remove wire from junction of diodes CR1 and CR2, subassembly 22375-2. If problem is solved, replace subassembly 22375-2, and also replace overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.
	b. If terminal 7 (PS1P1) is still grounded after procedure of step 4.a., the probable cause is a shorted capacitor in subassembly 21495 or a grounded collector on transistors Q1 or Q2. Replace subassembly 21495 or defective transistor. Replace overcurrent assembly 21435 with 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.
	c. If condition occurs in ac only, check for shorted transformer (Tl) primary or open in diodes CR1 or CR2 of subassembly 22375-2. Replace defective transformer or subassembly 22375-2. Replace overcurrent assembly 21435 witho 21435-1, if applicable. Perform alignment and adjustment procedures of table 4-43, step 14.

4-17. DISASSEMBLY OF RECEIVER-TRANSMITTER.

CAUTION

Remove pressure valve cap and depress needle valve pin to repressurize receiver-transmitter before disassembling.

4-18. GENERAL TECHNIQUES. When disassembling receiver-transmitter, observe the following precautions:

Refer to precautions in paragraph 4-27a.3.

b. Before any connection is unsoldered, observe the position of each lead and identify or tag each lead to be removed with reference to its terminal.

4-19. SEPARATION OF ASSEMBLIES. The RT-859/APx-72 separates into two sections: the rf section and the digital and power supply section (see figure 4-16) .

CAUTION

Remove the rf section slowly to avoid pulling the antenna lead from its connector.

a. Unclamp and remove encircling flange coupler.

b. Separate the rf assembly from the digital and power supply assembly.

Disconnect subminiature coax connector (see figure 4-16) from video output jack AR3J1.

d. Remove silicon O-ring from rf section.

4-20. RF SECTION. perform the following steps to disassemble the rf section.

Remove screws (S1, S2, and S3 figure 4-16).

b. Remove rf shield (figure 4-16).

c. Remove screws A7S1 and A7S2 on modulator board A7 (figure 4-17).

d. Unsolder and tag all leads to A7.

e. Remove A7.

f. Unscrew and remove the preselector Z1 and amplifier AR1 mounting clamps (1, 2, and 3, figure 4-17) .

g. Disconnect Z1 and AR1 cables.

h. Remove mounting clamps held in position by screws (4 through 11, figure 4-17).

i. Remove cables from AR2.

j. Unsolder and tag all leads to power amplifier AR2.

k. Disconnect cables to low-pass filter 23 and oscillator Z2 and remove AR2. (Z3 is under A7 in figure 4-17.)

1. Unsolder and tag all leads to oscillator 22.

Remove case mounting screw (12, figure 4-17) and Z2.

n. Disconnect cable to detector and video amplifier AR3.

o. Unsolder and tag all leads to AR3 and remove.

p. Remove mounting screws 13 and 14 on sensitivity board A8 (figure 4-17) . (Take care not to lose the standoff that separates the filter FL16 from the sensitivity board.)

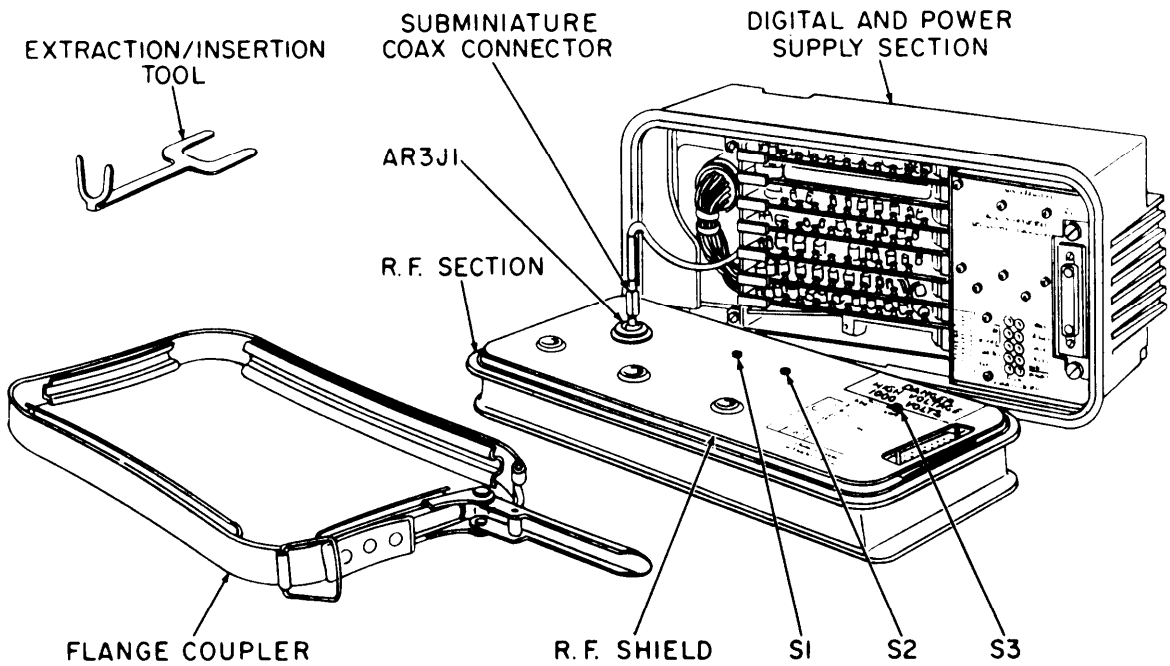


Figure 4-16. RT-859/APx-72, Disassembly

q. Unsolder and tag all leads to A8 and remove.

r. Unsolder and tag leads to FL16 and remove.

Remove mounting screw (16, figure 4-17).

t. Unsolder and tag all leads to transformer assembly T1 (figure 4-17).

u. Remove two guide pins (17 and 18, figure 4-17).

v. Unsolder and tag all leads to power-in connector XPS1P2 (figure 4-17) .

Remove screw 15 on side of filter assembly FL6 through FL15 (figure 4-17).

Unsolder and tag all leads to filter assembly FL6 through FL15 and remove. (See figure 4-33.)

4-21. DIGITAL AND POWER SUPPLY SECTION. Perform the following steps to disassemble this section.

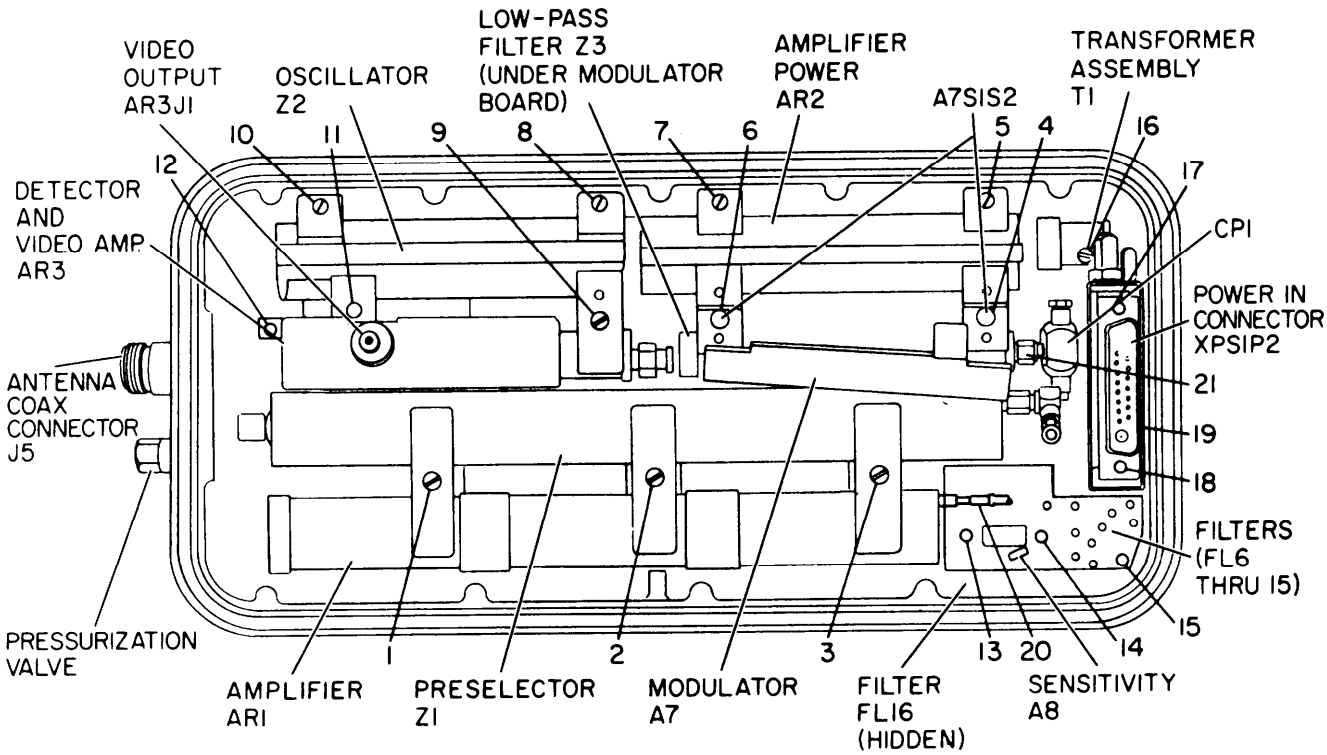


Figure 4-17. RT-859/APX-72 RF Section, Subassembly Location and Disassembly Points

a. Remove all fuses.

b. Lift up lift-out handles (figure 4-18) and pull circuitboard out of card cage.

CAUTION

Do not twist circuitboards or use excessive force when withdrawing them from the card cage. Such actions may cause damage to components or bend the board guides or connections.

c. Disconnect digital power and control connector (figure 4-18).

NOTE

Use connector extraction/insertion tool (figure 4-16) supplied with Test Set, Transponder AN/APM-239. Insert rounded edge of tool and disconnect with an upward pull.

d. Loosen two slotted lift-out screws (1, figure 4-18) and remove power supply PS1.

e. Remove four slotted mounted screws (1, 2, 3, and 4, figure 4-19) .

f. Remove card cage.

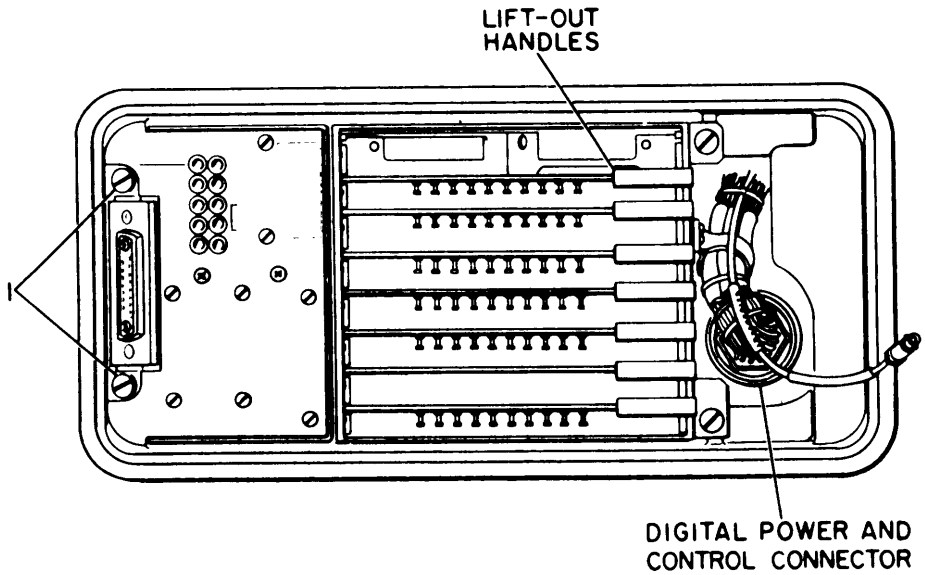


Figure 4-18. Digital and Power Supply Section and Circuitboard Removal

g. Remove two screws (5, figure 4-19) and disengage Circuitboard connector at the bottom of card cage, opposite screws hidden from view. (Follow this procedure for each connector in card cage.)

h. Unsolder and tag all leads to card cage connectors.

Remove four slotted screws (1, 2, 5, and 9, figure 4-20) and lift off faceplate. (The faceplate and its internal components are the only components that may be removed without performing any other disassembly tasks.)

j. Unscrew two nuts (6 and 8, figure 4-20) and remove elapsed time indicator (7, figure 4-20).

k. Unscrew two self-locking nut caps (3 and 10, figure 4-20) and remove carrying handle (4, figure 4-20).

1. Unsolder and tag all leads from power and control connector J1 (figure 4-21).

m. Unscrew two mounting nuts and remove J1.

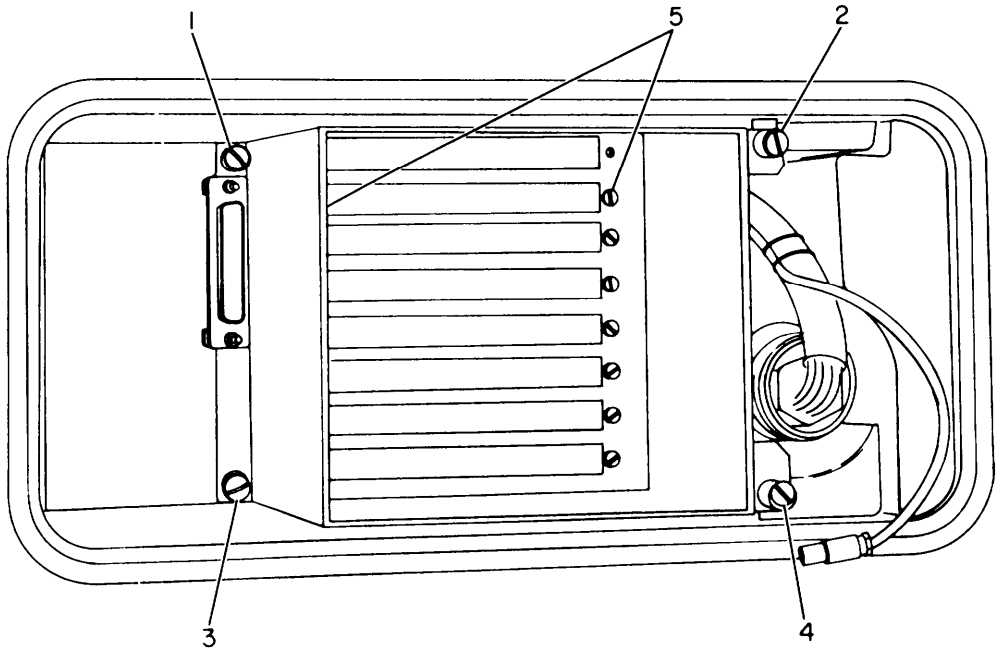


Figure 4-19. Digital and Power Supply Section, Circuitboard Cage Removal

n. Unsolder and tag all leads from thumbwheel switch assembly (figure 4-21).

o. Unsolder and tag all leads from elapsed time indicator (figure 4-21).

p. Remove mounting screws for filter assembly FL2, FL3, FL4, and FL5 (figure 4-21).

q. Unsolder and tag all leads to filter assembly FL2, FL3, FL4, and FL5.

r. Remove filter assembly FL2, FL3, FL4, and FL5.

s. Remove mounting screws for relay K1 (figure 4-21) .

t. Unsolder and tag all leads and diodes to relay K1.

u. Remove relay K1.

v. Remove mounting screws for relay K2 (figure 4-21).

w. Unsolder and tag all leads and diodes to relay K2.

x Remove mounting screws for FL1 (figure 4-21).

y. Unsolder and tag all leads to filter FL1.

z. Remove FL1.

aa. Unscrew power and control feedthrough (figure 4-21).

ab. Power and Control Connector J1 (figure 4-21).

1. Remove three screws securing insert on rear of connector J1 (figure 4-21).

2. Lift edge of insert clamp from which screws were removed

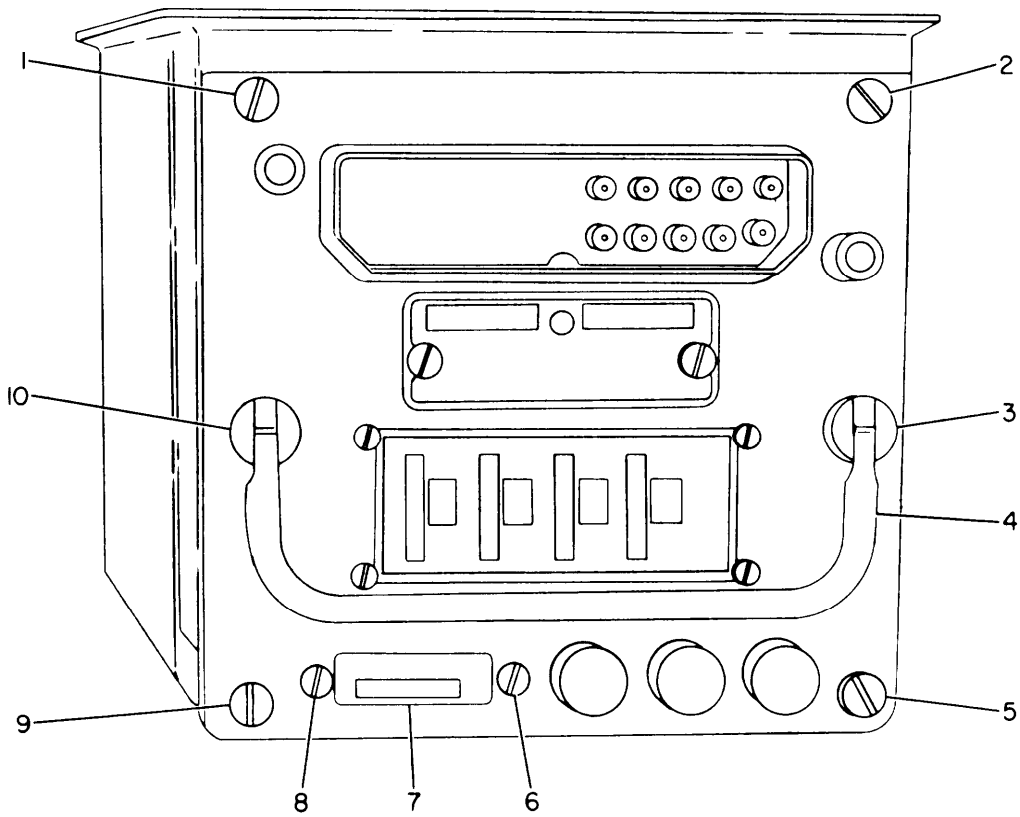


Figure 4-20. Faceplate Removal

until three fingers (figure 4-21) are free from holding slot on connector shell.

3. press firmly and evenly against connector pins from front side of connector until insert is free of connector shell.

CAUTION

Ensure that insert is not separated into component sections as misalignment of pins may result.

4. Remove two self-locking nuts (figure 4-21) .

5. Remove connector shell.

ac. Power Supply PS1.

1. Remove 12 screws (1, 3, 6, 7, 8, 9, 10, 11, 13, 20, 21, 22, figure 4-22).

2. Remove power supply cover and clamp.

3. Remove two screws (2, 3, figure 4-23) from high voltage assembly A5.

4. Unsolder and tag all leads to high voltage assembly A5 and remove.

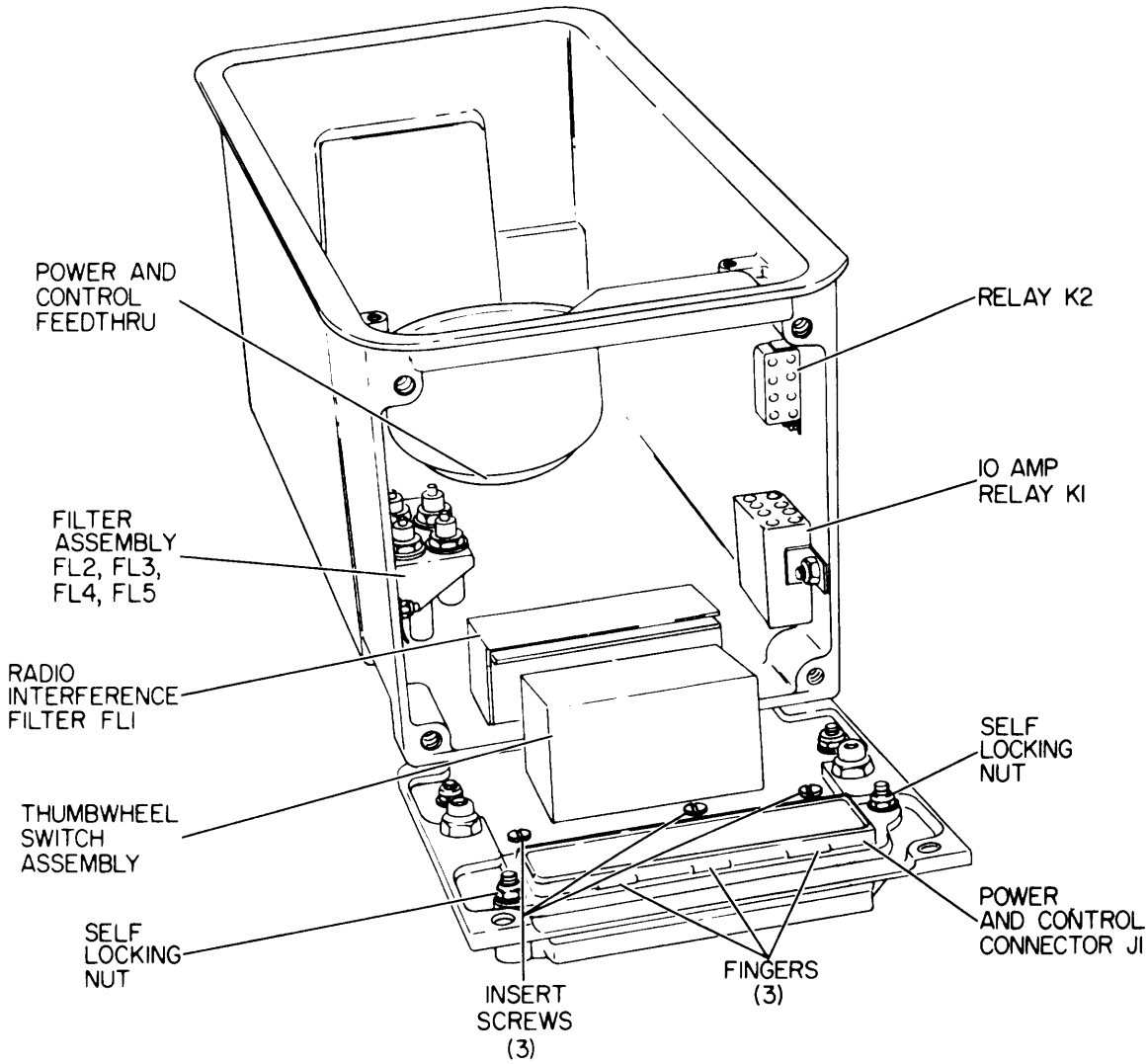


Figure 4-21. Faceplate Removed

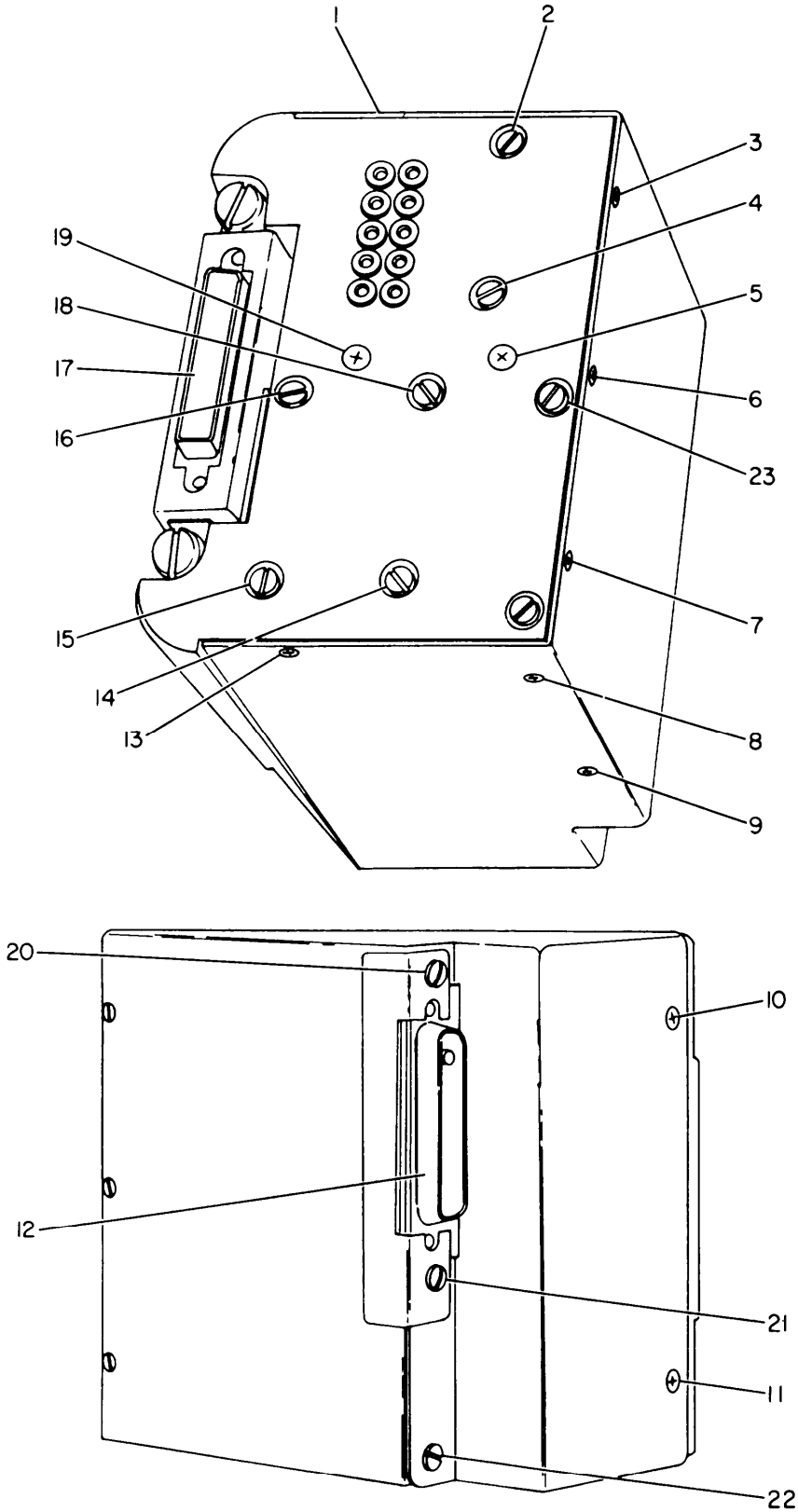


Figure 4-22. Power Supply Cover Removal and External Mounting Screws

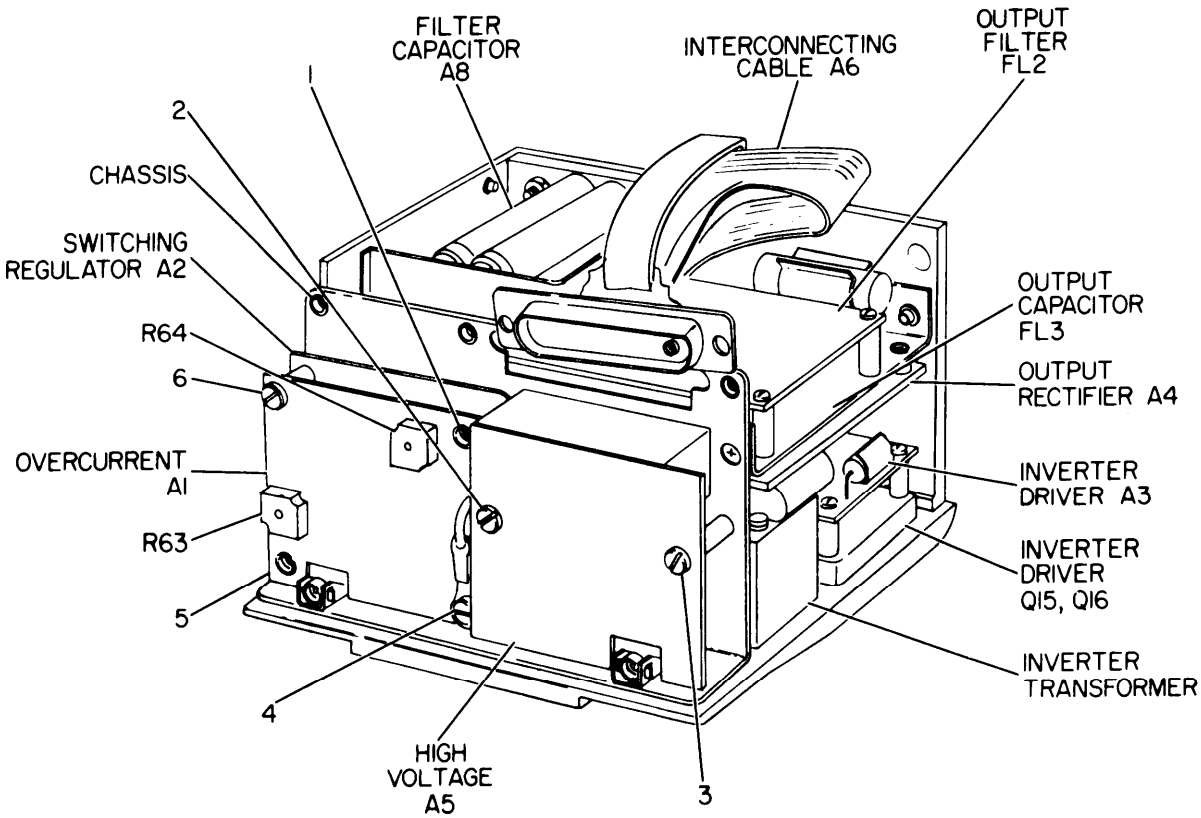


Figure 4-23. Power Supply, Identification of Assemblies

5. Remove four screws (1, 4, 5, 6, figure 4-23) from overcurrent assembly Al.

6. Separate switching regulator assembly A2 from overcurrent assembly Al, and unsolder and tag all leads to both assemblies (figure 4-23) .

7. Remove four screws (1, 2, figure 4-24, 2, 4, figure 4-22) and remove output assembly (FL2-FL3, and A4) (figure 4-25).

8. Remove four screws (1, 2, 3, 4, figure 4-25) from output rectifier assembly A4.

9. Unsolder and tag all leads to output rectifier assembly A4.

10. Remove four screws (11, 12, 13, 14, figure 4-26) from output filter assembly FL2.

11. Separate output filter assembly FL2 from output capacitor assembly FL3.

12. Remove four screws (4, 6, 7, 10, figure 4-26) from inverter driver assembly A3.

13. Unsolder and tag all leads to inverter driver assembly A3.

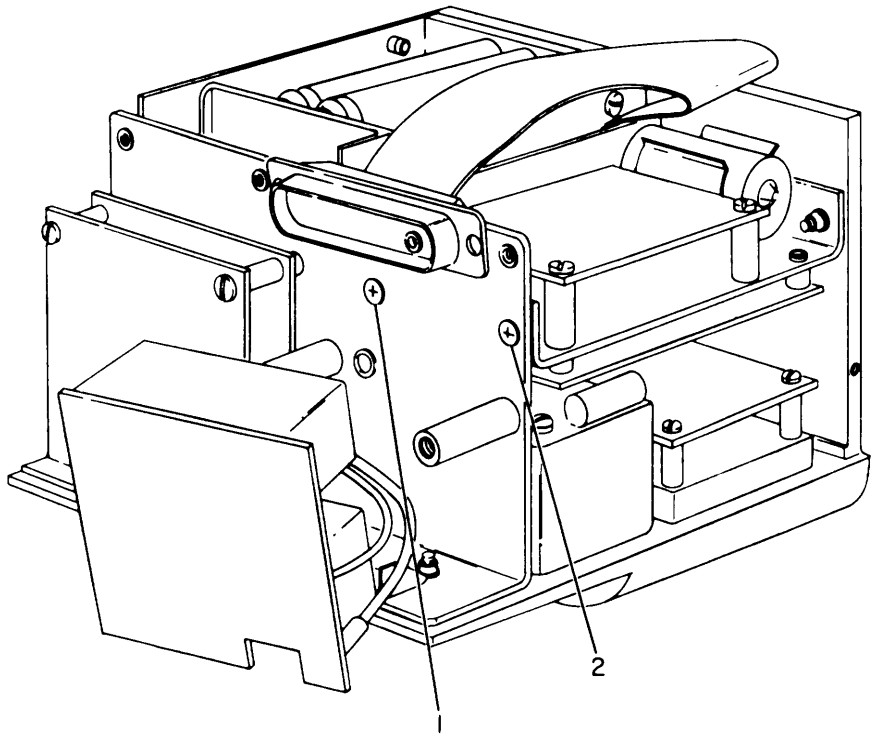


Figure 4-24. Power Supply, Output Assembly Removal

14. Remove two screws (8, 9, figure 4-26) from inverter driver assembly transistors Q15 and Q16.

15. Unsolder and tag all leads to inverter driver assembly transistors Q15 and Q16.

16. Remove four screws (15, 16, 17, 18, figure 4-26) from inverter transformer T3.

17. Unsolder and tag all leads to inverter transformer T3.

18. Unsolder and tag all leads to dual diode CR34, CR35 (figure 4-26).

19. Remove screw from underside of main chassis releasing diode.

20. Remove four screws (1, 3, 5, one not shown, figure 4-26) from interconnection board and subassembly and remove subassembly.

21. Remove four screws (1, 2, 3, 4, figure 4-27) from filter capacitor assembly A8.

22. Unsolder and tag all leads to filter capacitor assembly A8.

23. Remove four screws (1, 3, 4, 10, figure 4-28) from switch regulator driver assembly A7.

24. Unsolder and tag all leads to switch regulator driver assembly A7.

25. Separate switch regulator driver assembly from reactor L2 (figure 4-28).

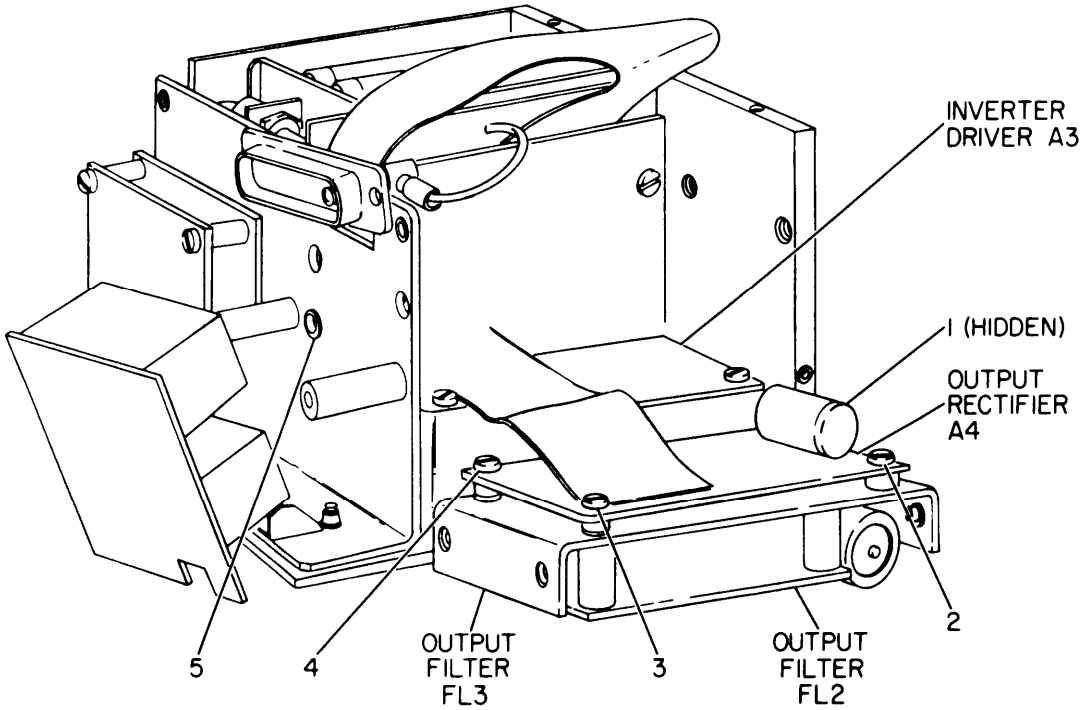


Figure 4-25. Power Supply, Output Rectifier Assembly Removal

26. Unsolder and tag all leads to reactor L2 and remove L2.

27. Remove four screws (14, 15, 16, 18, figure 4-22) securing power transformer T1 shown in figure 4-28.

28. Unsolder and tag all transformer leads and remove T1.

29. Unsolder and tag all leads to RFI filter FL1 (figure 4-28).

30. Remove 2 screws (11, 12, figure 4-28) and remove FL1.

31. Unsolder and tag all leads to components on chassis assembly (figure 4-28).

32. Remove 3 screws (5, figure 4-28) and remove chassis assembly.

33. Remove four screws (2, three hidden, figure 4-28) attaching reactor L1 to gusset plate and remove L1.

34. Remove screw (2, figure 4-26) and remove semiconductor device CR1, CR2 (figure 4-28) from gusset plate.

35. Remove two recessed screws (5, 19, figure 4-22) and remove gusset plate (figure 4-28).

36. Remove nuts (6, 7, 8, 9, figure 4-28) and remove semiconductor devices Ql, Q2.

4-22. CLEANING.

4-23. Clean, receiver-transmitter and Mountings MT-3809/APX-72 and MT-3948/APX-72, externally by removing dust and other foreign

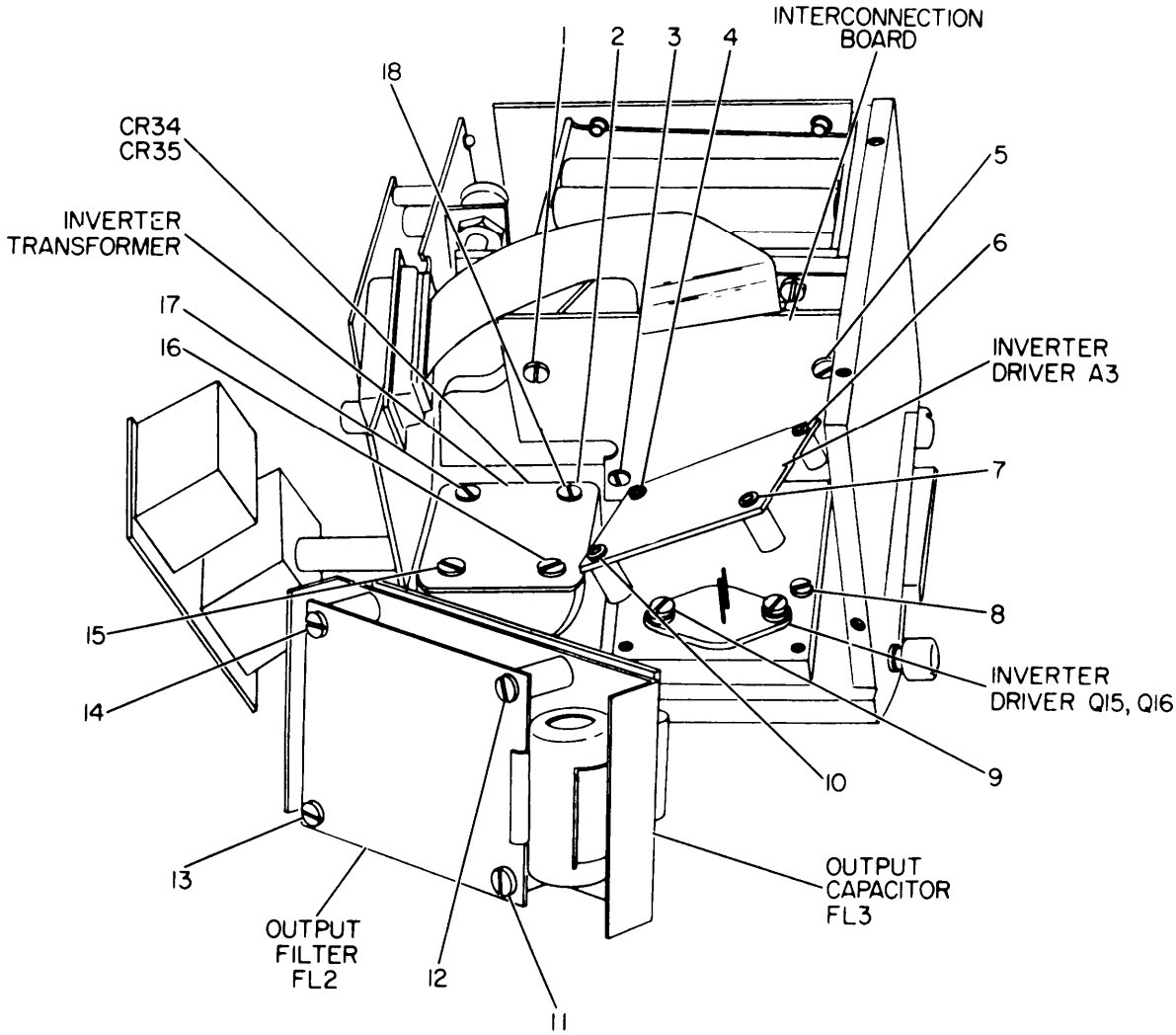


Figure 4-26. Power Supply, Internal Disassembly Points

matter with a dry cloth or dust-brush. Clean circuitboard contacts using a two-inch china bristle brush and cleaning compound, Federal specification O-T-620A.

4-24. INSPECTION.

4-25. At the intermediate, direct/general maintenance level, a thorough inspection shall be made of the receiver-transmitter and its subassemblies, both internally and externally, before restoring it to service. The inspection of the mountings MT-3809/APX-72 and MT-3948/APX-72 consists of checking for cracked or broen frame and loose or missing hardware.

a. Internal Inspection.

1. Remove and visually inspect digital circuitboard assemblies for cracks and breaks, broken track, and loose or missing electrical components. Replace defective circuitboards and tag them for repair, or discard, as their condition warrants.

2. Visually inspect circuitboard card cage for cracks and

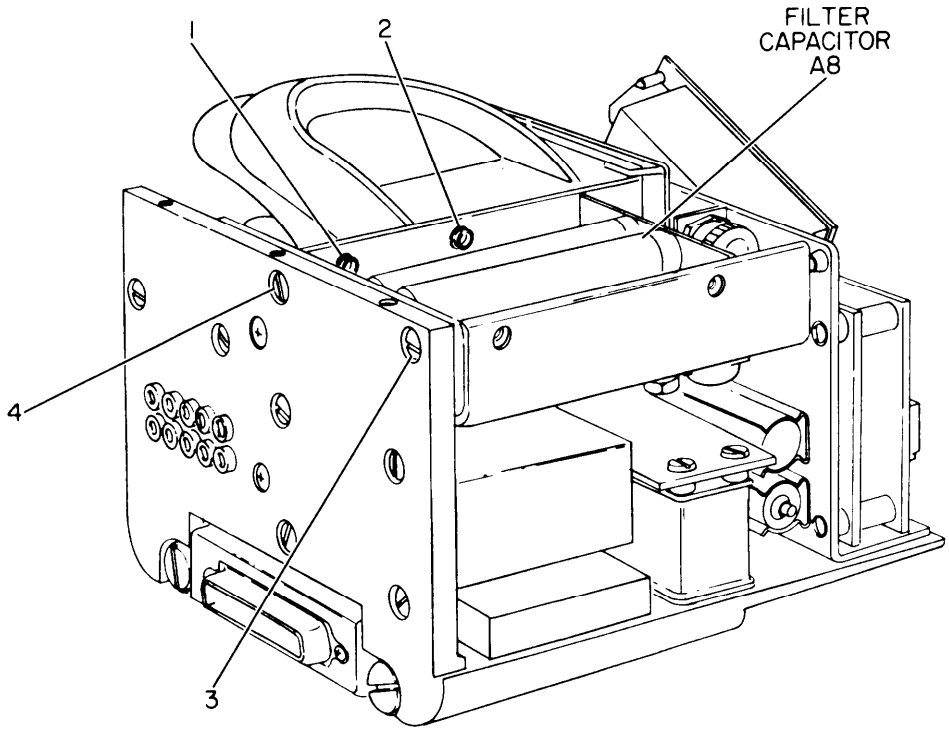


Figure 4-27. Power Supply, Filter Capacitor Assembly Removal

other defects. If defective, replace and tag cage for repair, or discard, as condition warrants.

3. Replace circuitboard sub-assemblies ensuring that they are properly seated and inserted in position according to color coding (refer to table 2-1).

4. Check power supply for proper seating and secure fastening.

5. Check rf components for proper seating and secure fastening.

6. Visually inspect rf circuitboards for evidence of warping, cracking, broken track, loose, and missing components. If defective, replace and tag for repair, or discard, as condition warrants.

7. Check all internal cables for security of connections.

b. External Inspection.

1. Visually inspect jacks J1 and J5. Ensure that they are clean and have no broken or bent pins. Replace if defective, discard defective jack.

2. Check pressure valve for proper operation.

3. Check MODE 2 code switch for proper mechanical action. Observe that the mechanical action is without backlash, binding or scraping. Replace if defective.

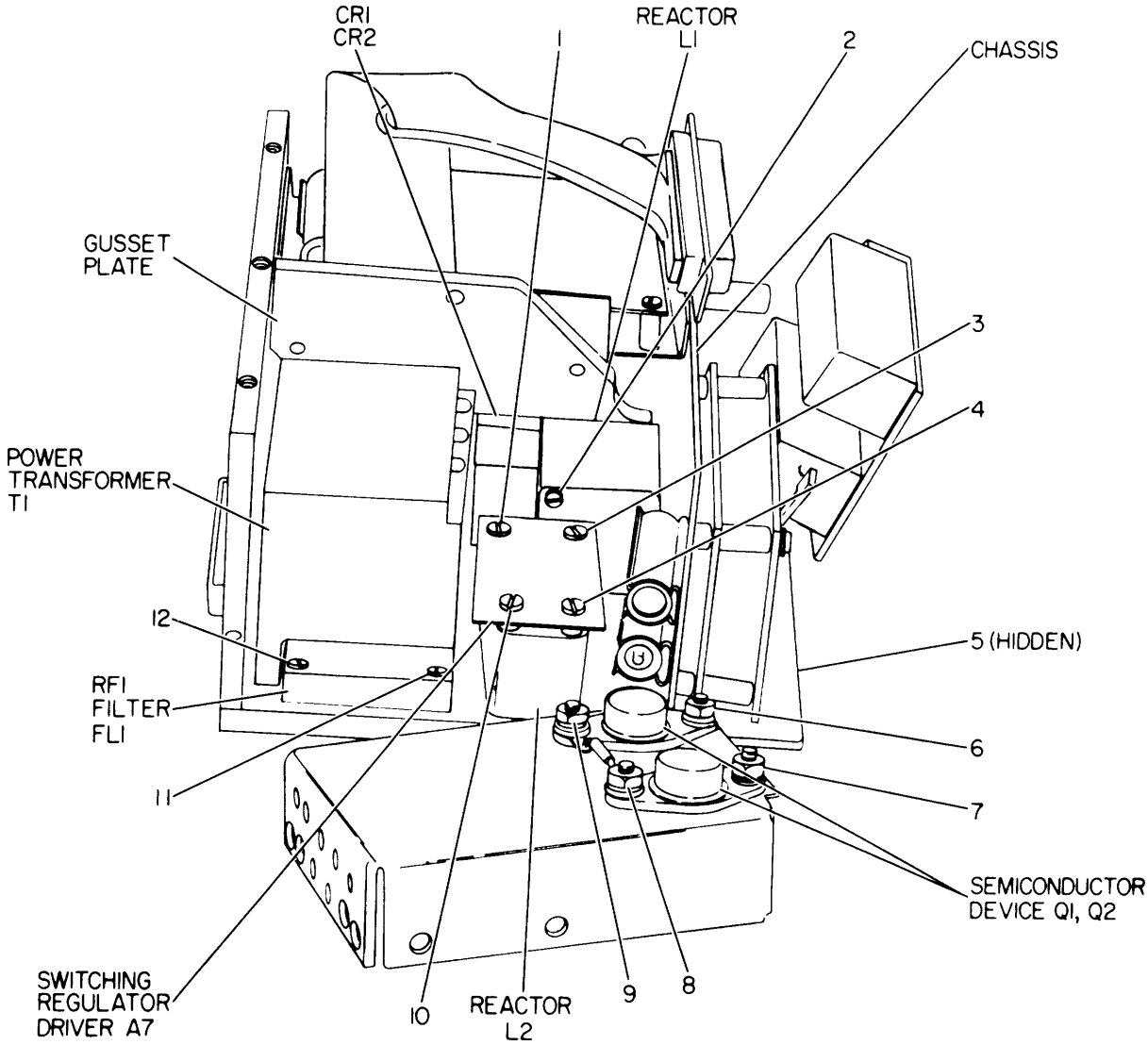


Figure 4-28. Power Supply, Identification of Internal Assemblies and Disassembly Points

4. Visually inspect elapsed time indicator for serviceability, ensure glass surface is clean and not cracked or damaged. Replace indicator if defective or expended.

5. Check two operating fuses for condition and correct values. Check spare fuse for proper value.

4-26. REPAIR.

NOTE

The U.S. Air Force will repair the following assemblies at depot level only.

Processor (A1) Encoder Clock (A4)
Decoder (A2) Encoder Control (A5)
Mode 4 (A3) Encoder Gating (A6)
Power Supply (PS1)

4-27. All subassemblies of the receiver-transmitter can be easily reached and replaced without special procedures. Refer to paragraphs 4-17 and 4-30 for instructions for disassembly and assembly as required. Refer to Illustrated Parts Breakdown Manual (NAVAIR 16-30APX72-3, NAVSHIPS 0967-217-4030, and T.O. 12P4-2APX72-4) or the Repair Parts and Special Tools List (ARMY) (TM 11-5895-490-35P) for replacement part numbers. Refer to subparagraph c., below, for instructions on assembly or manufacture of repair parts source coded AF, A, MF, or M in the Illustrated Parts Breakdown Manual or coded A or M in the Repair Parts and Special Tools List.

a. Circuitboard Repair. Circuitboards contain transistorized and modular components which can be easily damaged if adequate precautions are not observed during repair procedures. The following instructions apply specifically to the repair of circuitboards.

1. Tools . Recommended tools are a vise or special jig to hold circuitboard, a 25 to 40-Watt pencil type soldering iron with special provision for grounding soldering tip (see figure 4-29) and a pair of needlenose pliers.

2. Bulk Materials. Bulk materials recommended for cleaning, repairing, and assembling of the receiver-transmitter consist of the following:

(a) Federal specification O-T-620A, cleaning compound for cleaning circuitboard contacts.

(b) Specification MIL-A-46106, adhesive for cementing applicable components listed in table 4-34 to circuitboards.

(c) Specification MIL-S-8660B, silicone base heat-conducting components for application between mating surfaces of rf section and digital and power supply sections prior to assembly (refer to paragraph 4-34c.).

(d) Bendix part number 2077846-0001 (Dow Corning 340) silicone base heat-conducting compound for application between mating surfaces of transmitter (AR2, Z2) , receiver (AR1, 21), power supply (Psi) , and their respective cases before assembly (refer to paragraphs 4-32q, u, and 4-33aa.l).

3. Precautions.

(a) Do not allow circuitboard to be damaged through movement or undue pressure.

(b) Do not use a soldering gun; damaging voltages may be induced in circuit components.

(c) Do not use an ungrounded soldering iron (see figure 4-29) when soldering microelectronic devices; heater induced voltages will destroy the input capacitor of MOS microelectronic devices.

CAUTION

Do not use an ac soldering iron without an isolating transformer in the line. Also check for short circuits to the soldering iron tips before using.

(d) Do not overheat solder joints; components or circuitboard may be damaged.

(e) Do not use acid core solder.

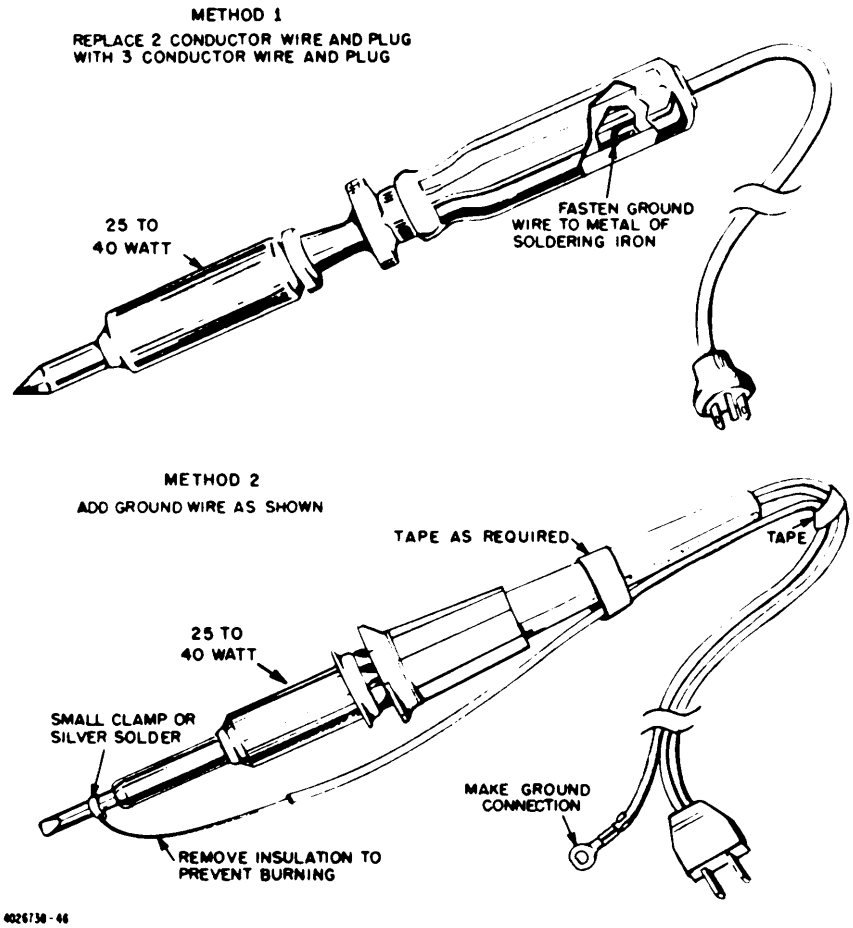


Figure 4-29. Recommended Methods for Grounding Soldering Irons

4. Procedure.

(a) Clamp circuitboard firmly in vise or jig.

(b) Unsolder connections which attach component or module to circuitboard. The conformal coating on the circuitboards is readily soldered through and need not be removed.

(c) Remove cemented components (refer to table 4-34) by lifting.

(d) Remove any adhesive residue from circuitboards by peeling it off. New adhesive will bond with any adhesive residue but caution must be exercised so that height of replacement part does not exceed maximum limits listed in table 4-34.

(e) Cut leads of replacement part to proper length.

(f) Fit replacement part into same position on circuitboard as that occupied by original part

applying cement, bead, or spacer, if applicable, (refer to table 4-34). The bead is used to prevent solder from being pulled into adjacent circuits, the pacer to separate body of esistor from circuitboard.

(g) Solder leads to circuitboard connections using needle-nose pliers as a heat sink, if practical.

(h) Ensure that when repairs are completed, the maximum height above circuitboard of components does not exceed the dimensions of table 4-34.

(i) Clean circuitboard contacts with cleaning compound Federal specification O-T-620A before replacing in the receiver-transmitter.

b. Subassembly Replacement. The Transmitter [Power Amplifier (AR2) and Oscillator (Z2)] , RF Amplifier (AR1), Delay Line (DL1), and subassemblies of the Power Supply (PS1) listed in table 4-36, are nonrepairable. If found defective, these subassemblies must be replaced with designated spares in the same position as the original subassembly.

Table 4-34. Component Mounting Information

NOMENCLATURE AND ASSEMBLY NO.	BEAD 2054239-0701	ADHESIVE MIL-A-46106	SPACER 4023758-0001	DISC 2025799-0702	MAXIMUM HEIGHT ABOVE CIRCUITBOARD (INCHES)
Processor (Al) 4030070 (RT-859/ APX-72)		C2, C23, DL1	R11, R37, R76		0.375
Processor (Al) 4028684 (RT-859A/ APX-72)		DL1	Al, A2-Use 4023632-0002 R11, R14, R48, R66, R100 - Use 4023758-0001	Q1-Q17 , Q19-Q32	0.375 (DL1 0.385)
Processor (Al) 4028684-)502 (80249) RT-859A/ APX-72		DL1	A2-Use 4023632-0002	Q1-Q17, Q19-Q32	0.375 (DL-O.385)

Table 4-34. Component Mounting Information (Cont)

NOMENCLATURE AND ASSEMBLY NO.	BEAD 2054239-0701	ADHESIVE* MIL-A-46106	SPACER 4023758-0001	DISC 2025799-0702	MAXIMUM HEIGHT ABOVE CIRCUITBOARD (INCHES)
Decoder (A2) 4023412-0502 (RT-859/APX-72) or 4023412-0504 (RT-859A/APX-72)		C17, C23, C27	R43, R47, R49, R60, R85, R109, R137		0.405 (C17, C23, C27-0.415)
Decoder (A2) 4023412-0504 (80249) (RT-859A/APX-72)		C17, C23, C27		Ql, Q2, Q8-Q49	0.390 (C17, C23, C27-0.415)
Mode 4 (A3) 4023416 (RT-859/APX-72)		C6, C21, C31	R14, R54 R84, R85		0.390 (C6, C21, C31-0.415)
Mode 4 (A3) 4028683 (RT-859A/APX-72)	C38	C21, C31	R54, R84, R85 Use 4023758-0001		0.390 (C21, C3l-0.415)
Mode 4 (A3) 4028683-0502 (80249) (RT-859A/APX-72)		C21, C31		Q4-Q15, Q19-Q32, Q201-Q211	0.390 (C21, C31, C203, C205-0.415)
Mode 4 (A3) 116104-1 (RT-859A/APX-72)		Y1 *USE ADHESIVE HAZELTINE P/N 22663 OR EQUIVALENT.			0.41

Table 4-34. Component Mounting Information (Cont)

NOMENCLATURE AND ASSEMBLY NO.	BEAD 2054239-0701	ADHESIVE MIL-A-46106	SPACER 4023758-0001	DISC 2025799-0702	MAXIMUM HEIGHT ABOVE CIRCUITBOARD (INCHES)
Encoder Clock (A4) 2031111 RT-859/APX-72 or RT-859A/APX-72	C8, C13, C15, C19, C22, C23, C27, C36, C41		R15, R16, R42, R52, R80, R87, R94, R105, R106, R109, R110, R121, R125, R129, R132, R134		0.430
Encoder Clock (A4) 2031111-0502 (80249) (RT-859A/APX-72)				Q1-Q5, Q7-Q21, Q23-Q40 For A4A1 use 4023609-0001. For Q22, Q41 use 4023640-0701	0.430
Encoder Control (A5) 4023415 (RT-859/APX-72 or RT-859A/APX-72)			R14-R16, R20, R28-R30		0.440
Encoder Control (A5) 4023415-0502 (80249) (RT-859A/APX-72)	R11-R16, R45-R55 - Use sleeving C236205-22		A1-A4 - Use 4023517-0001	Q1-Q11	0.440

Table 4-34. Component Mounting Information (Cont)

NOMENCLATURE AND ASSEMBLY NO.	BEAD 2054239-0701	ADHESIVE MIL-A-46106	SPACER 4023758-0001	DISC 2025799-0702	MAXIMUM HEIGHT ABOVE CIRCUITBOARD (INCHES)
Encoder Gating (A6) 4023414-0502 (RT-859/APX-72 or RT-859A/APX-72)			R41, R73		0.330
Encoder Gating (A6) 4023414-0504 (80249) (RT-859A/APX-72)		C24 - Use 2077894-0001		Q1-Q21 For Q22 use 2025799-0703	
Modulator (A7) 4023408					0.380
Sensitivity (A8) 4023550					0.470
Video Amplifier (AR3) No. 1 4023448	C5, C6, C7				0.340
No. 2 4023449 (RT-859/APX-72 or RT-859A/APX- 72)					0.310 (VR1, VR2 - 0.350)

Table 4-34. Component Mounting Information (Cont)

NOMENCLATURE AND ASSEMBLY NO.	BEAD 2054239-0701	ADHESIVE MIL-A-46106	SPACER 4023758-0001	DISC 2025799-0702	MAXIMUM HEIGHT ABOVE CIRCUITBOARD (INCHES)
Video Amplifier (AR3) (80249) 124563-0501	C2, C16, L1, R7, R10, R24 - Use sleeving ST460125-1-22 L1 (body) - use sleeving ST461326-106				

1. Tools. Recommended tools, in addition to those normally supplied, consist of a torque screwdriver capable of measuring from 0 to 12 inch pounds. Refer to CAUTION preceding assembly instructions, paragraph 4-32q., for use of this special tool.

2. Special Instructions.

(a) RF Section. When remounting power amplifier (AR2), oscillator (22), amplifier (AR1), and preselector (21), a torque of 4 ±1 inch-pounds must be applied to each mounting screw. Refer to CAUTION preceding assembly instructions of paragraph 4-32q.

(b) Power Supply. The spare parts subassemblies for the power supply are listed under 2073404-0705 in table 4-35. These subassemblies are interchangeable with all previous subassemblies listed. When repairing power supply containing overcurrent subassembly 21435, it is recommended that this subassembly be replaced by 21435-1 as part of the repair procedure. Refer to instructions in table 4-35.

c. Assembly and Manufacture of Repair Parts. Repair parts which are to be assembled or manufactured at the Intermediate and Direct/General Support Maintenance level are source coded A, AF, M, or MF in the Illustrated Parts Breakdown Manual and A or M in the Repair and Spare Parts List. These documents will contain instructions for simple items of manufacture source coded M or MF, such as gaskets and washers, by providing information on type of material and thickness. The more complex repair parts listed in table 4-36, requiring outline drawings or schematics and detailed instructions, are described in this section.

1. Cable Assembly and Manufacture. The procedure for the assembly or manufacture of cables is divided into four general operations : preparation of the wires that make up the cable, preparation of a template for layout and formation of the cable, inserting and temporarily clamping wires to conform to template outline, and lacing the wires to provide the finished cable.

Table 4-35. Power Supply (PS1) Nonrepairable Subassemblies

FIGURE	REF DESIG	NOMENCLATURE	2073404-0704	2073404-0705
4-23	A1	Overcurrent	21435	*21435-1
4-23	A2	Switching Regulator	21431	21431-1
4-23, 4-26	A3	Inverter Driver	21443	21443-1
4-23, 4-25	A4	Output Rectifier	21447	21447-1
4-23	A5	High Voltage (21455)	22146	22146-1
4-23	A6	Interconnecting (21475) Cable	22145	22145-1
4-28	A7	Switching Regulator Driver	21439	21439
4-23, 4-27	A8	Filter Capacitor	21494	21494
4-28	FL1	RFI Filter	22653	22653
4-23, 4-25, 4-26.	FL2	Output Filter	21451	21451
4-23, 4-25, 4-26	FL3	Output Capacitor	21472	21472
4-23, 4-26	Q15/Q16	Inverter Driver	21474	21474
4-28		Harness	21499	21499
4-23, 4-28		Chassis	21493	21493

*Replacement spare 21435-1 (figure 4-22) has a wire lead attached to terminal E24. When replacinq overcurrent assembly 21435 with 21435-1, route this wire through hole in chassis assembly 21493 (5, figure 4-25) and connect to terminal E16 on inverter driver assembly 21443 (figure 4-25). When replacing overcurrent assembly 21435-1 with 21435-1, remove wire from terminal E24 of spare and discard it. Connect existing wire from terminal E16 of inverter driver assembly 21443 or 21443-1 to terminal E24.

In earlier versions of the power supply (PS1), the 1000 vdc return was grounded on the high voltage subassembly 21455 and through interconnecting cable subassembly 21475. Therefore, subassemblies 22146-1 and 22145-1 must be installed in pairs to provide continuity for the 1000 vdc return.

Table 4-36. Assembled and Manufactured Repair Parts List

Part Number	Source Code			Paragraph	Table	Figure Number
	USAF	ARMY	NAVY			
2031114-0501	A	AH	AF	4-27c.1.	4-37	4-30
2031117-0501	M		MF	4-27c.1.	4-38	4-31
2031116-0501	A		AF	4-27c.1.	4-39	4-32
4023580-0501	A	AH	AF	4-27c.2.	4-40	4-33

(a) Preparation of Wire. Tables 4-37 through 4-39 present the details for preparation of the wires that will form the applicable cable.

(1) Prepare tray or bins for each wire number listed in column 1.

(2) Select the type of wire (column 2 and specifications at bottom of table) color coded as shown in column 3 and cut to the approximate length shown in column 4.

(3) Strip the tin ends of each wire observing remarks column for any special details.

(b) Preparation of Template. The cable outlines on figures 4-30 through 4-32 are drawn to scale and can be used for this purpose if the scaled distances between registration marks are within tolerance.

(1) Fasten the cable assembly outline of applicable figure, or copy thereof, to a plywood backing or other suitable material.

(2) Place nails or pegs, as applicable, at bends and junctions of template to provide contour for forming wires.

(c) Forming the Cable. The order or sequence in which the wires are inserted to form the cable is not critical.

(1) Select a practical point on the template on which to start forming the cable.

(2) Select the numbered wire from the tray or bins corresponding to the number at the selected point on the template.

(3) Form wires on template observing beginning and ending wire numbers, and observing remarks column of table for any special route designations.

(4) Use temporary clamps to hold wires securely in place during this process.

(d) Lacing the Cable. To ensure that the assembled cable retains the form of the template, lace as follows:

(1) Lace the main trunk with a continuous single twist lock stitch having a maximum spacing between stitches of 0.5 inch (0.38 inch for front panel wiring assembly, figure 4-32). Stitch each side of all branches and before each breakout. (Cable 2, figure 4-30, sheet 2, has no main trunk.)

(2) Lace branches with a continuous single twist lock stitch having a maximum spacing between stitches of 0.38 inch (0.25 inch for front panel wiring assembly, figure 4-32). Stitch each side of all branches and before all breakouts on chassis cable (2, figure 4-30, sheet 2) and rf section wiring assembly, figure 4-31.

(3) Start lacing with a single stitch around a single wire followed by two twist lock stitches against each other around the complete bundle.

(4) Terminate the lacing by two twist lock stitches tied against each other around the complete bundle followed by a single stitch tied around a single wire.

Table 4-37. Wiring Assembly, Chassis (Part No. 2031114-0501)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
			CABLE NO. 1			
1	Connector & Wht-Coax.			XAIP1-22	P3-AR3-J1	Part No.
1A	Cable Assy	Black		XAIP1-Z		4023582-0501
2	AWG 24	Wht-Yel	12.5	P2-37	XPS1P1-10	
3	AWG 22	Wht-Gy	13.0	P2-62	XPS1P1-2	
4	AWG 24	Wht-Blk	3.0	P2-63	P2-64	
5						
6	AWG 22	Red	13.0	P2-66	XPS1P1-7	
7	AWG 22	Blk	13.0	P2-67	XPS1P1-9	
8	AWG 22	Gy	13.0	P2-91	XPS1P1-3	
9	AWG 24	Blk	8.0	P2-88	XA6P1 (GND)	
10	AWG 22	Blk	8.5	P2-40	XA6P1 (GND)	
11	AWG 22	Blk	11.5	P2-41	XA6P1 (GND)	
12	AWG 24	Blk	4.0	Wire, Braid (Shield) 76	XA6Pl (GND)	Detail D
13	AWG 24	Wht-Blk-Brn	11.0	P2-21	XA6P1-6	
14	AWG 24	Wht-Blu-Gy	10.5	P2-51	XA5P1-40	Detail D
15	AWG 24	Wht-Yel-Grn	11.0	P2-82	XA5P1-42	Detail D
16	AWG 24	Wht-Blu-Vio	10.5	P2-79	XA5P1-43	Detail D
17	AWG 24	Wht-Grn-Gy	10.5	P2-52	XA5P1-44	Detail D
18	AWG 24	Wht-Blk-Red	10.5	P2-22	XA6P1-9	
19	AWG 24	Wht-Grn-Vio	10.0	P2-30	XA5P1-46	Detail D
20	AWG 24	Wht-Red-Blu	10.0	P2-2	XA5P1-47	
21	AWG 24	Wht-Orn-Grn	10.0	P2-16	XA5P1-48	
22	AWG 24	Wht-Red-Yel	10.0	P2-18	XA5P1-49	
23	AWG 24	Wht-Red-Orn	10.0	P2-9	XA5P1-50	
24	AWG 24	Wht-Brn-Gy	9.5	P2-8	XA5P1-51	
25	AWG 24	Wht-Vio-Gy	9.5	P2-78	XA6P1-13	Detail D
26	AWG 24	Wht-Red-Gy	9.5	P2-6	XA5P1-52	
27	AWG 24	Wht-Red	9.0	P2-83	XA5P1-53	
28	AWG 24	Red	9.0	P2-55	XA5P1-54	
29	AWG 24	Grn	8.5	P2-86	XA5P1-55	
30	AWG 24	Wht-Gy	9.0	P2-56	XA5P1-57	
31	AWG 24	Wht-Blk	8.5	P2-59	XA5P1-58	
32	AWG 24	Vio	8.5	P2-34	XA5P1-59	
33	AWG 24	Wht-Brn-Grn	9.0	P2-3	XA5P1-60	
34	AWG 24	Wht-Brn-Orn	8.5	P2-10	XA5P1-61	
35	AWG 24	Wht-Grn-Blu	11.0	P2-80	XA5P1-6	Detail D
36	AWG 24	Wht-Yel-Gy	11.5	P2-53	XA5P1-7	Detail D
37	AWG 24	Wht-Yel-Vio	11.0	P2-31	XA5P1-8	Detail D
38	AWG 24	Wht-Yel-Blu	11.0	P2-81	XA5P1-9	Detail D

Table 4-37. Wiring Assembly, Chassis (Part No. 2031114-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
		CABLE NO. 1 (Cont)				
39	AWG 24	Wht-Orn-Gy	11.0	P2-54	XA5P1-11	Detail D
40	AWG 24	Wht-Orn-Vio	10.0	P2-32	XA5P1-13	
41	AWG 24	Wht-Orn-Blu	10.0	P2-5	XA5P1-14	
42	AWG 24	Wht-Red-Grn	10.0	P2-7	XA5P1-15	
43	AWG 24	Wht-Orn-Yel	10.0	P2-1	XA5P1-17	
44	AWG 24	Wht-Brn-Vio	9.5	P2-19	xA5P1-18	
45	AWG 24	Wht-Red-Vio	9.0	P2-17	XA5P1-19	
46	AWG 24	Wht- Grn	10.0	P2-71	XA4P1-L	
47	AWG 24	Blu	9.0	P2-57	XA5P1-20	
48	AWG 24	Gy	9.0	P2-84	XA5P1-21	
49	AWG 24	Yel	9.0	P2-35	xA5P1-22	
50	AWG 24	Orn	9.0	P2-58	XA5P1-23	
51	AWG 24	Wht	8.5	P2-87	xA5P1-24	
52	AWG 24	Brn	9.0	P2-85	XA5P1-25	
53	AWG 24	Wht-Brn-Blu	9.5	P2-11	xA5P1-26	
54	AWG 24	Wht-Brn-Yel	9.5	P2-24	xA5P1-27	
55	AWG 24	Wht-Brn-Red	9.5	P2-43	xA5P1-28	
56	AWG 24	Wht-Vio	12.0	P2-25	XA3P1-B	
57	AWG 24	Wht-Blu	11.5	P2-27	XA3P1-D	
58	AWG 24	Blu	11.0	P2-39	XA3P1-H	
59	RG-178 B/U	Coaxial Cable	11.0	P2-69	XA4P1-9	Details B and C
59A	AWG 24	Blk	2.0	Coax Shield	XA4P1-8 (GND)	Details C and E
59B	AWG 24	Blk	1.5	Coax Shield	P2-68	Details C and E
59C	AWG 24	Wht	1.5	Coax Center	XA4P1-9	Details C and E
60	RG-178 B/U	Coaxial Cable	11.0	P2-73	XA3P1-K	Details B and C
60A	AWG 24	Blk	2.0	Coax Shield	XA3P1-K (GND)	Details C and E
60B	AWG 24	Blk	1.5	Coax Shield	P2-46	Details C and E
60C	AWG 24	Wht	1.5	Coax Center	XA3P1-K	Details C and E
61	AWG 24	Wht-Orn	10.5	P2-20	XA4P1-11	
62	RG-178 B/U	Coaxial Cable	10.5	P2-72	XA3P1-M	Details B and C
62A	AWG 24	Blk	2.0	Coax Shield	XA3P1-M (GND)	Details C and E
62B	AWG 24	Blk	1.5	Coax Shield	P2-45	Detail C

Table 4-37. Wiring Assembly, Chassis (Part No. 2031114-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
		CABLE NO. 1 (Cont)				
62C	AWG 24	Wht	1.5	coax Center	XA3P1-M	Detail C
63	AWG 24	Wht-Blk-Gy	10.5	P2-26	XA3P1-P	
64	RG-178 B/U Coaxial Cable		9.5	P2-75	XA3P1-V	Detail C
64A	AWG 24	Blk	2.0	Coax Shield	XA3P1-V (GND)	Detail C
64B	AWG 24	Blk	1.5	Coax Shield	P2-48	Detail C
64C	AWG 24	Wht	1.5	Coax Center	XA3P1-V	Detail C
65	RG-178 B/U Coaxial Cable		8.0	P2-76	XA3P1-X	Detail C
65A	AWG 24	Blk	2.0	Coax Shield	XA3P1-X (GND)	Detail C
65B	AWG 24	Blk	1.5	Coax Shield	P2-49	Detail C
65C	AWG 24	Wht	1.5	Coax Center	XA3P1-X	Detail C
66	RT-178 B/U Coaxial Cable		12.5	P2-77	XA3P1-1	Detail C
66A	AWG 24	Blk	2.0	Coax Shield	XA3P1-2 (GND)	Detail C
66B	AWG 24	BLK	1.5	Coax Shield	P2-50	Detail C
66C	AWG 24	Wht	1.5	Coax Center	XA3P1-1	Detail C
67	AWG 24	Wht-Brn	12.5	P2-44	XA3P1-3	
68	RG-178 B/U Coaxial Cable		11.0	P2-60	XA2P1-36	Detail C
68A	AWG 24	Blk	2.0	Coax Shield	XA2P1-36 (GND)	Detail C
68B	AWG 24	Blk	1.5	Coax Shield	P2-61	Detail C
68C	AWG 24	Wht	1.5	Coax Center	XA2P1-36	Detail C
69	AWG 24	Wht-Blk-Orn	12.0	P2-42	XA2P1-41	
70	AWG 24	Wht-Blk-Blu	11.0	P2-36	XA2P1-47	
71	AWG 24	Wht-Blk-Vio	9.5	P2-15	XA2P1-54	
72	AWG 24	Wht-Blk-Grn	9.5	P2-33	XA2P1-58	
73	AWG 24	Wht-Blk-Yel	9.5	P2-23	XA2P1-62	
74	RG-178 B/U Coaxial Cable		9.0	P2-74	XA3P1-20	Details B and C

Table 4-37. Wiring Assembly, Chassis (Part No. 2031114-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
			CABLE NO. 1 (Cont)			
74A	AWG 24	Blk	2.0	Coax Shield	XA3P1-20 (GND)	Details C and E
74B	AWG 24	Blk	1.5	Coax Shield	P2-47	Details C and E
74C	AWG 24	Wht	1.5	Coax Center	XA3P1-20	Details C and E
75	RG-178 B/U Coaxial Cable		12.0	P2-89	XA2P1-4	Details B and C
75A	AWG 24	Blk	2.0	Coax Shield	XA2P1-4 (GND)	Details C and E
75B	AWG 24	Blk	1.5	Coax Shield	P2-90	Details C and E
75C	AWG 24	Wht	1.5	Coax Center	XA2P1-4	Details C and E
76	Braid, Wire		3.50 ±0.12	Belden Part No. 8660		Detail D
77	Ferrule Grounding		0. 750	Rayclad Part No. D103		Detail D
78	Insulating Sleeving	Clear	3.50 ±0.12	Rayclad Part No. RNF-100-3/8		Detail D
79	Ferrule Grounding	Blu	0.6 ±0.04	Rayclad Part No. D-144-09		Details C and E
80	Ferrule Grounding	Blu	0.406 ±0.04	Rayclad Part No. D-110-00		Details C and E
81	Sleeve Marker (9)	Wht	0.75 +0.06	MIL-I-23053		Detail C and Table 1
82	Contact Electrical			Deutsch 2803-10-0000		Detail C
83	Connector Plug, Elec.	P2			J2	Part No. RSMO7-27-30S
			CABLE NO. 2			
1	AWG 24	Red	3.5	XPS1P1-5	XA6P1-C	
2	AWG 24	Grn	5.0	XPS1P1-13	XA6P1-L	
3	AWG 24	Orn	5.5	XPS1P1-4	XA6P1-R	
4	RG-178 B/U Coax Cable		5.0	XA4P1-10	XPS1P1-A2	Detail K
4B	AWG 24	Blk	1.5	Coax Shield	XA3P1 (GND)	Details M and E
4C	AWG 24	Wht	1.5	Coax Center	XA4P1-10	Details M and E
5	AWG 24	Blu	4.5	XPS1P1-1	XA3P1-H	
6	AWG 24	Yel	4.0	XPS1P1-14	XA3P1-F	

Table 4-37. Wiring Assembly, Chassis (Part No. 2031114-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
			CABLE NO. 2 (Cont)			
7	RG-178 B/U	Coax Cable	7.0	XPS1P1-6	XA2P1-28	Detail L
7A	AWG 24	Blk	2.0	Coax Shield	XPS1P1-12	Details C and E
7B	AWG 24	Blk	2.0	Coax Shield	XA2P1-29 (GND)	Details C and E
7C	AWG 24	Wht	2.0	Coax Center	XA2P1-28	Details C and E
8	AWG 24	Blk	3.5	XPS1P1-11	XA6P1 (GND)	
9	AWG 24	Wht-Blk	5.5	XPS1P1-15	XA2P1-10	
10	AWG 24	Wht-Orn	4.5	XA6P1-16	XA5P1-36	
11	AWG 24	Blu	4.0	XA6P1-15	XA5P1-37	
12	AWG 24	Wht-Grn-Gy	4.0	xA6P1-14	XA5P1-39	
13	AWG 24	Yel	3.5	XA6P1-11	XA5P1-65	
14	AWG 24	Orn	3.5	XA5P1-29	XA4P1-M	
15	AWG 24	Wht-Blk-Grn	3.0	XA5P1-4	XA4P1-N	
16	AWG 24	Wht-Blk-Orn	4.5	XA5P1-3	XA4P1-V	
17	AWG 24	Wht-Red-Gy	5.0	XA3P1-18	XA2P1-35	
18	AWG 24	Orn	4.5	XA3P1-4	XA2P1-59	
19	AWG 24	Gy	6.0	XA6P1-P	XA4P1-C	
20	AWG 24	Wht	5.5	XA6P1-F	XA5P1-5	
21	AWG 24	Wht-Gy	8.5	XA6P1-X	XA4P1-J	
22	AWG 24	Wht	6.5	XA6P1-K	XA5P1-10	
23	AWG 24	Red	5.5	XA6P1-C	XA5P1-12	
24	AWG 24	Blu	7.0	XA6P1-J	XA5P1-16	
25	AWG 24	Orn	9.5	XA6P1-R	XA5P1-29	
26	AWG 24	Wht-Brn	10.5	XA6P1-Y	XA5P1-33	
27	AWG 24	Vio	11.0	XA6P1-M	XA4P1-X	
28	AWG 24	Wht-Blu	9.5	XA6P1-U	XA4P1-14	
29	AWG 24	Wht-Red	10.0	XA6P1-T	XA4P1-18	
30	AWG 24	Grn	8.0	XA6P1-L	XA5P1-62	
31	AWG 24	Red	6.5	XA6P1-C	XA2P1-44	
32	AWG 24	Brn	9.0	XA6P1-S	XA5P1-63	
33	AWG 24	Wht-Blk	6.0	XA5P1-34	XA4P1-P	
34	AWG 24	Wht-Blk-Gy	6.0	XA5P1-35	XA4P1-R	
35	AWG 24	Wht-Orn	5.5	XA5P1-36	XA4P1-S	
36	AWG 24	Blu	6.5	XA5P1-37	XA4P1-U	
37	AWG 24	Wht	6.5	XA5P1-38	XA4P1-15	
38	AWG 24	Wht-Blk-Vio	5.0	XA5P1-41	XA4P1-2	
39	AWG 24	Wht-Vio	5.0	XA6P1-10	XA5P1-2	
40	AWG 24	Wht-Blk-Red	8.0	XA6P1-9	XA5P1-30	
41	AWG 24	Wht-Grn	9.0	XA6P1-17	XA4P1-13	

Table 4-37. Wiring Assembly, Chassis (Part No. 2031114-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 * *REMARKS
			CABLE NO. 2 (Cont)			
42	AWG 24	Wht-Yel	7.0	XA6P1-19	XA4P1-1	
43	AWG 24	Brn	7.5	XA5P1-63	XA4P1-6	
44	AWG 24	Grn	7.5	XA5P1-62	XA4P1-H	
45	AWG 24	Wht-Blk	10.0	XA5P1-66	XA4P1-17	
46	AWG 24	Wht-Blk-Yel	9.5	XA6P1-21	XA4P1-T	
47	AWG 24	Wht-Vio	4.0	XA5P1-2	XA4P1-3	
48	AWG 24	Wht-Brn-Blu	7.0	XA4P1-A	XA2P1-20	
49	AWG 24	Wht-Brn-Vio	7.0	XA4P1-B	XA2P1-61	
50	AWG 24	Wht-Brn-Gy	7.0	XA4P1-D	XA2P1-57	
51	AWG 24	Wht-Brn-Yel	7.5	XA4P1-F	XA2P1-15	
52	AWG 24	Grn	5.0	XA4P1-H	XA3P1-C	
53	AWG 24	Wht	5.5	XA5P1-10	XA4P1-4	
54	AWG 24	Orn	6.5	XA4P1-M	XA3P1-4	
55	AWG 24	Blu	6.5	XA5P1-16	XA4P1-7	
56	AWG 24	Wht	11.5	XA4P1-Z	XA2P1-31	
57	AWG 24	Grn	5.5	XA3P1-C	XA2P1-51	
58	AWG 24	Yel	6.5	XA3P1-F	XA2P1-56	
59	AWG 24	Wht-Orn-Blu	5.0	XA3P1-K	XA2P1-37	
60	AWG 24	Wht-Red-Grn	8.0	XA3P1-J	XA2P1-24	
61	AWG 24	Wht-Red-Vio	9.0	XA3P1-S	XDL1P1-11	
62	AWG 24	Wht-Red-Blu	9.0	XA3P1-T	XDL1P1-13	
63	AWG 24	Wht	8.0	XA3P1-Z	XA2P1-3	
64	AWG 24	Wht-Orn-Yel	9.5	XA3P1-U	XA2P1-25	
65	AWG 24	Wht-Red-Yel	6.5	XA3P1-R	XA2P1-2	
66	AWG 24	Wht-Red-Gy	5.0	XA2P1-35	XA1P1-F	
67	AWG 24	Wht	7.0	XA2P1-39	XA2P1-31	
68	AWG 24	Red	6.5	XA2P1-44	XA1P1-6	
69	AWG 24	Wht-Orn	7.5	XA2P1-43	XDL1P1-14	
70	AWG 24	Wht-Yel	8.5	XA2P1-50	XDL1P1-15	
71	AWG 24	Grn	7.0	XA2P1-51	XA1P1-C	
72	AWG 24	Wht-Blu	8.5	XA3P1-12	XA2P1-32	
73	AWG 24	Yel	7.5	XA2P1-56	XA1P1-J	
74	AWG 24	Orn	7.5	XA2P1-59	XA1P1-H	
75	AWG 24	Wht-Yel-Vio	9.0	XA2P1-60	XDLIP1-12	
76	AWG 24	Wht-Yel-Blu	8.5	XA2P1-63	XDL1P1-10	
77	AWG 24	Wht-Orn-Vio	6.5	XA2P1-1	XA1P1-Y	
78	AWG 24	Wht	5.5	XA2P1-3	XDL1P1-8	
79	AWG 24	Wht-Red	6.0	XA2P1-16	XDL1P1-7	
80	AWG 24	Wht	8.5	XA2P1-21	XDL1P1-22	
81	Contact Electrical	Part No. 2004803-0703		ITT Cannon Part No. DM53743-5000		Details M and N
82	AWG 24	Wht-Orn-Yel	7.5	XA2P1-25	XDLIP1-9	
83	AWG 24	Wht-Blk	6.0	XDLIP1-4	XAIP1-11	

Table 4-37. Wiring Assembly, Chassis (part No. 2031114-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
			CABLE NO. 2 (Cont)			
84	AWG 24	Wht	6.0	XDL1P1-8	XA1P1-5	
85	AWG 24	Wht-Blk	6.0	XA2P1-10	XA1P1-K	
86	Connector Receptacle			Cannon Part No. DBM-17W2S		Detail P
87	Ferrule Grounding	Blu	0.406 ±0.040	Rayclad Part No. D-110-00		Details M and E
88	Ferrule Grounding	Blu	±.06 +0.040	Rayclad Part No. D-144-09		Details M and E
89	Insulation Sleeving		±.38 +0.06	Hytemp Part No. TUX-15		Detail P
90	AWG 24	Wht	4.0	XA3P1-6	XA1P1-2	Wires No. 90 and 91 apply for RT-859A/ APX-72 only. See figure 4-31.
91	AWG 24	Wht	9.0	XA3P1-W	XA1P1-19	

AWG SIZE	CONDUCTOR DIA NOMINAL	NO. OF STRANDS MINIMUM	MAX DC RESISTANCE OHMS/1000 FT AT 25°C	DIA OVER INSULATION MAXIMUM	ITEMS
24	0.024	16	26.8	0.40	CABLE NO. 1 - 2, 4, 9, 12-58, 59A, B, C, 60A, B, 61, 62A, B, C, 63, 64A, B, C, 65A, B, C, 66A, B, C, 67, 68A, B, C, 69, 73, 74A, B, C, and 75A, B, C. CABLE NO. 2 - 1-3, 4B, C, 5, 6, 7A, B, C, 8-80, and 82-85.
22	0.030	19	16.7	0.054	CABLE NO. 1 - 3, 6-8, 10, 11.

*Wire Type Specifications MIL-W-16878, Insulation Teflon MIL-M-14077

**See figure 4-30.

Table 4-38. Wiring Assembly, RF Section (Part No. 2031117-0501)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
1	RG-178 B/U	N/A	7.25	A2 (Conductor) CP2 (Shield)	A7-2 (Conductor) A7-3 (Shield)	See Detail C
2	AWG 24	Blk	8.0	A7-10	E6	
3	AWG 24	Blk	17.0	AR3-3	E6	Route B
4	AWG 24	Grn	18.0	AR3-2	FL7	Route A
5	AWG 24	Grn	8.5	A7-4	FL7	
6	AWG 24	Orn	17.5	AR3-1	FL6	Route A
7	AWG 24	Red	8.0	A7-6	FL9	
8	AWG 24	Blu	4.0	A8-2	FL8	Route B
9	AWG 24	Wht-Red	3.5	FL16-3	FL10	Route B
10	AWG 22	Brn	8.5	FL11	AR2-2	
11	AWG 24	Wht-Yel	4.0	A8-3	FL12	Route B
12	AWG 24	Wht-Blk	7.5	A7-7	FL13	
13	AWG 24	Yel	7.5	A7-1	FL14	
14	AWG 22	Blk	8.5	FL15	AR2-1	
15	AWG 22	Blk	15.5	AR1-10	FL15	Route A
16	AWG 24	Wht-Gy	15.5	AR3-4	A8-1	
17	AWG 24	Wht-Red	9.5	AR1-7	A8-4	Route B
18	AWG 24	Grn	12.0	AR1-4	A8-5	
19	AWG 24	Grn	8.5	AR1-1	AR1-4	
20	AWG 22	Brn	7.0	AR1-8	FL1l	Route A
21	AWG 22	Brn	9.0	AR1-5	AR1-8	
22	AWG 22	Brn	7.0	AR1-2	AR1-5	
23	AWG 24	Wht-Orn	8.0	AR1-9	A8-6	Route B
24	AWG 24	Wht-Blk	11.0	AR1-6	A8-7	Route B
25	AWG 24	Wht-Blu	13.5	AR1-3	A8-8	Route B
26	AWG 24	Blk	11.0	AR2-1	E8	
27	AWG 24	Blk	4.0	E8	Modulation Output Grd	
28	AWG 24	Wht	5.5	E7	Modulation Sample output	
29	AWG 24	Wht	7.5	A7-5	AR2-3	
30	AWG 22	Blk	12.0	Z2-3	AR2-1	
31	AWG 22	Brn	12.0	AR2-2	Z2-4	
32	RG-178 B/U	N/A	10.62	A7-8 (Conductor) A7-9 (Shield)	Z2-2 (Conductor) Z2-1 (Shield)	See Detail D
33	AWG 24	Blk	2.5	A8-9	E6	
34	AWG 24	Wht-Grn	18.5	AR3-5	E9	Route A
35	AWG 22	Bare	2.5	Shield Wire 1	A7-3	Detail C

Table 4-38. Wiring Assembly, RF Section (Part No. 2031117-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
36	AWG 22	Bare	2.5	Shield Wire 32	A7-9	Detail D
37	AWG 22	Bare	2.5	Shield Wire 32	Z2-1	Detail D

AWG SIZE	CONDUCTOR DIA NOMINAL	NO. OF STRANDS MINIMUM	MAX DC RESISTANCE OHMS/1000 FT AT 25°C	DIA OVER INSULATION MAXIMUM	ITEMS
24	0.024	19	26.8	0.048	2-9, 11-13, 16-19, 23-29, 33, 34
22	0.030	19	16.7	0.054	10, 14, 15, 20-22, 30, 31
22	0.0253			Bare	35-37

*Wire Type Specifications MIL-W-16878, Insulation Teflon MIL-M-14077

**See figure 4-32

Table 4-39. Wiring Assembly, Front Panel (Part No. 2031116-0501)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 F ROM	6 TO	7 **REMARKS
1	AWG 24	Blk	8.0	J2-38	S1-AC	
2	AWG 24	Wht-Blk	8.0	J2-59	S1-A1	
3	AWG 24	Wht	8.0	J2-87	S1-A2	
4	AWG 24	Orn	8.0	J2-58	S1-A4	
5	AWG 24	Yel	8.5	J2-35	S1-B1	
6	AWG 24	Blu	8.5	J2-57	S1-B4	
7	AWG 24	Grn	8.5	J2-86	S1-B2	
8	AWG 24	Vio	9.0	J2-34	S1-C1	
9	AWG 24	Brn	9.0	J2-85	S1-C2	
10	AWG 24	Wht-Gy	9.0	J2-56	S1-C4	
11	AWG 24	Gy	9.5	J2-84	S1-D1	
12	AWG 24	Red	9.5	J2-55	S1-D2	
13	AWG 24	Wht-Red	9.5	J2-83	S1-D4	

Table 4-39. Wiring Assembly, Front Panel (Part No. 2031116-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
14	RG-178 B/U	Coaxial Cable	10.0	J2-76	J1-9	Details C, E, F, and G
14A	AWG 24	Blk	2.0	J2-49	Coax Shield	Detail G
15	RG-178 B/U	Coaxial Cable	9.5	J2-77	J1-10	Details C, E, F, and G
15A	AWG 24	Blk	2.0	J2-50	Coax Shield	Detail G
16	RG-178 B/U	Coaxial Cable	9.5	J2-60	J1-11	Details C, E, F, and G
16A	AWG 24	Blk	2.0	J2-61	Coax Shield	Detail G
17	RG-178 B/U	Coaxial Cable	9.0	J2-89	J1-12	Details C, E, F, and G
17A	AWG 24	Blk	2.0	J2-90	Coax Shield	Detail G
18	RG-178 B/U	Coaxial Cable	9.0	J2-69	J1-13	Details C, E, F, and G
18A	AWG 24	Blk	2.0	J2-68	Coax Shield	Detail G
19	RG-178 B/U	Coaxial Cable	10.0	J2-75	J1-45	Details C, E, F, and G
19A	AWG 24	Blk	2.0	J2-48	Coax Shield	Detail G
20	RG-178 B/U	Coaxial Cable	10.0	J2-74	J1-46	Details C, E, F, and G
2OA	AWG 24	Blk	2.0	J2-47	Coax Shield	Detail G
21	RG-178 B/U	Coaxial Cable	10.0	J2-73	J1-47	Details C, E, F, and G
21A	AWG 24	Blk	2.0	J2-46	Coax Shield	Detail G
22	RG-178 B/U	Coaxial Cable	9.5	J2-72	J1-48	Details C, E, F, and G

Table 4-39. Wiring Assembly, Front Panel (Part No. 2031116-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
22A	AWG 24	Blk	2.0	J2-45	Coax Shield	Detail G
23	AWG 22	Wht	9.5	J2-66	J1-49	Detail D
24	AWG 24	Wht-Grn-Vio	8.5	J2-30	J1-31	Detail H
25	AWG 24	Wht-Yel-Vio	8.5	J2-31	J1-17	Detail H
26	AWG 24	Wht-Blu-Gy	9.0	J2-51	J1-41	Detail H
27	AWG 24	Wht-Grn-Gy	9.0	J2-52	J1-32	Detail H
28	AWG 24	Wht-Yel-Gy	8.5	J2-53	J1-23	Detail H
29	AWG 24	Wht-Orn-Gy	8.5	J2-54	J1-8	Detail H
30	AWG 24	Wht-Vio-Gy	9.0	J2-78	J1-42	Detail H
31	AWG 24	Wht-Blu-Vio	8.5	J2-79	J1-35	Detail H
32	AWG 24	Wht-Grn-Blu	8.5	J2-80	J1-30	Detail H
33	AWG 24	Wht-Yel-Blu	9.0	J2-81	J1-55	Detail H
34	AWG 24	Wht-Yel-Grn	9.0	J2-82	J1-54	Detail H
35	AWG 24	Wht-Orn-Blu	3.5	J2-5	FL1-44	
36	AWG 24	Wht-Brn-Orn	4.0	J2-10	FL1-41	
37	AWG 24	Wht-Orn-Grn	4.0	J2-16	FL1-45	
38	AWG 24	Wht-Brn-Yel	3.5	J2-24	FL1-40	
39	AWG 24	Wht-Orn-Vio	3.5	J2-32	FL1-43	
40	AWG 24	Wht-Brn-Red	4.0	J2-43	FL1-42	
41	AWG 24	Wht-Brn-Grn	4.0	J2-3	FL1-39	
42	AWG 24	Wht-Brn-Blu	4.0	J2-11	FL1-38	
43	AWG 24	Wht-Brn-Vio	4.0	J2-19	FL1-37	
44	AWG 24	Wht-Blk-Red	4.0	J2-22	FL1-47	
45	AWG 24	Wht-Vio	4.0	J2-25	FL1-46	
46	AWG 24	Wht-Blk-Gy	4.0	J2-26	FL1-48	
47	AWG 24	Wht-Brn-Gy	4.5	J2-8	FL1-36	
48	AWG 24	Wht-Red-Orn	4.5	J2-9	FL1-35	
49	AWG 24	Wht-Red-Yel	4.5	J2-18	FL1-34	
50	AWG 24	Wht-Orn	4.5	J2-20	FL1-51	
51	AWG 24	Wht-Blk-Brn	4.5	J2-21	FL1-49	
52	AWG 24	Wht-Grn	4.5	J2-71	FL1-50	
53	AWG 24	Wht-Red-Blu	5.0	J2-2	FL1-32	
54	AWG 24	Wht-Red-Grn	5.0	J2-7	FL1-33	
55	AWG 24	Wht-Red-Vio	5.0	J2-17	FL1-31	
56	AWG 24	Wht-Blk-Blu	5.0	J2-36	FL1-53	
57	AWG 24	Wht-Yel	5.0	J2-37	FL1-52	
58	AWG 24	Wht-Orn-Yel	5.5	J2-1	FL1-29	
59	AWG 24	Wht-Red-Gy	5.5	J2-6	FL1-30	
60	AWG 24	Wht-Blk-Yel	5.5	J2-23	FL1-55	
61	AWG 24	Wht-Blk-Grn	5.5	J2-33	FL1-54	
62	AWG 24	Wht-Blk-Orn	5.5	J2-42	FL1-56	
63	AWG 22	Blu	8.5	J2-39	K2-X2	

Table 4-39. Wiring Assembly, Front Panel (Part No. 2031116-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
64	AWG 24	Wht-Blk	7.5	J2-63	K1-X1	
65	AWG 24	Wht-Brn	8.5	J2-44	K2-X1	
66	AWG 22	Blk	5.0	J2-40	E1	
67	AWG 22	Blk	5.0	J2-41	E1	
68	AWG 22	Blk	5.0	J2-67	E1	
69	AWG 24	Wht-Blk	8.5	J2-64	J1-20	
70	AWG 24	Wht-Blk-Vio	9.0	J2-15	J1-59	
71	AWG 24	Wht-Blu	4.0	J2-27	FL5-1	
72	AWG 22	Wht-Gy	4.0	J2-62	FL3-1	
73	AWG 22	Gy	3.5	J2-91	FL2-1	
74	AWG 22	Wht-Gy	6.5	J1-1	FL3-2	
75	AWG 22	Red	12.5	J1-2	K1-A2	
76	AWG 22	Blk	11.0	J1-3	E1	
77	AWG 24	Wht-Blk-Orn	9.0	J1-4	FL1-15	
78	AWG 22	Gy	7.5	J1-5	F1-1	
79	AWG 22	Wht-Red	6.5	J1-6	F2-1	
80	AWG 22	Wht	7.0	J1-7	FL2-2	
81	AWG 24	Wht-Yel	8.5	J1-14	FL1-19	
82	AWG 24	Wht-Blk-Grn	8.5	J1-15	FL1-17	
83	AWG 24	Wht-Orn	8.0	J1-16	FL1-20	
84	AWG 24	Wht-Blk-Blu	8.5	J1-18	FL1-18	
85	AWG 24	Wht-Blk-Red	7.0	J1-19	FL1-24	
86	AWG 24	Wht-Blk-Brn	7.5	J1-21	FL1-22	
87	AWG 24	Wht-Blk-Yel	9.0	J1-22	FL1-16	
88	AWG 24	Wht-Red-Blu	8.5	J1-24	FL1-11	
89	AWG 24	Wht-Red-Grn	8.5	J1-25	FL1-10	
90	AWG 24	Wht-Red-Yel	8.0	J1-26	FL1-9	
91	AWG 24	Wht-Red-Orn	8.0	J1-27	FL1-8	
92	AWG 24	Wht-Brn-Gy	8.0	J1-28	FL1-7	
93	AWG 24	Wht-Brn-Vio	7.5	J1-29	FL1-6	
94	AWG 24	Wht-Grn	7.5	J1-33	FL1-21	
95	AWG 24	Wht-Blu	7.0	J1-34	FL5-2	
96	AWG 24	Wht-Brn-Blu	7.5	J1-36	FL1-5	
97	AWG 24	Wht-Brn-Grn	7.5	J1-37	FL1-4	
98	AWG 24	Wht-Brn-Yel	7.0	J1-38	FL1-3	
99	AWG 24	Wht-Brn-Orn	7.0	J1-39	FL1-2	
100	AWG 24	Wht-Brn-Red	7.0	J1-40	FL1-1	
101	AWG 24	Wht-Red-Vio	8.5	J1-43	FL1-12	
102	AWG 24	Wht-Red-Gy	9.0	J1-44	FL1-13	
103	AWG 24	Wht-Orn-Yel	9.0	J1-50	FL1-14	
104	AWG 24	Wht-Blk-Gy	7.5	J1-51	FL1-23	
105	AWG 24	Wht-Vio	7.5	J1-52	FL1-25	
106	AWG 22	Brn	13.5	J1-53	K2-B3	

Table 4-39. Wiring Assembly, Front Panel (Part No. 2031116-0501) (Cont)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
107	AWG 24	Wht-Orn-Grn	7.0	J1-56	FL1-26	
108	AWG 24	Wht-Orn-Blu	7.0	J1-57	FL1-27	
109	AWG 24	Wht-Orn-Vio	7.5	J1-58	FL1-28	
110	AWG 22	Gy	13.0	F1-2	K1-B2	
111	AWG 22	Gy	10.5	FL2-2	K1-B1	
112	AWG 22	Wht-Red	11.5	F2-1	K1-A1	
113	AWG 22	Wht-Red	6.0	F2-2	FL4-2	
114	AWG 22	Blk	9.5	MI-MINUS	E1	
115	AWG 22	Wht-Red	10.0	FL4-1	K2-X2	
116	AWG 22	Wht	3.5	MI-PLUS	F2-2	
117	AWG 22	Red	11.0	FL4-1	J1-49	Detail D
118	AWG 24	Blk	3.5	Wire Braid	E4	Detail H
119	Insulating Sleeving	Natural	0.25 ±.06	Hi-Temp Part No. TUX-16		Details C, J
120	Insulating Sleeving	Natural	±.38 ±.06	Hi-Temp Part No. TUX-17		Details C, G, J
121	Ferrule Grounding	Blu	±.75 ±.062	Rayclad Part No. D-103		Detail H
122	Sleeving Marker (9)	Wht	±.75 ±.06	MIL-I-23053		Detail G and Table 1
123	Insulation Sleeving	Clear	5.0 ±.12	Rayclad Part No. RNF-100-3/8		Detail H
124	Ferrule Grounding	Blu	±.6 ±.04	Rayclad Part No. D-144-09		Detail G
125	Braid, Wire		4.7 ±.06	Belden Part No. 8660		Detail H
126	Connector, J1			ITT Cannon Part No. DP J-5901O-33P-B-2		
127	Connector, J2			Sealtron Part No. 8415-27-3DP		
128	Shielding, Electrical			Birnbach Part No. 858		Details C, E
129	Retainer, Electrical Wire			Bendix Part No. 2073104-0002		Detail D
130	Bushing, Insulating		0.25	MIL-P-19468		Detail D
131	Retainer, Electrical Wire			Bendix Part No. 2073104-0001		Details E, G

Table 4-39. Wiring Assembly, Front Panel (Part No. 2031116-0501) (Cont)

AWG SIZE	CONDUCTOR DIA NOMINAL	NO. OF STRANDS MINIMUM	MAX DC RESISTANCE OHMS/1000 FT AT 25°C	DIA OVER INSULATION MAXIMUM	ITEMS
24	0.024	19	26.8	0.048	
22	0.030	19	16.7	0.054	

*Wire Type Specifications MIL-W-16878, Insulation Teflon MIL-M-14077.

**See figure 4-33.

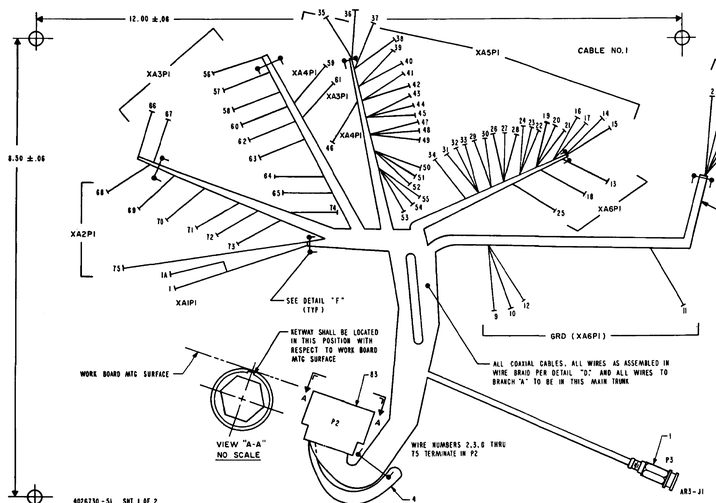
2. Connector and Filter Assembly. To assemble the connector and filter assembly (figure 4-34), procure the components listed in the Illustrated Parts Breakdown or the Repair Parts and Special Tools List and proceed as follows:

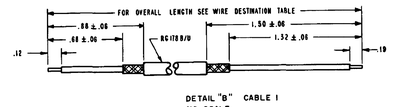
(a) prepare wire and insulation sleeving as detailed in table 4-40, stripping each wire 1/4-inch and 1/8-inch, respectively, with the exception of wire 1 which is stripped 5/16-inch and 1/8-inch.

(b) Insert A1 contact in connector XPS1P2, position connector as shown in figure 4-34, connect and solder 1/8-inch end of wires (1 through 15) and install insulated sleeving (16 and 17) as indicated on wiring assembly diagram and table 4-40.

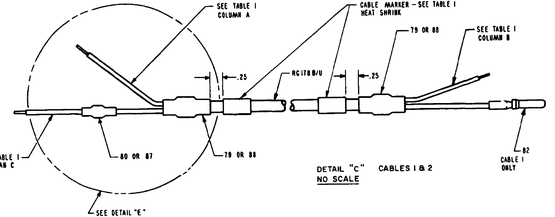
(c) See detail B, figure 4-34. Mount with connecting hardware provided, capacitor C1, terminal lugs E5 and E6. press insulated feedthrough terminals E7 and E9 from external side of assembly into openings provided. Mount previously wired connector XPS1P2 using guide pins and washers provided.

(d) Refer to wiring assembly, figure 4-34, and connect the solder leads from base of connector XPS1P2, as indicated, observing color coding and annotated instructions.

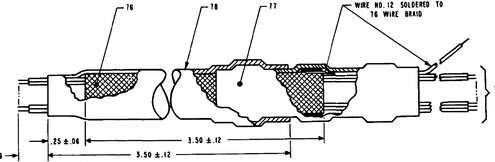




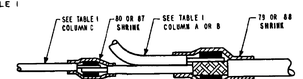
DETAIL "B" CABLE 1
NO SCALE



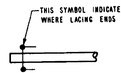
DETAIL "C" CABLES 1 & 2
NO SCALE



DETAIL "D" CABLE 1
NO SCALE



DETAIL "E" CABLES 1 & 2
NO SCALE



DETAIL "F" CABLES 1 & 2
NO SCALE

TABLE I				
COAX CABLE WIRE NO.	GROUND WIRE NO.		CENTER CONDUCTOR	CABLE MARKER NO.
	A	B	C	
CABLE NO.1				
59	59A	59B	59C	23
60	60A	60B	60C	26
62	62A	62B	62C	27
64	64A	64B	64C	24
65	65A	65B	65C	19
66	66A	66B	66C	20
68	68A	68B	68C	21
74	74A	74B	74C	25
75	75A	75B	75C	22
CABLE NO.2				
4	—	4B	4C	—
7	7A	7B	7C	—

Figure 4-30. Wiring Assembly Chassis (Part No. 2031114-0501), RT-859/APX-72 (Sheet 1 of 2)

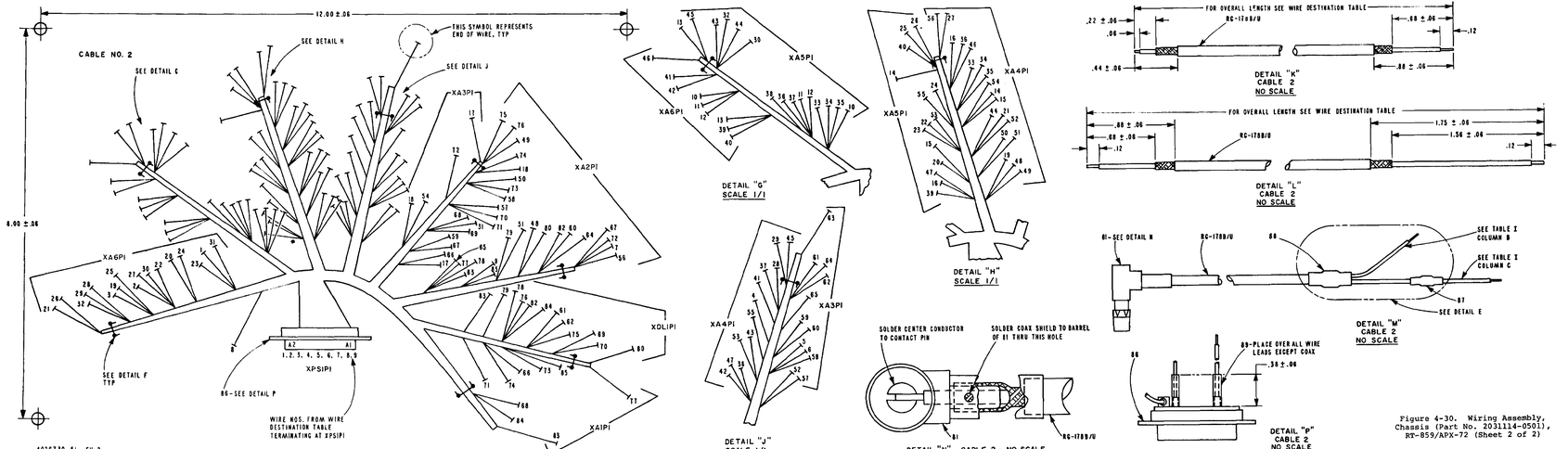


Figure 4-30. Wiring Assembly, Chassis (Part No. 2031114-0501), RT-859/APX-72 (Sheet 2 of 2)

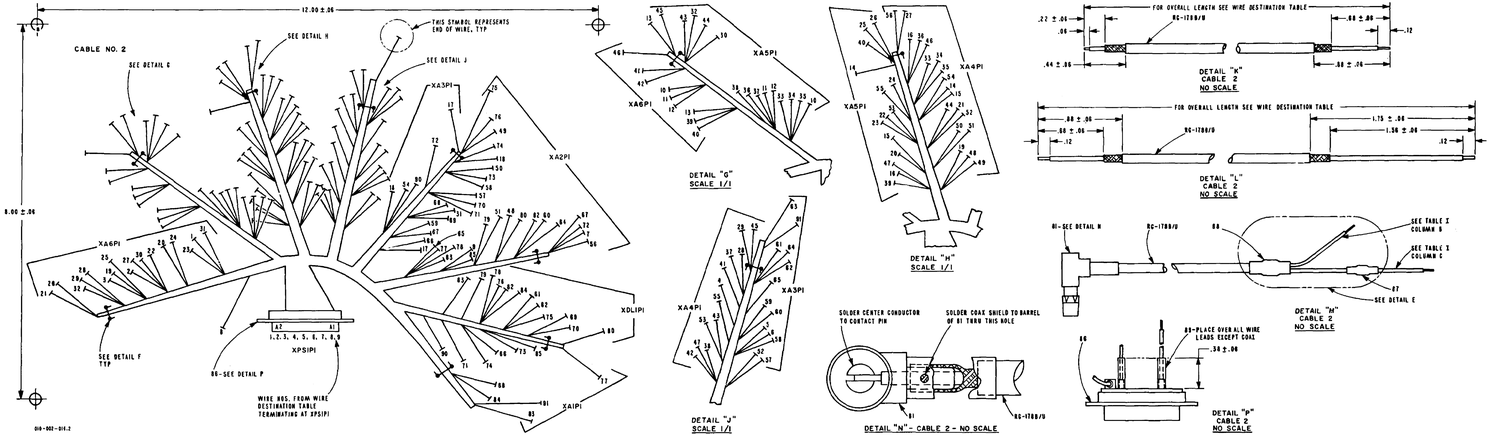
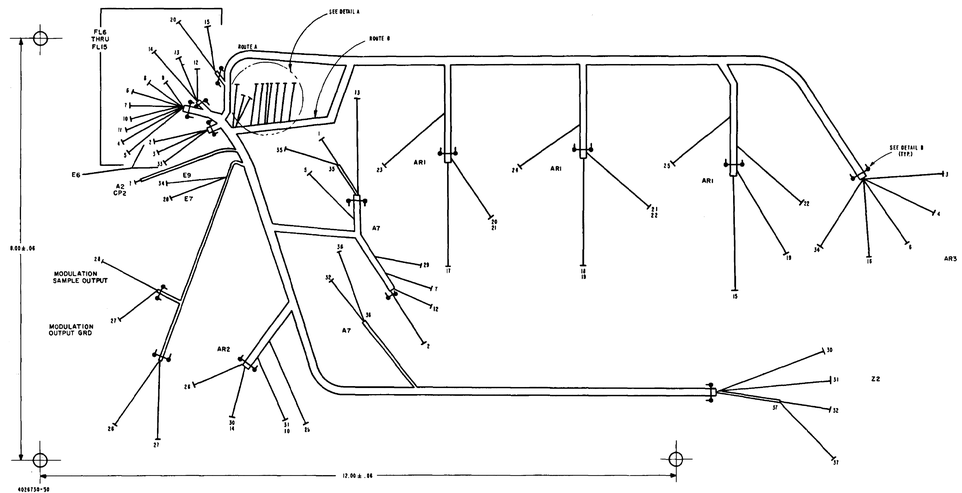
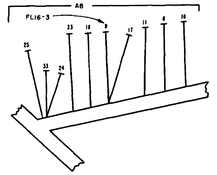
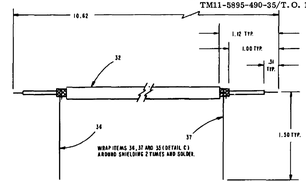


Figure 4-31. Wiring Assembly, Chassis (Part No. 2031114-050), RT-859A/APX-72

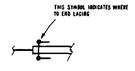




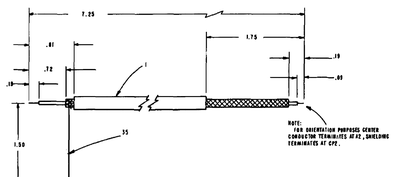
DETAIL "A"
SCALE 2/1



DETAIL "D"
SCALE 1/1



DETAIL "B"
NO SCALE



DETAIL "C"
SCALE 1/1

Figure 4-32. Wiring Assembly, RF Section (Part No. 2031117-0501)

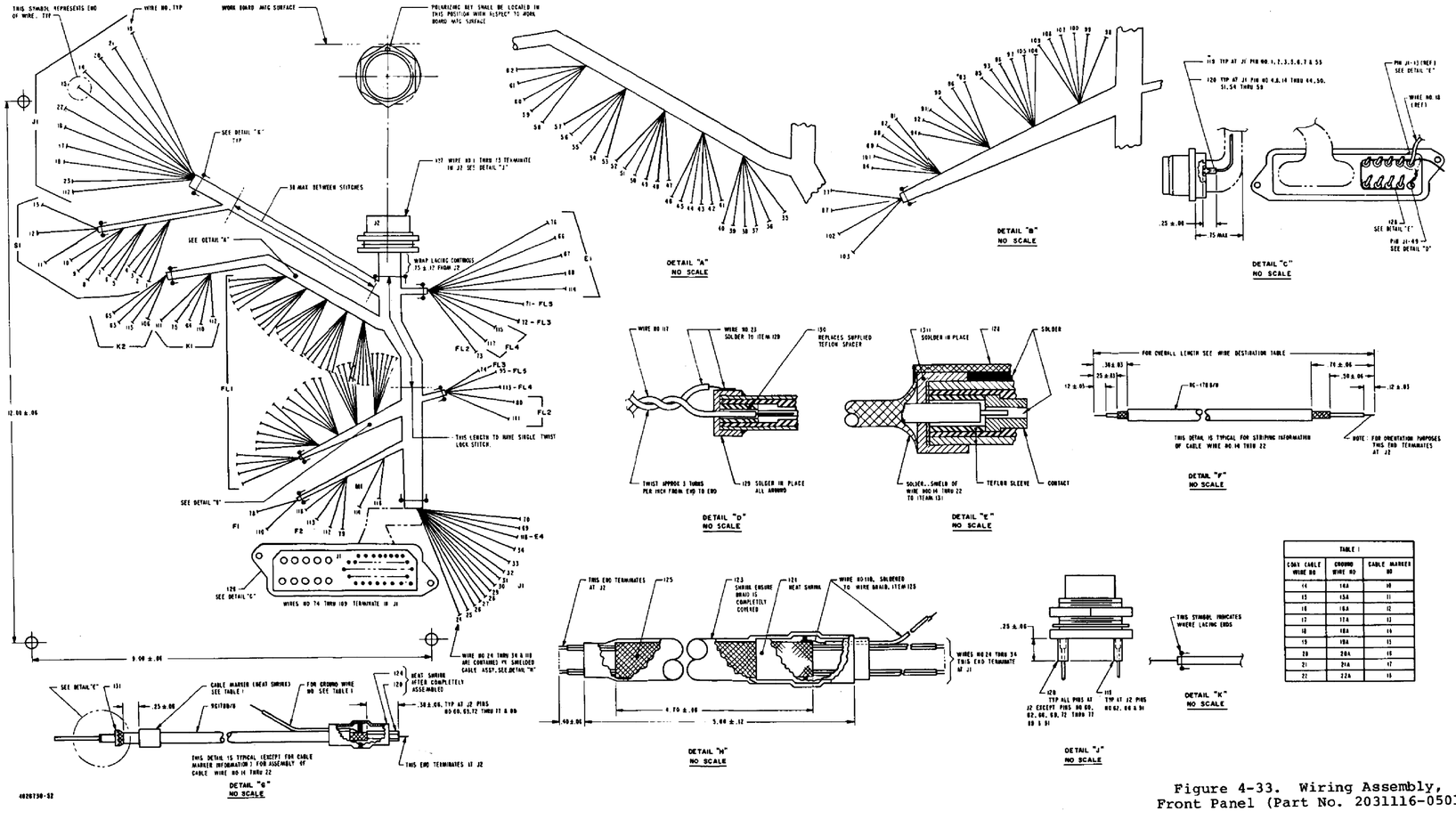
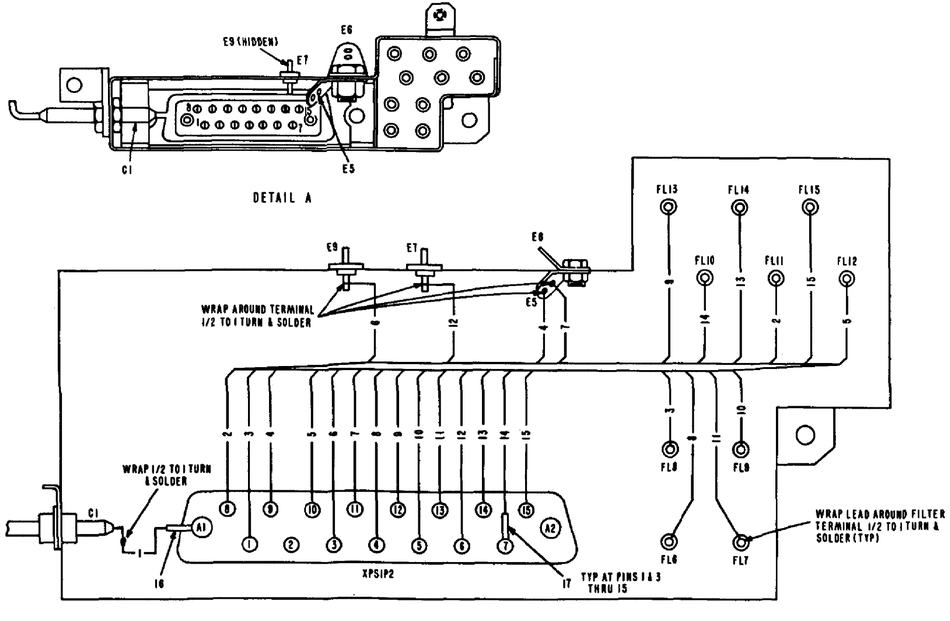


TABLE I		
COAX CABLE WIRE NO	GROUND WIRE NO	CABLE MARKER NO
14	14A	10
15	15A	11
16	16A	12
17	17A	13
18	18A	14
19	19A	15
20	20A	16
21	21A	17
22	22A	18

Figure 4-33. Wiring Assembly, Front Panel (Part No. 2031116-0501)



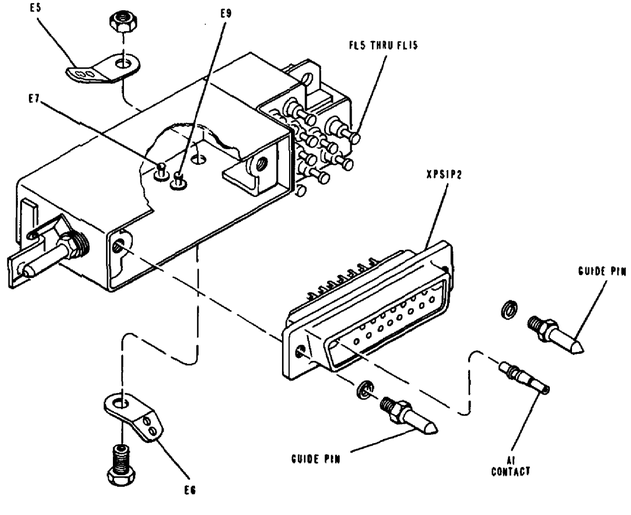


Figure 4-34. Connector and Filter Assembly (Part No. 4023580-0501)

Table 4-40. Connector and Filter Assembly (Part No. 4023580-0501)

1 WIRE NO.	2 *WIRE TYPE	3 WIRE COLOR	4 APPROX LENGTH REQD (Inches)	5 FROM	6 TO	7 **REMARKS
1	AWG 20	Red	2.0	XPS1P2-A1	C1	
2	AWG 24	Brn	3.5	XPS1P2-8	FL11	
3	AWG 24	Blu	3.0	XPS1P2-1	FL8	
4	AWG 24	Blk	2.0	XPS1P2-9	E5	
5	AWG 24	Wht-Yel	3.5	XPS1P2-10	FL12	
6	AWG 24	Wht-Orn	2.0	XPS1P2-3	E9	
7	AWG 24	Blk	2.0	XPS1P2-11	E5	
8	AWG 24	Orn	2.5	XPS1P2-4	FL6	
9	AWG 24	Wht-Blk	3.0	XPS1P2-12	FL13	
10	AWG 24	Red	2.5	XPS1P2-5	FL9	
11	AWG 24	Grn	2.5	XPS1P2-13	FL7	
12	AWG 24	Wh t	1.5	XPS1P2-6	E7	
13	AWG 24	Yel	3.0	XPS1P2-14	FL14	
14	AWG 24	Wht-Red	2.5	XPS1P2-7	FL10	
15	AWG 24	Blk	3.0	XPS1P2-15	FL15	
16	Insulation Sleeving #12	Natural	0.38 +0.06		A1	Hi-Temp Part No. TUX-14
17	Insulation Sleeving #14	Natural	0.38 +0.06 ea.		Pins 1 and 3 thru 15	Hi-Temp Part No. TUX-12

AWG SIZE	CONDUCTOR DIA NOMINAL	NO. OF STRANDS MINIMUM	MAX DC RESISTANCE OHMS/1000 FT AT 25°C	DIA OVER INSULATION MAXIMUM	ITEMS
24	0.024	19	26.8	0.048	2-15
20	0.038	19	10.5	0.072	1

*Wire Type Specifications MIL-W-16878, Insulation Teflon MIL-M-14077.

**See figure 4-34.

4-28. TOLERANCES AND LIMITS.

4-29. Table 4-41 lists the most adverse operating conditions under which the receiver-transmitter may be operated with some performance degradation.

Table 4-41. Tolerances and Limits

FUNCTION	DEGRADED PERFORMANCE LIMITS
Input Voltage Range	17 to 21 vdc
	103 to 107 and 122 to 127 vac
Antenna Mismatch	VSWR 1.497 to 1

4-30. ASSEMBLY OF RECEIVER-TRANSMITTER.

4-31. When assembling the receiver-transmitter, ensure that replaced wires are properly dressed to preclude damage to wires by kinking or pinching between components and chassis. (This will also ensure a proper fit.)

4-32. RF SECTION. Perform the following steps to assemble the rf section.

a. Connect cabling to filter assembly FL6 through FL15 (figure 4-17).

b. Replace screw (15, figure 4-17).

c. Solder leads to XPS1P2 (figure 4-17).

d. Replace guide pins (17 and 18, figure 4-17).

e. Solder leads to transformer assembly, T1 (figure 4-17).

f. Remount T1 with screws (16, figure 4-17).

g. Solder leads to sensitivity board, A8.

h. Replace A8 mounting screws (13 and 14, figure 4-17). Place the standoff between the ripple filter and the sensitivity board.

i. Solder leads to detector and video amplifier, AR3.

j. Connect cables to AR3.

k. Remount AR3 with screw (12, figure 4-17).

l. Solder leads to oscillator Z2.

m. Connect cables to oscillator Z2.

Connect cables to low-pass filter Z3.

o. Solder leads to power amplifier AR2.

p. Connect cables to AR2.

CAUTION

When installing AR2 and Z2 (step 4-33q) and AR1 and Z1 (step 4-33s), tighten the eight screws (4 through 11, figure 4-17) and three screws (1, 2, 3, figure 4-17) applying a torque of 4 ±1 inch-pounds. Excess tightening can cause damage to these components. (Screws 5, 7, 8, and 10, figure 4-17, have retaining brackets which hold wires clear of amplifier AR2 and oscillator Z2. Dress the

wires running parallel to AR2 and Z2 under the tuning screws. All tuning screws should be accessible without disassembling the unit.)

g. Apply a thin coat of heat-conducting compound [refer to paragraph 4-27.a.2. (d)] to AR2, Z2, and rf case. Remount AR2, Z2 (ensure these two components do not make physical contact), and Z3. Fasten with clamps and screws (4 through 11, figure 4-17) applying a torque of 4 ±1 inch-pounds.

r. Connect cable to preselector Z1 and amplifier AR1 and resolder leads to AR1 (figure 4-17).

s. Apply a thin coat of heat-conducting compound [refer to paragraph 4-27.a.2. (d)] to AR1, Z1, and rf case. Remount AR1 and Z1 with clamps and screws (1, 2, 3, figure 4-17) applying a torque of 4 ±1 inch-pounds.

t. Solder leads to modultator A7 and remount with screws (A7S1, S2, figure 4-17).

u. Replace rf shield with screws (S1, S2, and S3, figure 4-16).

4-33. DIGITAL AND POWER SUPPLY SECTION. Perform the following steps to assemble the digital and power supply section.

a. Replace power and control feedthrough connector (figure 4-21) .

b. Connect leads to filter FL1.

c Replace filter assembly and mounting screws (figure 4-21).

d. Solder leads and diodes to relay K1.

e. Replace relay K1 and mounting screws (figure 4-21).

f. Solder leads and diodes to relay K2.

g. Replace relay K2 and mounting screws FL2, FL3, FL4, FL5.

h. Solder leads to filter assemblies FL2, FL3, FL4, FL5.

i. Replace filter assembly and mounting screws (figure 4-21).

j. Insert carrying handle and replace nut caps (figure 4-21) .

k. Replace elapsed time indicator (7, figure 4-21).

1. Replace elapsed time indicator mounting screws (6 and 8, figure 4-20).

m. Solder all leads to elapsed time indicator.

Replace thumbwheel switch assembly (figure 4-21).

o. Replace thumbwheel switch assembly retaining nuts (figure 4-21).

P Solder leads to thumbwheel Switch assembly (figure 4-21).

g. Power and Control Connector J1 (figure 4-21).

1. Replace connector shell fastening in place with two self-locking nuts (figure 4-21).

2. Replace insert in connector shell ensuring fingers are in holding slot and fasten with three insert screws (figure 4-21).

Replace faceplates and tighten screws (figure 4-20).

s. Replace fuses.

t. Solder leads to card cage connectors and insert with card cage (figure 4-34).

u. Remount card cage connector with screws (5, figure 4-19). Refer to paragraph 4-22g.

v. Replace card cage and secure with slotted mounting screws (1, 2, 3, and 4, figure 4-19).

w. Connect power and control connector (figure 4-18) . Refer to NOTE in paragraph 4-21c.

x. Tighten screws (1, 2, 3, and 4, figure 4-19).

y. Replace circuitboards. Observe carefully the color-coded dots on top of each circuitboard and on the side of the card cage. Be sure the color-codes match before replacement of the circuitboards.

z. Power supply assembly.

1. Position gusset plate.

2. Replace two screws (19, 5, figure 4-22).

3. Position chassis assembly.

4. Replace two screws (4, hidden, figure 4-28).

5. Position reactor PS1L1.

6. Replace four screws (hidden) on gusset plate and replace reactor PS1L1.

7. Position semiconductor device PS1CR1, CR2.

8. Replace one screw (11, figure 4-28).

9. Position power transformer PS1T1.

10. Replace four screws (14, 15, 16, and 18, figure 4-22).

11. Solder leads to PS1T1.

12. Solder leads to switch regulator assembly.

13. Position switch regulator drive assembly on top of reactor PS1L2.

14. Replace four screws (3, 6, 7, and 8, figure 4-28).

15. Solder leads to filter capacitor assembly.

16. Replace four screws (1, 2, 3, and 4, figure 4-27).

17. Position interconnection board and subassembly.

18. Replace four screws (1, 5, and two not shown, figure 4-26) .

19. Position semiconductor device PS1CR34, CR35.

20. Replace one screw on semiconductor device.

21. Solder leads to PS1CR34, CR35.

22. Position inverter transformer.

23. Replace four screws (15, 16, 17, and 18, figure 4-26).

24. Solder leads to inverter transformer.

25. Position inverter drive transistor subassembly.

26. Replace two screws (8 and 9, figure 4-26).

27. Solder leads to inverter driver transistor subassembly.

28. Position inverter drive assembly.

29. Replace four screws (4, 6, 7, and 10, figure 4-26).

30. Solder leads to inverter drive assembly.

31. Position output filter assembly on top of output capacitor subassembly.

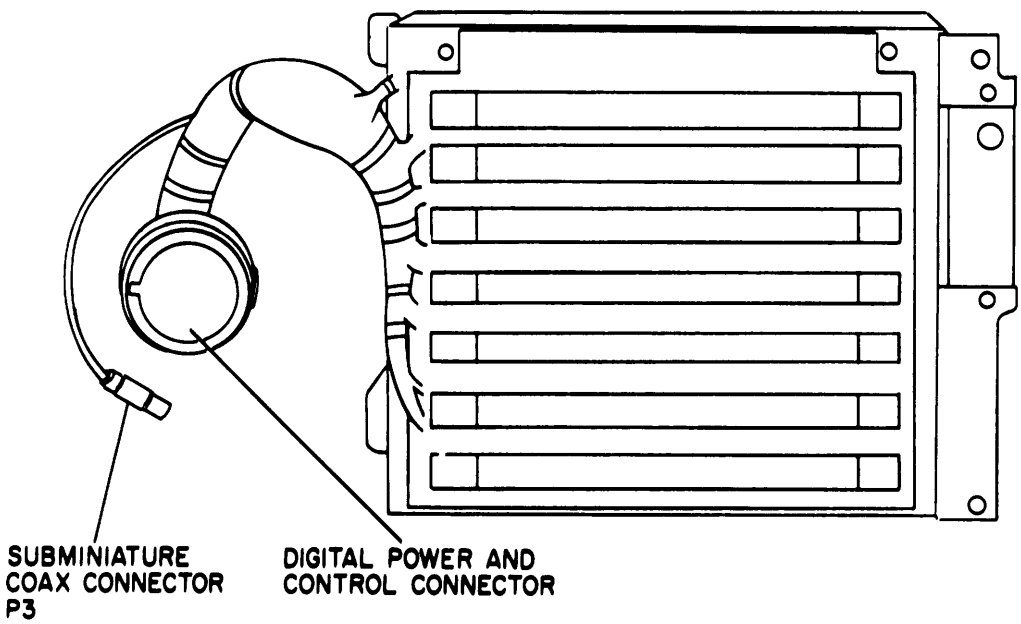


Figure 4-35. Circuitboard Cage Assembly, Rear View

32. Replace four screws (11, 12, 13, and 14, figure 4-26).

33. Position output rectifier assembly on top of output capacitor subassembly.

34. Replace four screws (1, 2, 3, and 4, figure 4-25).

35. Solder leads to output rectifier assembly.

36. Position output assembly,

37. Replace four screws (1, 2, figure 4-24, and 2, 4 figure 4-22).

38. Position overcurrent assembly on top of switching regulator assembly.

39. Replace four screws (1, 5, 4, and 6, figure 4-23).

40. Solder leads to overcurrent and switching assembly.

41. Solder leads to 1 KV assembly.

42. Position 1 KV assembly.

43. Replace two screws (2 and 3, figure 4-23).

44. Position power supply covex and clmap.

45. Start 12 screws (20, 21, 22, 1, 3, 6, 7, 8, 9, 10, 11, and 13, figure 4-22) and tighten.

aa. Replace power supply PS1.

1. Apply a thin coat of heat-conducting compound (part number 2077846-0001) to contacting surfaces of power supply and digital and power supply section [refer to paragraph 4-27a.2.(d)].

2. Tighten two screws (1, figure 4-18).

4-34. CONNECTION OF ASSEMBLIES. Perform the following steps to connect the assemblies.

a. Inspect silicon O-ring seal for serviceability. If damaged or deteriorated, discard and obtain serviceable item from supply.

b. Replace serviceable silicon O-ring seal around flange of rf section.

c. Apply a thin coat of heat-conducting compound (specification MIL-S-8660B) on contacting surfaces of both the rf and digital and power supply sections [refer to paragraph 4-27a.2.(c)].

d. Place digital and power supply section, top side down, on work bench.

e. Connect subminiature coax P3 to video output jack AR3J1.

f. Place rf section on digital and power supply section.

g. Replace and secure flange coupler.

h. Pressurize assambled receiver-transmitter to 10 lb/in2 gage using MK-20A/UP pump, dehydrator or equivalent.

i. Remove pressurization pump and connect the locally fabricated gauge shown in figure 4-36.

1. Release pressure to 5 lb/in^2 gage.

2. After thirty minutes, observe the test gauge. If the pressure drop is less than 1 lb/in^2 gage the unit is acceptable, Repressurize unit and return to stock.

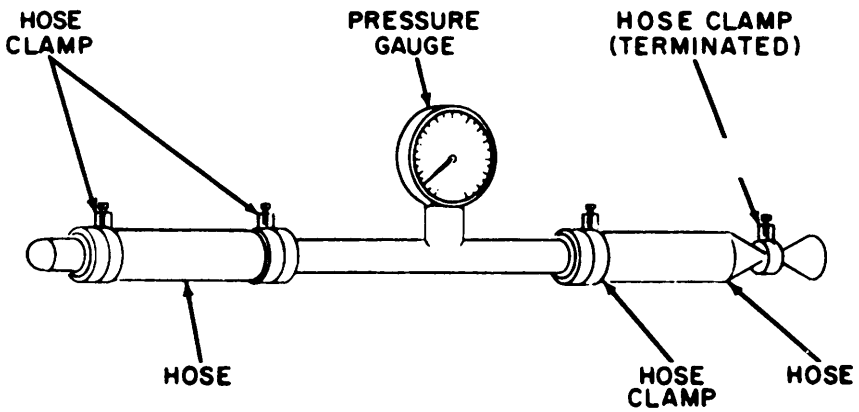


Figure 4-36. Test Gauge Assembly

4-35. ALIGNMENT AND ADJUSTMENT PROCEDURES USING RADAR TEST SET AN/UPM-98A OR AN/UPM-137.

4-36. Alignment and adjustment procedures are performed to obtain optimum results from the receiver-transmitter. These procedures are followed, when necessary, in conjunction with the performance tests and measurements (refer to paragraph 4-9) and during repair or replacement of individual subassemblies. Test equipment, used for alignment procedures, is listed in table 4-1. Test points, adjustments, and waveform figure references are listed in table 4-24 and their locations in figure 4-13.

a. Alignment Using Radar Test Set AN/UPM-98A. To perform a complete alignment of the receiver-transmitter, follow the instructions in table 4-43. The preliminary connections and procedures for step 1 of table 4-43 are described below and shown in figure 4-37. The connections and procedures for steps 2 through 14 are described in paragraph 4-15a. and shown in figure 4-12.

1. Receiver-Transmitter.

(a) Repressurize and remove flange coupler.

(b) Separate digital and power supply section from rf section removing O-ring and rf shield (refer to paragraphs 4-19 and 4-20a. and b.).

(c) Connect both sections together, side by side, using a typical jig which could consist of two flange couplers welded together (figures 4-12 and 4-37).

(d) Connect power supply jumper cable (figure 4-11) between XPS1P2 and XPS1J2.

(e) Connect rf connector and cable assembly (part number 4023657, figure 4-11) between AR3J1 and P3.

(f) Connect a jumper cable between E9 and PS1TP4 (+6 vdc).

(g) Connect POWER, CONTROL & VIDEO J1 to TRANSPONDER power and control on AN/APM-239.

(h) Connect a 10-db pad (Weinschel Model 10-10, or equivalent) to ANT. J5.

(i) Connect a cable between 10-db pad and RF OUT on SG-677/U.

(j.) Connect Probe from A input VERTICAL AMPLIFIER AN/USM-140B to AR3TP1.

2. Test Set, Transponder AN/APM-239.

(a) Connect PWR INPUT to 115-vac, 400-Hertz voltage source.

(b) Ensure TRANSPONDER power and control is connected to POWER CONTROL & VIDEO J1 on receiver-transmitter.

(c) Set all controls and switches as directed in table 4-2.

WARNING

Ensure that C-6280(P)/APX MASTER switch is set in OFF or STBY while performing procedures of step 1, table 4-43.

3. Sweep Frequency Generator (SG/667/U or AN/USM-203).

(a) Connect power cord to 115-vac, 60-Hertz voltage source.

(b) Connect SCOPE HORIZ to HORIZ INPUT on AN/USM-140B.

(c) Ensure that RF OUT is connected to ANT. J5 on receiver-transmitter through a 10-db pad.

(d) Connect SCOPE VERT to B input VERTICAL AMPLIFIER AN/USM-140B.

(e) Set POWER to ON.

(f) Set all controls and switches as shown in table 4-42.

4. Oscilloscope, AN/USM-140B.

(a) Connect power cord to 115-vac, 60-Hertz voltage source.

(b) Ensure that HORIZ INPUT is connected to SCOPE HORIZ on SG-677/U.

(c) Ensure that B input VERTICAL AMPLIFIER is connected to SCOPE VERT on SG-677/U.

Table 4-42. Sweep Frequency Generator. Preliminary Control Settings

CONTROL	POSITION
SWEEP WIDTH range	WIDE
BAND SELECTOR	UHF
Meter	Zero set
RF OUTPUT	Adjust for zero db on meter
ATTENUATOR DB	50
SWEEP WIDTH vernier	Center
FREQUENCY	1000 MHz
PREAMPLIFIER GAIN	Rotate 3/4 CW
AC-DC switch	AC

(d) Ensure that A input VERTICAL AMPLIFIER is connected through probe to AR3TP1.

(e) Set A and B VERTICAL AMPLIFIER to CHOPPED mode.

(f) Set POWER to ON and adjust controls and switches for a display presentation.

5. Signal Generator, AN/URM-64A.

(a) Connect power cord to 115-vat, 60-Hertz voltage source.

(b) Connect RF OUTPUT to LP IN on AN/UPM-98A.

(c) Set POWER to ON.

(d) Set SYNC SEL to ZERO SET and adjust ZERO SET to indicate ZERO SET on DBM METER.

(e) Set SYNC SEL to CW and adjust POWER SET to indicate +3 DB on DBM METER.

(f) Set SYNC SEL to RATE X10, PULSE RATE to 400, PULSE WIDTH to 10, OUTPUT ATTENUATOR to minimum attenuation.

6. Radar Test Set, AN/UPM-98A.

(a) Connect power cord to 115-vac 60-Hertz voltage source.

(b) Ensure that LP IN is connected to RF OUTPUT on AN/URM-64A.

(c) Set both POWER switches to ON.

(d) Set METER SELECT (CAL-CONTROL) to WM and WAVEMETER INPUT to DEMOD.

7. Preliminary procedures. The AN/URM-64A and SG-677/U are used in the preliminary procedures to locate the 103O-MHZ frequency.

(a) Set WAVEMETER FREQUENCY on AN/UPM-98A to 1030 MHz using calibration charts.

(b) Adjust SIGNAL FREQUENCY on AN/URM-64A to obtain a meter dip on AN/UPM-98A meter, adjusting WM SENS (CAL-CONTROL) as required. This procedure calibrates the AN/URM-64A or 1030-MHZ marker output.

NOTE

If meter dip cannot be noted, perform steps (1) through (7) below. If meter dip is noted proceed to c below.

(1) Remove cable connector from LP IN (AN/UPM-98A) and connect to EXTERNAL MARKER (SG-677/U).

(2) Adjust SIGNAL FREQUENCY dial (AN/URM-64A) for a reading of 1000. Set SYNC SEL to CW and adjust POWER control to indicate 0 DB on DBM meter.

(3) Pull out MASTER GAIN control (SG-677/U) and turn it fully CW. Adjust FREQUENCY dial control (SG-677/U) around 1000 MHz until 1000 MHz marker appears. Adjust PHASING and FREQUENCY controls simultaneously until markers coincide and marker is positioned on center vertical line on the AN/USM-140B scope. Disconnect cable from EXTERNAL MARKER input.

(4) On SG-677/U, pull out 100 MHz marker and turn fully CW.

(5) Vary FREQUENCY dial control around 1000 MHZ to position the 1000-MHZ marker on the vertical center line. Adjust PHASING and FREQUENCY dial controls simultaneously until markers on AN/USM-140B coincide.

(6) Push in 100-MHZ marker and pull out 10-MHZ marker. The 10-MHZ marker positioned on the vertical center line represents the 1000 MHz on the FREQUENCY dial. Increase FREQUENCY dial reading until the third 10-MHZ marker moving toward center from right, is positioned on the center vertical line. This is the 1030-MHZ frequency marker.

NOTE

To adjust the AN/URM-64A for 1030 MHz to be used in step 3 of table 4-43, proceed as follows:

(a) Push in 1 MHz and 10 MHz marker controls.
(b) Reconnect cable to EXTERNAL MARKER input.
(c) Pull out EXTERNAL MARKER control and adjust fully CW.
(d) Vary SIGNAL FREQUENCY control (AN/URM-64A) until 1030 MHz marker appears on center of scope display. This establishes 1030 MHz output of the AN/URM-64A.

(7) Adjust SWEEP WIDTH vernier and PHASING control simultaneously until the 1020- and 1040-MHz markers are positioned at opposite ends of the sweep (sweep 20 MHZ wide). Readjust FINE tuning to place the 1030-MHZ marker at the center of the sweep. Pull out l-MHz marker and rotate CW until l-MHz markers appear on the AN/USM-140B. Pull out BLANKING control. Proceed to (f) below.

(c) Remove cable connection from LP IN (AN/UPM-98A) and connect to EXT MARKER (SG-677/U).

(d) Set SYNC SEL (AN/URM-64A) to CW.

(e) On SG-677/U, pull out MASTER GAIN control and rotate CW to midscale. Adjust PHASING control and FREQUENCY dial simultaneously until markers appearing on AN/USM-140B coincide. Pull out

10-MC markers and rotate CW until 10-mc markers appear on AN/USM-140B (ensure that 1 MC and 100 MC markers are OFF). Adjust SWEEP WIDTH vernier and PHASING control simultaneously until the 1020- and 1040-mc markers are positioned at opposite ends of sweep (sweep 20-mc wide). Readjust FINE TUNING to place the 1030-mc marker at center of sweep. Switch 10 MC marker OFF, pull out 1 MC marker and rotate CW until 1-mc markers appear on AN/USM-140B. Pull out BLANKING control.

(f) Adjust AN/USM-140B to align B trace with horizontal center line and adjust SWEEP FREQUENCY (SG-677/U) to place 1030-MHZ marker found in step (b) or (e) on vertical center line of AN/USM-140B.

(g) Count 3.5 l-MHz markers each side of center frequency (1030 MHz) to locate upper and lower 6-dB frequencies.

(h) Set A input VERTICAL AMPLIFIER (AN/USM-140B) SENSITIVITY to .1V/CM, C-6280(P)/APX(AN/APM-239) MASTER to STBY. Adjust RF VARIABLE ATTENUATOR (SG-677/U) as required to view full scale bandpass waveform on A trace (AN/USM-140B).

b. Alignment Using Radar Test Set AN/UPM-137. This alignment and adjustment procedures that are provided in table 4-44, page 4-289 use similar test setup procedures that are used for performance tests. The preliminary connections and procedures for table 4-44, page 4-209 are described helm and shown in figure 4-38, page 4-287.

1. Receiver-Transmitter.

(a) prepare the receiver-transmitter for alignment by performing procedures of paragraph 4-36a.1. (a) through (g), page 4-265.

(b) Connect CHAN B VIDEO INPUT of AN/UPM-137 Oscilloscope to AR3TP1 using a 1:1 probe.

2. Test Set, Transponder AN/APM-239

(a) Connect PWR INPUT to 115 vat, 400-cycle voltage source.

(b) Ensure TRANSPONDER power and control is connected to POWER CONTROL and video J1 on receiver-transmitter.

(c) Set all controls and switches as directed in table 4-2, page 4-16.

WARNING

Ensure that C-6280(P)/APX MASTER switch is set in OFF or STBY unless directed otherwise.

3. Test Set, Radar AN/UPM-137.

(a) Connect power cable to 115 vat, 60 Hz source.

(b) Connect all test equipment as shown in figure 4-38, page 4-2-7.

(c) Set all controls and switches to positions identified in table 4-15, page 4-48 with the following exceptions: Set OUTPUT ATTEN 0-100 dBm dial to -30 dBm, the CHAN A 75 Ω switch to OUT, the CHAN A VOLT/DIV to 0.5, the TIME/DIV switch to 50 USEC, the SWEEP DELAY RANGE MULT switch on the oscilloscope to X400, the XMTR

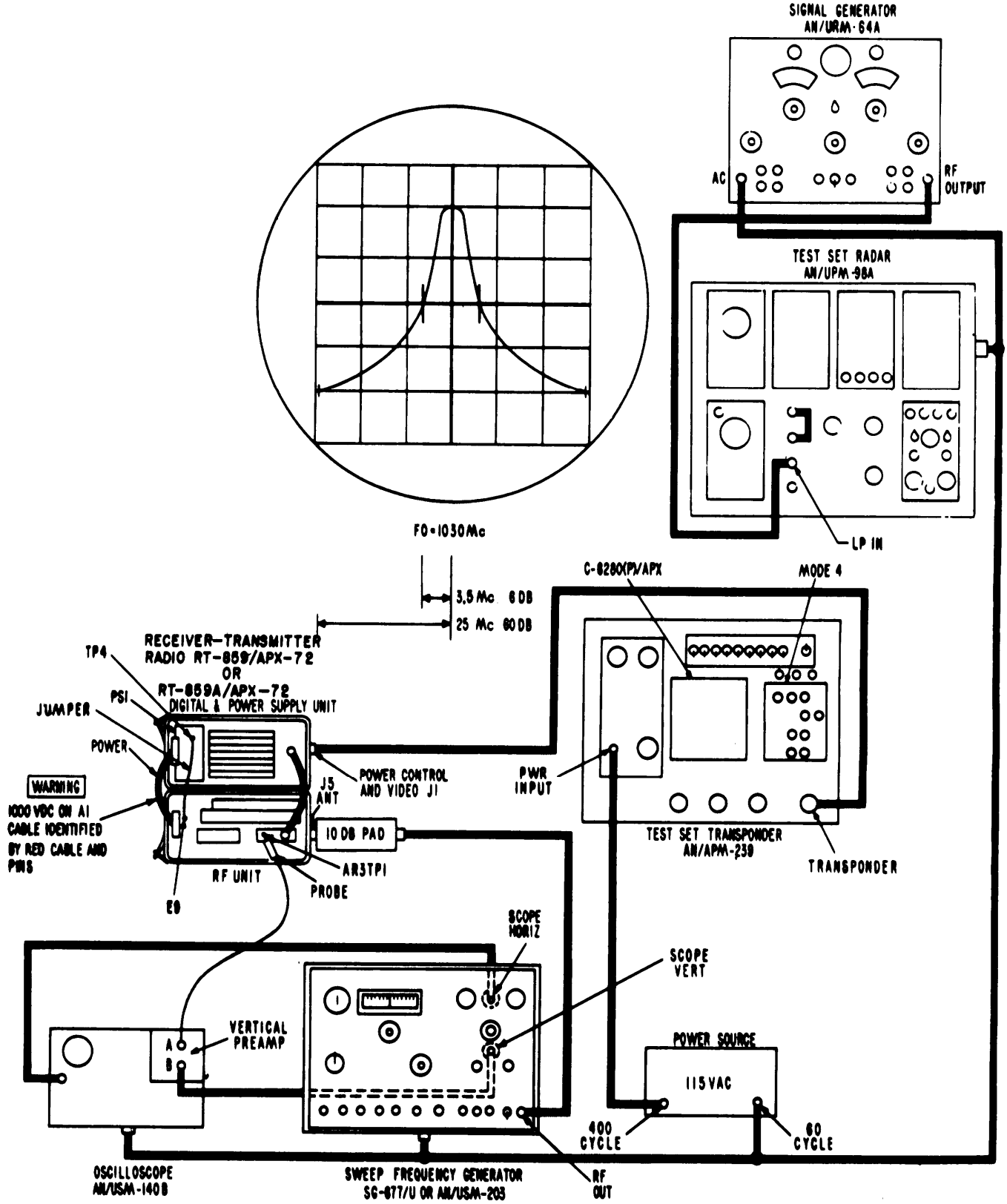


Figure 4-37. Receiver Alignment Test Setup, Using AN/UPM-98A Test Set

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A

STEP	PROCEDURE	REMARKS
1. Receiver alignment	a. Connect equipment as rescribed in paragraph 4-36a. and shown in figure 4-37.	
	WARNING Terminals adjacent to receiver tuning adjustments are at voltage levels hazardous to life.	
	b. Loosen locknuts on preselector adjustment Z1C1 and rf amplifier AR1C3.	
	c. Adjust Z1C1 for peak response at 1030 MHz. Normally Z1C2, Z1C3, AR1C1, and AR1C2 do not require adjustment. Should adjustment of Z1C1 not provide peak response at 1030 MHz, loosen locknuts and adjust Z1C2, Z1C3, AR1C1, AR1C2, and AR1C3 in given order for peak response.	Observe waveform for indication of 1030 MHz near peak of curve.
	d. Adjust Z1C1 and AR1C3 alternately for the best obtainable waveform about 1030 MHz. Obtain best compromise between peak response and waveform symmetry.	Monitor waveform on AN/USM-140B.
	e. Adjust (SG-677/U) VARIABLE ATTENUATOR for 0.5-volt peak deflection of waveform. Adjust (AN/USM 140B) "A" trace VERT GAIN for full scale deflection.	
	f. Repeat step l.c. to obtain +3.5 MHz at 6-dB points (half scale) if necessary.	Observe waveform for ±3.5-MHz bandwidth at 6-dB markers.

Table 4-43. Complete Alignment and Adjustment procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
1. Receiver alignment (Cent)	g. When bandwidth of ±3.5 MHZ has been achieved, tighten both adjustment locknuts using care to prevent change in tuning adjustments.	
	h. Disconnect jumper wire between TP4 and E9.	Bandwidth waveform should disappear.
	i. Measure frequency and bandwidth for minimum performance standards using procedures of paragraph 4-11.d and table 4-7.	Performance standard center frequency 1030 ±1.5 MHz and 6-dB bandwidth 7 MHz, minimum.
	NOTE Connect equipment as described inparagraph 4-15a. and shown in figure 4-12 for steps 2. through 14., modifying as directed.	
2. Voltage level adjustments. (For AR3 part Nos. 4023409-0501 and 4023409-0502, only.)	a. Replace ME-26/U Multimeter with differential voltmeter MIL-V-9989 for this step. Set C-6280(P)/APX to STBY.	
	b. Connect positive lead of differential voltmeter to ground and negative lead to AR3TP3. Adjust AR3R76 for voltage reading of -4.5 vdc. Disconnect leads.	Read -4.5 +0.025 vdc.
	c. Connect negative lead of differential voltmeter to ground and positive lead to AR3TP2. Adjust AR3R73 for voltage reading of 4.5 vdc. Disconnect leads.	Read +4.5 ±0.025 vdc.
3. Normal sensitivity adjustments	a. Set AN/UPM-98A using procedures of paragraph 4-11.a.2 (a) through (g). Set MODE SELECT (INTERROGATION CODER) to C and adjust PULSEWIDTH to 0.8 µs. Set ATTENUATION	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
3. Normal sensitivity adjustments (Cont)	to obtain a signal level of -60 dBV at J5 of the receiver-transmitter. b. Connect electronic counter as described in paragraph 4-11.a.5. Set SENSITIVITY to FREQ C, TRIGGER VOLTS C dial to 10 and adjust outer dial to trigger counter. Set C-6280(P)/APX (AN/APM-239) MASTER to NORM and M-C to ON. Adjust PRF control (XTAL MARK & SYNC) on AN/UPM-98A for a reading of 500 on counter. Increase ATTENUATION 30.5 dB to obtain a signal level of -90.5 dBV at J5 of the receiver-transmitter. c. Connect probe of AN/USM-140B to A1TP6 and adjust A8R6 for maximum amplitude of the pulse at A1TP6. Measure from center of base line noise to center of peak pulse noise. If a maximum amplitude is less than 0.6 volt minimum, receiver-transmitter is defective. If this pulse meets amplitude requirements, measure voltage difference between peak of base line noise and base of peak pulse noise. A measurement of 0.2 volt or more is acceptable, a measurement less than 0.2 volt indicates a defective receiver-transmitter. d. Ensure that AN/URM-64A is set for 1030 MHz as described in paragraph 4-36a.7. Set OUTPUT ATTENUATOR (AN/URM-64A) for a dial reading of -55 dBm. Set SYNC SEL switch to CW. Disconnect	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
3. Normal sensitivity adjustments (Cont)	cable from HP IN (AN/UPM-98A) and connect it to RF OUTPUT (AN/URM-64A).	
	e. Set C-6280( )/APX (AN/APM-239) MASTER switch to STBY and M-2 switch to ON.	
	f. On AN/USM-140B, set TIME/DIV to .2 MSEC. Connect oscilloscope probe to A1TP2 and adjust A1R22 slowly CW until circuit begins to trigger on noise, then adjust A1R22 1/4 turn CCW.	
	g. Disconnect cable from RF OUTPUT (AN/URM-64A) and connect it to HP IN (AN/UPM-98A). Set ATTENUATION (AN/UPM-98A) for a -90 dBV at ANT. J5 on receiver-transmitter.	
	h. Ensure that electronic counter is connected to SUPPRESSION OUT "(AN/APM-229)" Adjust A1R25 for a count of 450 on the electronic counter.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
4. Ditch length adjustments (RT-859/APX-72 only.)	a. Ensure C-6280(P)/APX (AN/APM-239) MASTER switch is in STBY. Remove cables between ANT. J5 (RT-859/APX-72) and HP IN (AN/UPM-98A), and between SG IN and SG OUT (AN/UPM-98A). Connect a 10-dB pad (minimum power rating 5 Watts, frequency 1090 MHz) to ANT. J5 and a cable between 10-dB pad and SG OUT.	
	b. Set ATTENUATION to obtain -40 dBV at ANT. J5 on RT-859/APX-72. Connect AN/USM-140B probe to A1TP4.	
	c. Adjust A1R10 to obtain trapezoidal line equal to 13.5 µs. Disconnect probe from A1TP4.	Waveform figure 6-3.
4A. Wide Pulse detector adjustments (RT-859A/APX-72 only.)	a. Ensure C-6280(P)/APX (AN/APM-239) MASTER switch is in STBY and M-C switch is set to ON. Disconnect cable from HP IN (AN/UPM-98A) and connect it to SG OUT. Increase ATTENUATION for a count of 450 on the electronic counter. This establishes the MTL reference for SG OUT. Decrease ATTENUATION 3 dB.	
	b. Adjust PULSE WIDTH (INTERROGATION CODER) AN/UPM-98A for pulse width of 1.4 µs as observed on the AN/USM-140B.	
	c. Adjust A1R10 until counter indicates an average of 10 counts per second NOTE. Adjust A1R10 CW to reduce count.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
4A. Wide Pulse detector adjustments (RT-859A/ APX-72 only.) (Cont)	d. Rotate ATTENUATION AN/UPM-98A from 3 dB to 50 dB above MTL. If electronic counter indicates an average higher than 10 counts, readjust A1R10.	
5. Side lobe suppression adjustments	a. Ensure C-6280(P)/APX (AN/APM-239) MASTER switch is in STBY. Make connections described in step 4a., above. Connect AN/USM-140B probe to A1TP6.	
	b. Set AN/UPM-98A MODE SELECT to c, PULSE WIDTH to 0.8 µs, ISLS SELECT to 2 VS. Set ATTENUATION (AN/UPM-98A) for a signal level at ANT. J5 of 6 dB above MTL and adjust signal level of ISLS to equal that of the first interrogation pulse as displayed on the AN/USM-140B, note this reference level. Decrease ATTENUATION by 6 dB. Readjust ISLS control for a pulse amplitude equal to the reference level noted above. This adjusts the ISLS pulse level to 6 dB below interrogation pulse level. Connect AN/USM-140B probe to A1TP2.	
	c. Adjust ATTENUATION (AN/UPM-98A) to obtain -77 dBV at ANT. J5. Adjust A1R6 until ISLS pulse appears intermittently at A1TP2, then readjust until ISLS pulse just disappears. Sweep ATTENUATION from MTL plus 3 dB to plus 50 dB. If ISLS pulse reappears intermittently from 6 to 50 dB.	

Table 4-43. Complete Alignment and Adjustmant Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
5. Side lobe suppression adjustment (Cont)	above MTL, ropeat adjustments until ISLS does not appear in this range. Disconnect probe from A1TP2.	
	d. Set ISLS SELECT (INTERROGATION CODER) to OUT, MODE SELECT to 2. Adjust ATTENUATION to obtain MTL at ANT. J5. Set C-6280(P)/APX M-2 (WAPM-239) to ON, M-C to OUT, MASTER to NORM. Adjust A8R6 until counter indicates an average of 450 counts.	90% replies.
	e. Set C-6280(P)/APX MASTER to STBY. Repeat stops 4a. and 5.b. and c. and adjust A1R6 only if required.	
	f. Repeat stop 3 above.	
6. Low sensitivity adjustments	a. Set ISLS SELECT (INTERROGATION CODER) to OUT, MODE SELECT to 2, and adjust ATTENUATION to obtain -78 dBV at ANT. J5 (receiver transmitter). Set C-6280(P)/APX M-2 (AN/APM-239) to ON, MASTER to LOW.	
	b. Adjust A8R5 until electronic counter, indicates an averago of 450. Set C-6280(P)/APX MASTER to STBY.	90% replies.
7. Reply rate limiter adjustments	a. Rmove cable and 10-dB pad connected between SG OUT on AN/UPM-98A and ANT. J5 of receiver-transmitter. Connect cable from ANT. J5 to HP IN. Connect jumper cable from SG IN to SG OUT.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
7. Reply rate 1imiter adjustments (Cont)	b. On AN/UPM-98A set TRIGGER TO INT, METER SELECT (Cal-CONTROL) to 5000 PRF, and adjust PRF (XTAL MARK & SYNC) to indicate 3000 on meter. Set ATTENUATION to obtain -84 dBV at ANT. J5. Adjust A2R89 for an electronic counter indication of approximately 2000 counts.	
8. Transmitter pulse width adjustments	a. Adjust AN/UPM-98A PRF (XTAL MARK & SYNC) to indicate 1800 PRF on meter. Set VIDEO OUT (CAL-CONTROL) to SHAPE. Set C-6280 (P)/APX (AN/APM-239) MASTER to NORM.	
	b. Adjust A7R4 for a reply pulse width *of* 0.45 µs at the 50% amplitude points.	
9. Duty cycle control adjustments	a. Adjust AN/UPM-98A PRF (XTAL MARK & SYNC) to indicate 1700 PRF on meter. Set MODE 2 code (receiver-transmitter) to 7777.	
	b. Adjust A2R51 for an average counter Indication of 1625.	
	c. Repeat procedures of step 7a., adjusting A2R89 for an average counter indication of 1200.	
10. Reply/pulse spacing adjustments (RT-859/APX-72 only)	a. Set MODE 2 code (receiver-transmitter) to 0000. Adjust PRF for count of 500 +3 on counter. Perform procedures of table 4-12, steps 1a. through 1.d.	

Table 4-43. Complete alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
10. Reply pulse spacing adjustments (RT-859/APX-72 only) (Cont)	b. Adjust A4C1 so that F_2 leading edge falls on 15th marker ±0.05 µs.	Frame spacing 20.3 ±0.05 µs.
	c. Set MODE 2 code to 0007. F2 should remain within ±0.05 µs, if not, readjust A4C1 and repeat steps b. and c. until tolerance is met.	
	d. Disconnect and remove cable between VIDEO on DISPLAY chassis and VIDEO OUT on CAL-CONTROL chassis of AN/UPM-98A.	
11. Transmitter frequency and power adjustments	a. Set C-6280(P)/APX MASTER TO STBY. Disconnect cable at ANT. J5, insert 10-dB pad and reconnect cable. Set SYNC SELECT (XTAL MARK & SYNC) to INT, TRIGGER (CAL-CONTROL) to INT, and adjust PRF (XTAL MARK & SYNC) to indicate 500 PRF on meter. Set C-6280(P)/APX MASTER to NORM. Set MODE 2 code (receiver-transmitter) to 7777. Decrease ATTENUATION until reply pulses appear on AN/USM-140B.	
	b. Set AN/UPM-98A WAVEMETER FREQUENCY to 1090 MHz using charts supplied with test equipment. Set METER SELECT (CAL-CONTROL) to WM, WAVEMETER INPUT to DEMOD. Adjust Z2C1 (receiver-transmitter) for a maximum meter needle dip varying WM SENS as required.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN\UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
11. Transmitter frequency and power adjustment (Cent)	c. Set VIDEO OUT (CAL-CONTROL) to POWER and adjust AR2C1 for maximum pulse amplitude display on AN/USM-140B.	
	d. Readjust Z2C1, if required, to set transmitter on exact frequency. Detune WAVE-METER FREQUENCY. Measure peak amplitude of replies (AN/USM-140B) using conversion charts (HP IN) supplied with AN/UPM-98A, cable loss factor, and 10-db pad. NOTE If measured power in step 11.d. is less than 35 watts on conversion, proceed as follows: set MASTER on C-6280(P)/APX to STBY, disconnect cable from HP IN and reconnect to LP IN, remeasure peak amplitude.	
12. Mode 4 gate adjustments (RT-859A/APX-72, Part No. 4028683-0502 only)	a. Set up receiver-transmitter as described in paragraph 4-36.a.l. (a) through (e) and (g). Connect teat set-up as described in paragraph 4-11.j. and shown in figure 4-3.	
	b. Perform procedure of step 1., table 4-14.	
	c. Connect AN/USM-140B probe to A3TP6.	
	d. Adjust A3R215 to obtain a 92-us pulse.	
	e. Connect AN\USM-140B probe to A3TP8.	
	f. Adjust A3R224 until this pulse is positioned 300 us after the decode pulse of A3TP7.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
13. Mode 4 reply limiter adjustments	a. Set AN/UPM-98A (CAL-CONTROL) VIDEO OUT to SHAPE, METER SELECT to 5000 PRF, TRIGGER to INT. Adjustment PRF (XTAL MARK & SYNC) to indicate 2500 PRF on meter.	
	b. Adjust A3R29 or A3R1 on mode 4 boards with P/N 116104-1, until an average rate of 2000 is indicated on electronic counter.	
14. Mode 4 audio level adjustments	a. On AN/UPM-98A (CAL-CONTROL) set METER SELECT to 500 PRF, TRIGGER to INT. Adjust PRF (XTAL MARK & SYNC) to obtain an indication of 500 PRF on meter. On AN/APM-239, disconnect cable connection from MODE 4 TRIG, add a coax tee to cable, and connect to AUDIO. Connect a 150-Ohm load on open end of coax tee. Set C-6280(P)/APX AUDIO-OUT-LIGHT to AUDIO.	
	b. Adjust A3R89 or A3R2 on mode 4 boards with P/N 116104-1, for a 3-volt peak-to-peak audio signal measured on AN/USM-140B.	
15. Power supply, voltage and overcurrent adjustments	s. Ensure C-6280(P)/APX (AN/APM-239) MASTER is OFF. Disconnect cable from PS1P2 and XPS1P2 in setup shown in figure 4-12.	
	b. Loosen two slotted lift-out screws (1, figure 4-18) and remove power supply (PSI). Remove 12 screws (1, 3, 6 through 11, 13, 20, 21, and 22, figure 4-22) and remove cover and clamp.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
15. Power supply, voltage and overcurrent adjustments (Cont)	NOTE If tester is not available, proceed to step m. and use load bank described in Section III. c. Connect Tester-Dummy Load TS-3243/APM to PS1P1 and PS1P2 by means of connectors P1 and P2, respectively. Connect differential voltmeter, MIL-V-9989 between TP1 and TP2 of the tester. Adjust differential voltmeter RANGE control to 500-Volt position. d. Place the power supply in position so that R63 and R64 are available for adjustment, (see figure 4-23). Adjust resistor R64 fully counterclockwise (at least 20 turns). WARNING Lethal voltages are present when power is applied to the test setup using Tester-Dummy Load TS-3243/APM. These dangerous voltages are present on red Al wire, on terminal E5 of the tester, and on terminal A1 in the open power supply. e. Place RESERVE LOAD switch S1 at OFF position. f. Place POWER switch S2 at ON position.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
15. Power supply, voltage and overcurrent adjustments (Cont)	g. Adjust resistor R63 (see figure 4-23) for an indication of 310 +16, -6 vdc on the differential voltmeter.	310 +16, -6 vdc
	h. Measure power supply voltages as directed in table 4-25, steps 2 through 9. If the voltages do not meet the limits specified in table 4-25 and step g. above, adjust R63 until all voltages are within limits specified, <u>including differential</u> voltmeter reading.	
	i. Place RESERVE LOAD switch S1 at ON.	
	j. Set differential voltmeter at VTVM position. Adjust resistor R64 clockwise until the output voltage reading on the differential voltmeter drops to zero indicating that the overcurrent circuit is just beginning to operate. Proper operation of the overcurrent circuit is indicated by periodic attempts to rise shown by any of the output voltages. This should occur at a 1- to 5-second interval.	
	k. Adjust resistor R64 counterclockwise until the overcurrent circuit just drops out of operation as indicated by a reading of 310 +16, -6 vdc on the differential voltmeter. Set R64 approximately one turn further counterclockwise from this point.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN\UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
15. Power supply, voltage and overcurrent adjustments (Cont)	l. Verify that resistor R64 is adjusted properly by switching the RESERVE LOAD switch S1 from ON to OFF several times while observing that reading on differential voltmeter remains steady, then leave the switch in the OFF position. Proceed to step w. m. Connect load bank (figure 3-1) to PS1P2 using cable disconnected in step a., above. Connect load bank ground to PS1TP1 ground. Connect cable assembly, power supply test (part number 4023656-0501, figure 4-11, page 4-86) between PS1P1 and XPS1P1. Connect differential voltmeter, MIL-V-9989 between TP1 and TP2 of load bank (figure 3-1). Adjust RANGE control to 500-volt position. n. Place PS1 in position so that R63 and R64 are available for adjustment. Adjust resistor R64 (figure 4-23, page 4-217) fully counterclockwise (at least 20 turns). WARNING Lethal voltages are present when power is applied to test setup using load bank. These dangerous voltages are present on Al wire as shown in figure 3-1, on related resistors, terminals and wiring in load bank, and on Al terminal in open power supply.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
15. Power supply, voltage and overcurrent adjustments (Cont)	o. Set C-6280(P)/APX (AN/PM-239) MASTER to STBY for 1 minute, then to NORM.	
	p. Adjust resistor R63 (figure 4-23) for an indication of 310 +16, -6 vdc on the differential voltmeter.	310 $^{+16}_{-6}$ vdc
	q. Ensure that input power is less than the following limits: (1) 100 VA (115 vac at 0.869 Amp) ac voltage source. (2) 70 Watts (27.5 vdc at 2.54 Amp) dc voltage source.	
	r. Measure power supply voltages as directed in table 4-25, steps 2 through 9. If voltages do not meet the limits specified in table 4-25 and step p. above, adjust R63 until all voltages are within limits specified, including differential voltmeter reading.	
	s. Place switch S1 on load bank to ON.	
	t. Adjust resistor R64 clockwise until the output voltage reading on the differential voltmeter drops to zero indicating that the overcurrent circuit is just beginning to operate. Proper operation of the overcurrent circuit is indicated by periodic attempts to rise shown by any of the output voltages. This should occur at a 1- to 5-second interval.	

Table 4-43. Complete Alignment and Adjustment Procedures Using AN/UPM-98A (Cont)

STEP	PROCEDURE	REMARKS
15. Power supply, voltage and overcurrent adjustments (Cont)	u. Adjust resistor R64 counterclockwise until the output voltage reading on the differential voltmeter is approximately 310 +16, -6 vdc indicating that the overcurrent circuit is no longer operating. Set R64 approximately one turn further counterclockwise from this point.	$310\ ^{+16}_{-6}$ vdc
	v. Verify that resistor R64 is adjusted properly by switching S1 on load bank from ON to OFF several times while observing that reading on differential voltmeter remains steady. Then leave S1 in OFF position.	
	w. To reassemble and replace the power supply, use procedure in paragraph 4-332, steps 44. and 45. and paragraph 4-33aa.	

FREQ XTAL switch on the rf generator to SWEEP and the CW SOURCE INTL 1030 MHz switch on the same generator to INTL 1030 MHz. Set the PRF RANGE MULT switch to EXT +. Set the CHAN A AC/DC switch to AC.

(d) Ensure that CHAN A VIDEO INPUT is not connected.

4. Preliminary Procedures. The following procedures are done to establish a calibrated sweep response pattern on the AN/UPM-137 oscilloscope.

(a) Temporarily increase OUTPUT ATTEN 0-100 dBm dial setting on AN/APM-137 to -100 dBm.

(b) Sync the oscilloscope using the HORIZONTAL TRIG LEVEL and STABILITY controLs and adjust the SWEEP DELAY MULT 1-11 and TIME/DIV controls on the oscilloscope until the crystal markers appear. The markers should appear such that the -10 MHz marker is at the left edge of the oscilloscope graticule, the +10 MHz marker is at the right edge, and the 1030 MHz marker is in the center. This results in a horizontal scale of 2 MHz/cm. (See figure 4-6, page 4-60.)

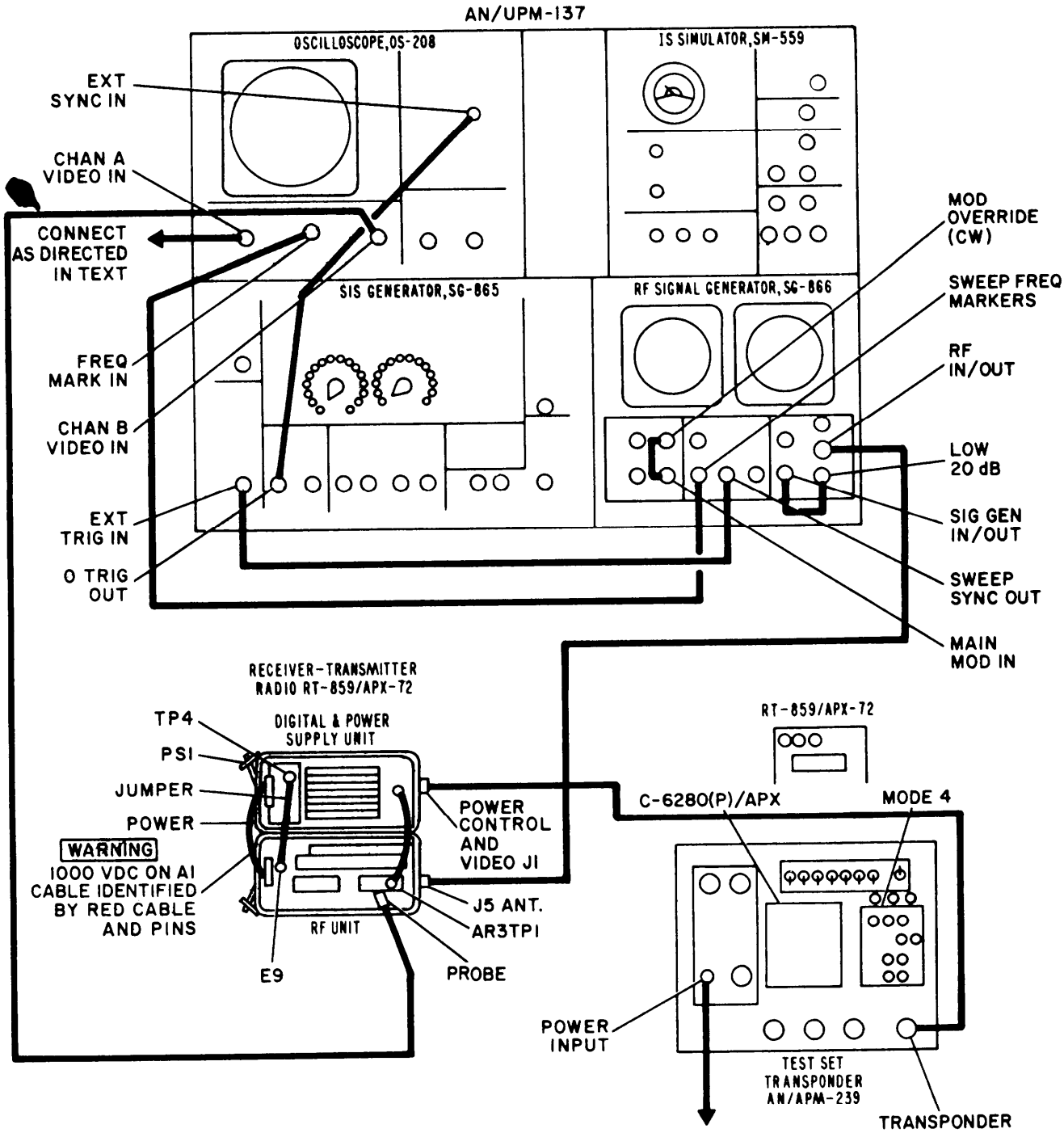


Figure 4-38. Alignment Test Setup, Using AN/UPM-137 Test Set

(c) Set CHAN A VOLT/DIV to .1. Reduce the OUTPUT ATTEN 0-100 dBm dial as required to obtain a swept frequency response pattern on the oscilloscope peaked near the center.

(d) Adjust the OUTPUT ATTEN 0-100 dBm dial until the sweep response is 4 cm high, spaced evenly above and below the horizontal center line of the graticule. The TIME/DIV control may be temporarily increased one step to more accurately determine the baseline. The 6 dB response point is now at the centerline and the 6 dB bandwidth may be observed.

(e) Perform the alignment procedures of table 4-44, page 4-289.

c. Subassembly Alignment. Alignment procedures to correct misalignments of individual subassemblies, determined during checkout procedures, and alignments required upon repair or replacement of subassemblies are listed in table 4-45, page 4-300. Following completion of alignment procedures, the receiver-transmitter shall be subjected to the checkout procedures of paragraph 4-12.

4-37. CALIBRATION. (Not Applicable)

4-38. TESTING.

4-39. The testing procedures required after repair or replacement of subassemblies and components of the receiver-transmitter shall consist of alignment as indicated in table 4-45, page 4-300 followed by the checkout procedures described in paragragh 4-12, page 4-45.

4-40. DIFFERENCE DATA.

4-41. Part number differences between the RT-859/APX-72 and the RT-859A/APX-72 are -indicated in table 4-46, page 4-301.

4-42. PREPARATION FOR STORAGE OR SHIPMENT.

4-43. STORAGE. The receiver-transmitter housing provides adequate protection for its contents, and the mountings (MT-3809\APX-72 and MT-3948/APX-72) are sufficiently sturdy that no additional protection is necessary during periods of limited storage.

4-44. SHIPMENT. The procedures for repackaging and shipment depends on the materials available and the conditions under which the equipment is to be shipped. Refer to Organization Maintenance Manual for RT-859\APX-72 (NAVSHIPS 0967-217-4010, TM 11-5895-490-20) and specifications MIL-E-17555F (Ships), MIL-E-17555 (USAF), and SB38-100 (Army) for instructions pertaining to preservation, packaging and packing.

Table 4-44. Complete Alignment and Adjustment Procedures Using AN\UPM-137

STEP	PROCEDURE	REMARKS
1. Receiver alignment	a. Connect equipment as shown in figure 4-38, page 4-287.	
	WARNING Terminals adjcacent to receiver tuning adjustments are at voltage levels hazardous to life.	
	b. Loosen locknuts on preselector adjustment Z1C1 and rf amplifier AR1C3.	
	c. Adjust Z1C1 for peak response at 1030 MHz. Normally Z1C2, Z1C3, AR1C1, and AR1C2 do not require adjustment. Should adjustment of Z1C1 not provide peak response at 1030 MHz, loosen locknuts and adjust Z1C2, Z1C3, AR1C1, AR1C2, and AR1C3 in given order for peak response.	Observe waveform on AN\UPM-137 oscilloscope for indication of 1030 MHz near peak of curve.
	d. Adjust Z1C1 and AR1C3 alternately for the best obtainable waveform about 1030 MHz. Obtain best compromise between peak response and waveform symmetry.	Monitor waveform on AN\UPM-137 oscilloscope.
	e. Adjust OUTPUT ATTEN 0-100 dBm control of AN\UPM-137 for 0.3 volt peak deflection (4 cm) of waveform.	
	f. Repeat step l.c. to obtain ±3.5 MHz at 6 dB points if necessary.	observe waveform for +3.5 MHz bandwidth from center frequency at 6 dB markers.

Table 4-44. Complete Alignment and Adjustment Procedures Using AN\UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
1. Receiver alignment (Cent)	g. When bandwidth of 7 MHz minimum has been achieved, tighten both adjustment locknuts using care to prevent change in tuning adjustments.	
	h. Measure center frequency and bandwidth for minimum performance standards using previously established horizontal calibration of 2 MHz/cm.	Performance standard center frequency 1030 +1.5 MHz and 6 dB bandwidth 7 MHz, minimum.
	i. Disconnect rf connector and cable assembly, part No. 4023657, figure 4-11, between AR3J1 and P3, then disconnect jumper wire between TP4 and E9.	Bandwidth waveform should disappear.
2. Voltage level adjustments (Does not apply for AR3, Part No. 4023409-0503)	a. Use a differential voltmeter MIL-V-9989 for this step. Set C-6280(P)\Apx (AN\APM-239) to STBY.	
	b. Connect positive lead of differential voltmeter to ground and negative lead to AR3TP3. Adjust AR3R76 for voltage reading of -4.5 vdc. Disconnect leads.	Read -4.5 ±0.025 vdc.
	c. Connect negative lead of differential voltmeter to ground and positive lead to AR3TP2. Adjust AR3R73 for voltage reading of +4.5 vdc. Disconnect leads.	Read +4.5 ±0.025 vdc.
3. Normal sensitivity adjustments for transponders equipped with AR3, Part No. 4023409-0501, or 4023409-0502.	a. Setup test equipment as shown in figure 4-4, page 4-47 with R-T sections separated, and perform the receiver normal triggering level sensitivity test defined in paragraph 4-12.c, page 4-51.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
3. (Cont)	Note: Leave the OUTPUT ATTEN 0-100 dBm dial at the setting that gives 90% of the suppression pulses. b. If necessary, readjust OUTPUT ATTEN 0-100 dBm dial to obtain a level of -77.5 dBm at ANT. J5 of receiver-transmitter. 1. Set C-6280(P) (AN/APM-239) MASTER switch to STBY. Turn MODE 1 switch of AN\UPM-137 to MODE 1 and MODE C switch to ON. Connect CHAN A VIDEO IN of oscilloscope to A1TP6 on receiver-transmitter. 2. Adjust A8R6 for maximum amplitude of the pulse at A1TP6. Measure from center of base line noise to center of peak pulse noise. If a maximum amplitude is less than 0.6 Volt minimum, receiver-transmitter is defective. If this pulse meets amplitude requirements, measure voltage difference between peak of base line noise and base of peak pulse noise. A measurement of 0.2 volt or more is acceptable, a measurement less than 0.2 volt indicates a defective receiver-transmitter. c. Set C-6280( ) (P)/APX (AN/APM-239) M-2 switch to ON.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
3. Normal sensitivity adjustments (Cont)	and MAIN MOD IN. Set C-6280(P)/APX (AN/APM-239) M-1, M-2, M-3\A, and M-C switches to ON.	
	d. Connect oscilloscope probe to A1TP2 and adjust A1R22 slowly CW until circuit begins to trigger on noise, then adjust A1R22 ccw until noise just disappears.	
	e. Disconnect cable to electronic counter from T connector on PRF COUNTER IN and connect it to SUPPRESSION OUT (AN/APM-239). Adjust A1R25 for a count of 450 on the electronic counter.	
3A. Normal sensitivity adjustments for transponders equipped with AR3, Part No. 4023409-0503	a. Perform the preliminary procedures and starting procedures of paragraphs 4-12.a and 4-12.b, page 4-46.	
	b. Perform the receiver normal sensitivity test of Table 4-16. If the minimum performance standards are not met, check the following test equipment settings: 1. Verify that the electronic counter indication at PRF COUNTER IN jack is 500. 2. Verify that the pulse width at CHAL/TAGVARAMP OUT jack is 0.8 microsecond at the 50% amplitude points.	

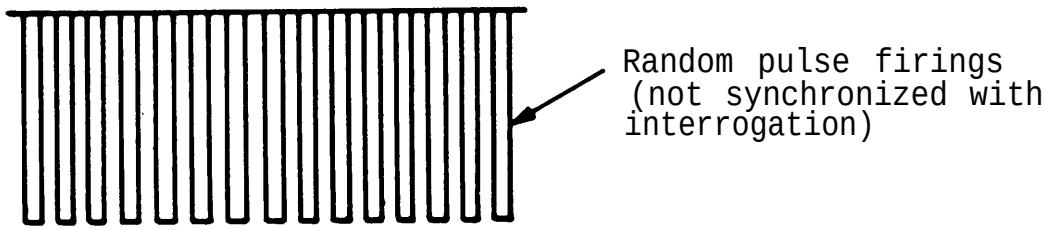
Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
3A. Normal sensitivity adjustments for transponders equipped with AR3, Part No. 4023409-0503 (Cont)	c. Adjust OUTPUT ATTEN 0-100 dBm control to obtain a level of -77.5 dBm at ANT. J5 of the receiver-transmitter. d. Set C-6280(P)/APX (AN/APM-239) MASTER switch to STBY. Turn MODE 1 switch of AN/UPM-137 to MODE 1 and MODE 3/A switch to ON. Connect CHAN A VIDEO IN of oscilloscope to A1TP6 on the receiver-transmitter. e. Adjust A8R6 for a 0.6 volt amplitude of the pulse at A1TP6 l Measure from center of base line noise to center of peak pulse noise. If a maximum amplitude that can be achieved is less than 0.6 volt, receiver-transmitter is defective. If this amplitude requirement is met, measure voltage difference between peak of base line noise and base of peak pulse noise. A measurement of 0.2 volt or more is acceptable. A measurement less than 0.2 volt indicates a defective receiver-transmitter.	

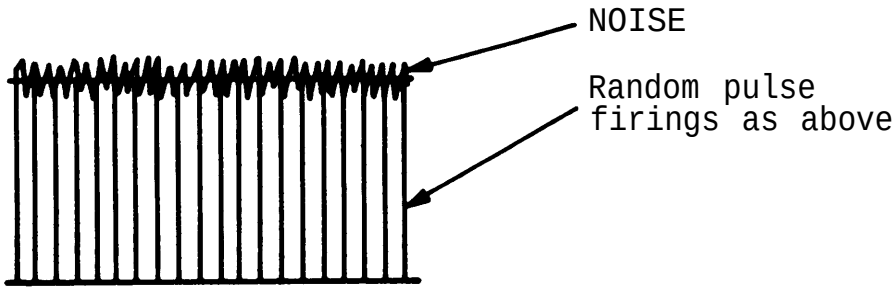
Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP		PROCEDURE	REMARKS
3A.	Normal sensitivity adjustments for transponders equipped with AR3, Part No. 4023409-0503 (Cont)	f. Connect the probes from both channels of the oscilloscope to A1TP3. Set both scope channels for a dc input with a deflection sensitivity of 0.5 volt/cm. Position the baseline of both traces near the bottom of the scope face with the waveform from each scope channel superimposed. Connect one of the scope probes to A1TP4. Adjust A1R22 until the baseline of the signal at A1TP4 is 0.3 volt above the baseline of the signal at A1TP3.	
		g. Temporarily disconnect the scope probe from A1TP3 and connect it to A1TP5. Adjust A1R25 as directed in figure 4-39, a through c, until the scope displays positive pulses, with the noise firings just eliminated between interrogations. (This adjustment should be made with a sweep speed of 100 microseconds/cm.) Rotate A1R25 another 1/4 turn ccw.	

(a) Turn A1R25 fully cw and observe the following waveform:



(b) Turn A1R25 ccw until the followinq waveform is observed:



(c) Continue to adjust A1R25 ccw until the noise firings between pulses (occurring at interrogation time) are just eliminated and the pulses are synchronized to interrogation time.

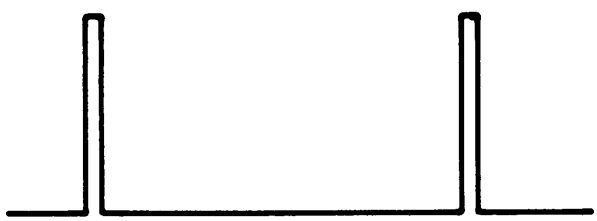


Figure 4-39. Adjustment of Waveform at A1TP5.

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP		PROCEDURE	REMARKS
3A.	Normal sensitivity adjustments for transponders equipped with AR3, Part No. 4023409-0503 (Cont)	h. Disconnect scope probe from A1TP5 and reconnect to A1TP3. Refer to figure 4-40 and adjust the OUTPUT ATTEN 0-100 dBm control to position the top of the pulse waveform at A1TP3 on a reference graticule near the top of the scope face. Increase the signal level by 5 dB (decrease the OUTPUT ATTEN 0-100 dBm setting) . Adjust A1R6 to position the top of the waveform at A1TP4 on the reference graticule.	
		i. Adjust OUTPUT ATTEN 0-100 dBm dial to obtain -47 dBm at ANT. J5 on receiver-transmitter. Disconnect jumper between AUX MOD IN and CHAL/TAG VAR AMP OUT, and connect it between MOD OVERRIDE (CW) and MAIN MOD IN. Set C-6280(P)/APX (AN/APM-239) M-1, M-2, M-3/A, and M-C switches to ON.	
		j. Connect oscilloscope probe to A1TP2 and adjust A1R22 slowly cw until circuit begins to trigger on noise. Then adjust A1R22 an additional 1/4 turn cw.	

Table 4-44. Complete Alignment and Adjustment procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
3A. Normal sensitivity adjustments for transponders equipped with AR3, Part No. 4023409-0503 (Cont)	k. Disconnect probe from A1TP2 and connect it to A1TP5. Adjust A1R25 slowly cw until noise appears on the scope display; then adjust A1R25 until the noise just disappears. Adjust A1R25 an additional 1/4 turn ccw. 1. Disconnect jumper between MAIN MOD IN and MOD OVERRIDE (CW) and connect it between CHAL/TAG VAR AMP OUT and AUX MOD IN. Set OUTPUT ATTEN *0-100* dBm dial to obtain -77.5 dBm at ANT. J5 on receiver-transmitter. Set C-6280(P)/APX (AN/APM-239) M-1, M-2, and M-3/A switches to OUT. m. Disconnect cable to electronic counter from T connector on PRF COUNTER IN and connect it to SUPPRESSION OUT (AN/APM-239). Adjust A8R6 for a count of 450 on the electronic counter (90% replies).	

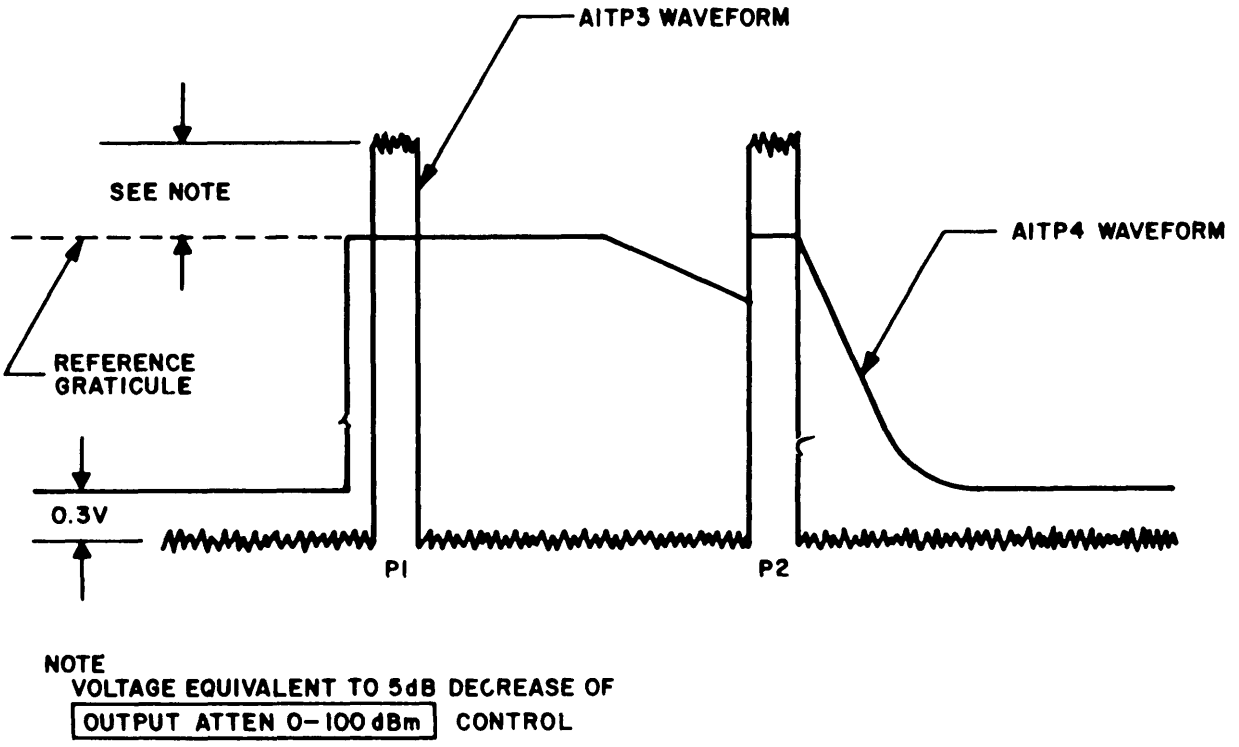


Figure 4-40. Normal Sensitivity Adjustments

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP		PROCEDURE	REMARKS
4. Ditch length adjustments (RT-859/ APX-72)	a.	Ensure C-6280(p)/Apx (AN/APM-239) MASTER switch is in STBY. Remove cables between ANT. J5 (receiver-transmitter) and RF IN/OUT on AN/UPM-137. Connect the 10-dB attenuator to ANT. J5 and a cable between the attenuator and SIG GEN IN/OUT.	
	b.	Set AUX ATTEN +3-60 dB dial to O and adjust OUTPUT ATTEN 0-100 dBm control to obtain -27 dBm at ANT. J5. Connect oscilloscope Channel A probe to A1TP4.	
	c.	Adjust A1R10 to obtain trapezoidal waveform with base line equal to 13.5 us. Disconnect probe from A1TP4.	See waveform at TP4 of figure 6-4.
4A. Wide pulse detector adjustments (RT-859A/ APX-72)	a.	Setup AN/UPM-137 using the preliminary and starting procedures in paragraphs 4-12.a and 4-12.b, page 4-46, establishing an output level 3 dB above MTL. Ensure that AUX-ATTEN-13-60 dB is set to 0.	
	b.	Set MODE 1 switch of AN/UPM-137 to MODE 1 (off) and MODE C switch to ON (up) l Set M1-TEST/ON/OUT switch of AN/APM-239 to OUT and MC-TEST/ON/OUT switch to ON. The C-6280(P)/APX MASTER switch should be set to STANDBY.	
	c.	Remove cable from AUX MOD IN and connect to CHAN B VIDEO IN of AN/UPM-137 oscilloscope. Set CHAN B 75Ω switch to IN.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
4A. Wide pulse detector adjustments (RT-859A/APX-72) (Cont)	d. Adjust the CHAL/TAG WIDTH control on the AN/UPM-137 for 1.4 µs pulse width. Reconnect cable to AUX MOD IN. Assure that the electronic counter is connected to SUPPRESSION OUT jack on AN/APM-239.	
	e. Adjust A1R10 until electronic counter indicates an average of 10 counts per second. Note: Adjust A1R10 cw to reduce the count.	
	f. Rotate the OUTPUT ATTEN on the AN/UPM-137 from 3 dB to 50 dB above MTL. If electronic counter indicates higher than an average ten counts, readjust A1R10.	
5. Side lobe suppression adjustments for transponders equipped with AR3, Part No. 4023409-0501, or 4023409-0502.	a. Ensure C-6280(P)/APX (AN/APM-239) MASTER switch is in STBY.	
	b. Connect CHAN B VIDEO IN of oscilloscope to VIDEO OUT on rf generator. Connect CHAL/TAG VAR AMP OUT of SIS generator to MAIN MOD IN of rf generator. Adjust AUX ATTEN +3-60 dB dial to O dB. Set the CHAL/TAG switch to SLS OUT and the SLS POSN control to NORM. Connect SLS OUT to AUX MOD IN. Verify that SLS pulse is present and equal in amplitude to the interrogation pulses on oscilloscope Channel B. Adjust AUX ATTEN +3-60 dB dial if necessary to obtain equality then increase dial reading by 9 dB.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
5. Side lobe suppression adjustments (Cont)	c. Adjust OUTPUT ATTEN 0-100 dBm control to obtain -64 dBm at ANT. J5 of receiver-transmitter. Connect CHAN A VIDEO IN of oscilloscope to A1TP2. Adjust A1R6 until ISLS pulse appears intermittently at A1TP2, then readjust until ISLS pulse disappears. Sweep OUTPUT ATTEN 0-100 dBm dial from 3 dB to 50 dB above MTL (77.5 dBm). If ISLS pulse reappears intermittently from 6 to 50 dB below MTL, repeat adjustments until ISLS does not appear in this range. Disconnect probe from A1TP2.	
	d. Setup the equipment as directed in step 3a, page 4-290. The AUX ATTEN and OUTPUT ATTEN should be set for a -77.5 dBm signal at ATN. J5. on the C-6280(P)/APX (AN/APM-239), set the M2-TEST/ON/OUT switch to ON and all other modes to OFF. On the SIS generator of the AN/UPM-137, set the CHAL/TAG CODER MODE 2 switch to ON and all other mode switches to off. Adjust A1R25 until counter indicates an average of 450 counts.	90% replies
	e. Set C-6280(P)/APX MASTER to STBY. Repeat steps 4.a. and 5.b. and c. and adjust A1R6 only if required. If A1R6 requires adjustment, repeat step 5.d. adjusting A1R25 only if required. If A1R25 requires adjustment, repeat complete cycle until no further adjustments are required.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP		PROCEDURE	REMARKS
5.	Side lobe suppression adjustments (Cont)	f. Restore equipment connections as stated in step 3.a.	
5A.	Side Lobe Suppression Adjustments for transponders equipped with AR3, Part No. 4023409-0503	a. Ensure that C-6280(P)/APX (AN/APM-239) MASTER switch is in STBY. b. Connect CHAN B VIDEO IN of oscilloscope to VIDEO OUT on rf generator. Connect CHAL/TAG VAR AMP OUT of SLS generator to MAIN MOD IN of rf generator. Adjust AUX ATTEN +3-60 dB dial to 0 dB. Set the CHAL/TAG switch to SLS OUT and the SLS POSN control to NORM. Connect SLS OUT to AUX MOD IN. Verify that SLS pulse is present and equal in amplitude to the interrogation pulses on oscilloscope Channel B. Verify that the width of all pulses is *0.8* microsecond. Adjust AUX ATTEN +3-60 dB dial if necessary to obtain equal amplitudes, and then increase dial reading by 9dB. Connect electronic counter to SUPPRESSION OUT jack on AN/APM-239. c. Sweep OUTPUT ATTEN 0-100 dBm control from 3 dB to 50 dB below minimum triggering level (MTL) (77.5 dBm). Verify that the electronic counter reads 500 (full firing) for levels from 6 dB to 50 dB below MTL. If misfiring occurs, adjust A1R6 slightly to obtain full firing.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP		PROCEDURE	REMARKS
5A.	Side Lobe Suppression Adjustments (Cont)	d. Restore the equipment connections as stated in paragraph 3A.a, above.	
6.	Low sensitivity adjustments	a. Set AUX ATTEN +3-60 dB dial to 0 dBm. On the C-6280(P)/APX (AN/APM-239), set the M2-TEST/ON/OUT switch to ON and all others to OFF. On the AN/UPM-137, set the CHAL/TAG CODER MODE 2 switch to ON (up) and all others to off. Adjust OUTPUT ATTEN 0-100 dBm dial to obtain -65 dBm at ANT. J5. Set C-6280(P)/APX (AN/APM-239) MASTER to LOW.	
		b. Adjust A8R5 until electronic counter indicates an average of 450. Set C-6280(P)/APX (AN/APM-239) MASTER to STBY.	90% replies
7.	Reply rate limiter adjustments	a. Assure that the MODE 2 code switches on the receiver-transmitter are set to 0000. Connect PRF COUNTER IN of AN/UPM-137 to O TRIG OUT. Set METER SELECT switch to *10,000.* Set the SIS generator PRF RANGE MULT to X1000 and adjust MULT 1-11 for a count of 3000 on the meter. Set OUTPUT ATTEN 0-100 dBm dial for -71 dBm at ANT. J5.	
		b. Adjust A2R89 for an electronic counter indication of 2000 counts average.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
8. Transmitter pulse width adjustments	a. Adjust the PRF MULT 1-11 control for a frequency count of 1800 on electronic counter. Set C-6280(P)/APX MASTER to NORM. Set OUTPUT ATTEN 0-100 dBm dial for -40 dBm at ANT. J5, and Channel B of oscilloscope at 0.5 V/CM.	
	b. Adjust A7R4 for a reply pulse width of 0.45 µs at the 50% amplitude points.	
9. Duty cycle control	a. Adjust the PRF MULT 1-11 control on the SIS generator for a count of 1700. Set the MODE 2 code switches on the receiver-transmitter to 7777.	
	b. Adjust A2R51 for an average counter indication of 1625.	
	c. Repeat procedures of step 7a., adjusting A2R89 for an average counter indication of 1200.	
10. Reply pulse spacing adjustments (RT-859/ APX-72 only)	a. Set MODE 2 code (receiver-transmitter) to 0000.	
	b. Set up the equipment as shown in figure 4-9 and described in paragraphs 4-12.i. and table 4-22 and perform all the frame spacing performance tests for the operating modes (1, 2, 3A, Test, and C Replies).	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
10. Reply pulse spacing adjustments (RT-859/APX-72 only) (Cont)	c. Adjust A4C1 so that F2 leading edge falls on 15th marker +0.05 µs.	Frame spacing 20.3 ±0.05 µs
	d. Set MODE 2 code to 0007. F2 should remain within ±0.05 µs (position scope display as required), if not, readjust A4C1 and repeat steps b. and c. until tolerance is met (XTAL MARKER to OFF).	
11. Transmitter frequency adjustments	a. Setup the equipment as shown in figure 4-5, page 4-52 and perform the transmitter frequency measurements of table 4-18, page 4-56 after first performing the starting procedures of paragraph 4-12b, page 4-46.	
	b. Adjust Z2C1, if required, to set transmitter on exact frequency by observing that the F_1-F_2 pulses peak symmetrically around the center marker when the markers are moved with the DELAY TRIG MULT 1-11 control. (See figure 4-6, view B.)	
	c. Perform transmitter power measurements of table 4-18, page 4-56. Adjust AR2C1 for peak power output of F1 and F2 pulses.	
	d. Repeat steps a, b, and c until no further adjustments are required.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
12. Mode 4 gate adjustments (RT-859A/APX-72, Part No. 4028683-0502 only)	a. Setup AN/UPM-137 for Mode 4 tests as described in paragraph 4-12.j. Establish a level 3 dB higher than MTL. b. The MODE 4 switch on the AN/UPM-137 should be ON. NOTE Use the extender board (see figure 4-14) to provide access to controls on the A3 Mode 4 board. c. Connect the AN/UPM-137 oscilloscope probe (Channel A) to A3TP6. d. Adjust A3R215 to obtain a 92-µs pulse. e. Connect the oscilloscope probe to A3TP8. f. Adjust A3R224 until this pulse is positioned 300 µs after the decode pulse of A3TP7. NOTE The pulse at TP7 starts 2.5 us after the leading edge of the 92- us pulse at TP6.	
13. Mode 4 reply limiter adjustments	a. Equipment should be connetted as shown in figure 4-10. The MODE 4 preliminary procedures should be performed and then the limiter performance test procedures of table 4-23. The Mode 4 REPLY switch on AN/APM-245 should be ON for the limiter tests.	

Table 4-44. Complete Alignment and Adjustment Procedures Using AN/UPM-137 (Cont)

STEP	PROCEDURE	REMARKS
13. Mode 4 reply limiter adjustments (Cont)	b. Adjust A3R29 or A3R1 on mode 4 boards with Part No. 116104-1, until an average rate of 2000 is indicated on electronic counter.	
14. Mode 4 audio level adjustments	a. Equipment should be connetted as shown in figure 4-10. The MODE 4 preliminary procedures should be performed and then the audio output performance test procedures of table 4-23.	
	b. Adjust A3R89 or A3R2 on mode 4 boards with part No. 116104-1, for a 3-volt peak-to-peak audio signal measured on the AN/UPM-137 oscilloscope.	
15.	Align power supply using procedures described in table 4-43, steps 15.a. through 15.w.	

Table 4-45. Alignment Procedures to be Performed After Repair or Replacement of a Subassembly

SUBASSEMBLY		ALIGNMENT PROCEDURE	REFERENCES TABLE 4-43 OR 4-44
Al	Processor	Complete alignment	Steps 1 thru 14
A2	Decoder	Reply rate limiter and duty cycle adjustments	Steps 7 and 9
A3	Mode 4	Mode 4 gate adjustment	Step 12
		AOC and audio adjustments	Steps 13 and 14
A4	Encoder clock	Reply pulse spacing	Step 10
A5	Encoder control	None	
A6	Encoder gating	None	
A7	Modulator	Transmitter pulse width alignment	Step 8
A8	Sensitivity	Normal and low sensitivity adjustments	Steps 3 and 6

Table 4-45. Alignment Procedures to be Performed After Repair or Replacement of a Subassembly (Cont)

SUBASSEMBLY	ALIGNMENT PROCEDURE	REFERENCES TABLE 4-43 or 4-44
AR1 RF amplifier	Receiver alignment and normal and low sensitivity adjustments	Steps 1, 3, and 6
AR2 Power amplifier	Transmitter power and frequency	Step 11
AR3 Detector and video amplifier	Voltage level adjustment	Step 2
DL1 Delay line	None	
PS1 Power supply	Voltage and overcurrent adjustments	Step 15 (Table 4-43 only, page 4-281)
Z1 Preselector	Receiver alignment	Step 1
Z2 Oscillator	Transmitter power and frequency	Step 11

Table 4-46. Difference Data

NOMENCLATURE*	ASSEMBLY USED WITH RT-859/APX-72	ASSEMBLY USED WITH RT-859A/APX-72
Processor (A1)	4030070-0502	4028683-0502
Decoder (A2)	4023412-0502	4023412-0504
Mode 4 (A3)	4023416-0502	4028683-0502 or 116104-1
Encoder Gating (A6)	4023414-0502	4023414-0504
Detector and Video Amplifier (AR3)	4023409-0501	4023409-0502 or 4023409-0503

*Assemblies not listed are identical in each model, and are interchangeable between models.

SECTION V

DEPOT MAINTENANCE PROCEDURES

PART 1. US ARMY PROCEDURES

5-1. GENERAL

NOTE

Unless otherwise noted, references to RT-8591APX-72 also apply to RT-859A\APX-72.

5-2. The US Army depot maintenance procedures for Receiver-Transmitter, Radio RT-859\APX-72 and Mountings MT-3809\APX-72 and MT-3948\APX-72 conform to the procedures found in Section IV of this manual. The type of repairs assigned to depot level only, consist of repair of main case, card ease, rf head, and unique repairs requiring more extensive shop facilities. Electronic special support equipment allocated at depot level for the RT-859\APX-72 is the same as used at the intermediate maintenance level described in table 4-1 of this manual.

5-3. DEPOT REBUILD OPERATIONS. Complete rebuild of the RT-85/APX-72, MT-3809/APX-72, and MT-3948\APX-72 and/or their individual components may be accomplished by depot maintenance facilities when authorized. Rebuild action will include all repairs, rebuild, and replacement operations necessary to make the equipment suitable for return to supply system stocks or for reissue to using organizations as equipment equivalent to new. Detailed procedures for making the repairs and adjustments established in the preceding portions of this manual, and such additional repair and rebuild operations as necessary, will be determined by the facility performing the work. Checkout procedures described in paragraph 4-6, of this manual, established the requirements that must be met by rebuilt or repaired equipment before it is returned to supply system stocks.

5-4. PARTS REPLACEMENT TECHNIQUES. The general parts replacement techniques and test procedures in Section IV of this manual permit complete rebuild and testing of the RT-859\APX-72.

5-5. DEPOT INSPECTION STANDARDS.

5-6. APPLICABILITY OF DEPOT INSPECTION STANDARDS. The RT-859/APX-72 must be tested thoroughly after rebuild or repair to ensure that it meets adequate performance standards for return to stock and reissue. The tests to ensure that the RT-8591APX-72 meets adequate performance standards are presented in checkout procedures in paragraph 4-9 of this manual. These tests are equivalent to those established for acceptance of equipment on contract. These tests shall be used to measure the performance of the repaired equipment. It is mandatory that repaired equipment to be reissued, or returned to stock for reissue, meet all of the performance standards described in this chapter.

5-7. APPLICABLE REFERENCES.

a. Repair Standards. Applicable procedures of the depot performing these tests and the general standards for repaired electronic equipment given in TB SIG 355-1, Depot Inspection Standard for Repaired Signal

Equipment, TB SIG 355-2, Depot Inspection Standard for Refinishing Repaired Signal Equipment, and TB SIG 355-3, Depot Inspection Standard for Moisture and Fungus Resistant Treatment, form a part of the requirements for testing the RT-859/APX-72.

b. Technical Publications. The other technical publications applicable to the RT-859/APX-72 are as follows:

Receiver-Transmitter, Radio RT-859/APX-72 --

Organizational Maintenance:
Publication - NAVSHIPS 0967-217-4010/TM 11-5895-490-20

Repair Parts and Special Tools List:
Publication - TM 11-5895-490-35P

Illustrated Parts Breakdown:
Publication - NAVAIR 16 - 30APX 72-3/
NAVSHIPS 0967-217 -4030/
T.O. 12P4-2APX72-4

c. Modification Work Orders. Perform all modification work orders applicable to the RT-859/APX-72 before making the tests specified. DA PAM 3-7, index of Modification Work Orders, lists all available MWO's.

5-8. TEST FACILITIES REQUIRED. The electronic test equipment required for depot testing are listed in table 4-1 of this manual .

5-9. GENERAL TEST REQUIREMENTS. Testing will be simplified when performed under conditions given in referenced paragraphs, tables, and figure illustrations listed in table 5-1.

Table 5-1. General Test Requirements

PROCEDURE	PARAGRAPH	TABLE	FIGURE
Preliminary Test Setup			
AN/APM-239	4-8a.l.	4-2	
AN/APM-123	4-8a.2.		
AN/UPM-98A	4-11a.2.	4-5	
AN/USM-207	4-11a.5.		
AN/APM-245	4-11j.2.	4-13	
AN/USM-203	4-36a.3.	4-42	
System Bench Test			
RT-859/APX-72	4-8a.3.		4-1
AN/APM-123	4-8b.	4-3, 4-4	4-1
Performance Tests and Measurements			
Modes 1, 2, 31A, and C	4-11a.-i.	4-6 thru 4-12	4-2
Mode 4	4-11j.	4-14	4-3
Power Supply	4-15b.3.	4-25	4-22
Alignment and Adjustment			
Complete System	4-35, 4-36a.	4-43	4-35
Subassemblies	4-36b.	4-45	

PART 2. USE OF TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT AN/APM-338

5-10. GENERAL .

5-11. Part 2 of this section contains instructions and information for performing depot maintenance procedures using Test Set, Electronic Circuit Plug-in Unit AN/APM-338 (hereinafter referred to as AN/APM-338). AN/APM–338 provides the capability for semi-automatic test and troubleshooting of the printed circuit card assemblies, detector and video amplifier, sensitivity, modulator and power supply of Receiver-Transmitter , Radio RT-859/APX-72 and RT-859A/APx-72. The necessary stimuli (pulse generators, signal conditioners, dc voltages , etc.) , interface circuits, and performance measurement circuits for comprehensive end-to–end functional checkout of the item under test are included in the AN/APM-338.

NOTE

All references to RT-859/APX-72 assemblies include those assemblies used in the RT-859/APX-72 and those assemblies used in the RT-859A/APX-72 which are identical to their counterparts in the RT-859/APX-72. All references to RT-859A assemblies include those assemblies which are used only in the RT-859A/APX-72.

5-12. PRINCIPLES OF OPERATION.

5-13. The AN/APM-338 contains a complete set of RT-859/APX-72 printed circuit card assemblies, Al through A6 and DL1, in a ‘card cage accessible to the operator. These card assemblies are electrically identical to those assemblies used in the RT-859/APX-72, and they constitute reference cards by which to compare the operation of those cards to be tested. A set of reference cards for the RT-859A/APX-72 is not required, since the differences in operation between models are compensated for by circuits within the AN/APM-338. To test any of the RT-859/APX-72 or RT-859A/APX-72 printed circuit card assemblies, Al through A6 and DL1, the operator removes the corresponding reference card and substitutes the card to be tested. Rotation of the appropriate TEST SELECTOR switch through each of its numbered positions will result in all FAULT INDICATOR lamps remaining extinguished if the card under test is in working order. A faulty card will cause the illumination of some of the FAULT INDICATOR lamps in some of the switch positions. The combination of lighted lamps and switch positions provides the key to the use of the fault isolation procedure tables (paragraph 5-29). Tests and fault isolation of the detector and video amplifier, sensitivity, modulator, and power supply assemblies are accomplished in the same manner, except that reference assemblies are not required.

5-14. DESCRIPTION OF AN\APM-338.

5-15. Associated with each of the slots or holding fixtures for RT-859/APX-72 or RT-859A/APX-72 assemblies to be tested is a TEST SELECTOR switch. The "0" position for each switch is the normal switch setting when the assembly with which it is associated is not being tested. To

safeguard against having more than one switch in an active (other than "O") position, a white lamp above each switch will light in all switch positions other than "O". When a TEST SELECTOR switch is rotated through its positions it will cause one or more of the red FAULT INDICATORS, A through G, to light if the assembly being tested is faulty. For some tests, the test switch should not be advanced too rapidly. The amber DELAY IN TEST indicator will light and remain lit until a sufficient time cycle has elapsed. The test switch should not be rotated to the next position until after this indicator is extinguished.

5-16. There are several adjustments which can be made to the Processor board (Al) under test to secure correct operation. Either of the amber CW or CCW lamps will light to show in which direction the adjustment should be made.

5-17. A red OVERLOAD INDICATOR lamp will light whenever a short circuit is present on the dc supply line with which the lamp is associated.

5-18. The BUILT IN TEST push-button provides a self-test function which verifies the operability of the interrogation circuits of the AN/APM-338.

5-19. INITIAL ADJUSTMENTS AND CONTROL SETTINGS.

5-20. Before applying power, check to see that each of the reference printed circuit cards, Al through A6 and DL1, are in place and correctly seated in each connector. Buffer assemblies must be plugged into cards as indicated in table 5-2.

Table 5-2. AN/APM-338 Buffer Assembly Connections

REFERENCE CARD	BUFFER ASSEMBLY
Processor (Al)	A34
Delay line (DL1)	none
Decoder (A2)	A35
Mode 4 (A3)	A36
Encoder Clock (A4)	A37
Encoder Control (A5)	none
Encoder Gating (A6)	A38

5-21. Buffer assemblies A30 and A31 must also be in place and correctly seated. These two assemblies are located in the front card cage, but are covered by a plate to prevent removal unless the AN/APM-338 requires maintenance. Make sure that all TEST SELECTOR switches are in the "0" positions.

5-22. When using the AN/APM-338 to test the modulator, sensitivity, detector and video amplifier, and power supply each assembly is installed in the following manner.

a. Modulator (A7). Orient the modulator assembly so that the terminals match the spring-loaded connections on the AN/APM-338, and the spring-loaded guide pins pass through the two mounting holes in the assembly. Press down evenly on both edges until the printed circuit board is held by the retaining clips.

b. Sensitivity (A8). This assembly is installed in the same manner as the modulator.

Detector and Video Amplifier (AR3). Rotate the holding fixture clockwise, thus swinging the cradle approximately 45 degrees. Place the video amplifier

in the cradle with the detector and coax at the top. The video output connector passes through a cutout in the cradle and a guide pin passes through one of the assembly mounting holes. Restore the holding fixture. Connect coaxial cable P2 (snap-on connector) to the video output and coaxial cable P1 (threaded connector) to the detector coax.

d. Power Supply (PS1). Place the power supply on the AN/APM-338 so that connector PSP1 engages the receptacle on the sloping front deck. Connect P3 from the test set front panel into PS1P2.

NOTE

References assemblies of these four items are not supplied as part of the AN/APM-338.

5-23. STARTUP AND SELF TEST.

5-24. Perform steps 1 through 6 of the operating instructions as shown in figure 5-1. These instructions are affixed to the cover of the AN/APM-338. If correct conditions are not obtained during self test, refer to the AN/APM-338 maintenance manual, NAVAIR 16-30APM338-1/T.O. 33D7-49-48-2/TM11-6625-2571-14, for maintenance procedures.

5-25. TESTS AND FAULT ISOLATION.

5-26. To check the performance of any of the RT-859/APX-72 or RT-859A/APX-72 assemblies, it is necessary to insert them into the appropriate position on the AN/APM-338 (first removing the reference card when one is provided). Rotation of the applicable TEST SELECTOR switch through all of its active positions, as explained for self test, will give a "go" condition (no FAULT INDICATORS lighted) if the assembly is good.

NOTE

Only one type of assembly may be tested at a time. Installing several different unknown assemblies can jeopardize the validity of the fault isolation procedures. When testing printed circuit card assemblies Al through A6 and DL1, none of the other four assemblies, A7, A8, AR3, or PS1, should be installed in the AN/APM-338.

5-27. If a FAULT INDICATOR lights during test of an assembly, and a valid self test has been obtained (paragraph 5-23), refer to the fault isolation procedures as described in paragraph 5-28.

5-28. USE OF FAULT ISOLATION PROCEDURES.

5-29. Tables 5-3 through 5-17 provide separate fault isolation procedures for each type of card or assembly which can be tested with the AN/APM-338. Separate tables are included for the RT-859A/APX-72 units. Each column in a fault isolation procedure table has the following application.

a. Test Sequence. This column contains a number corresponding to the position of the applicable TEST SELECTOR switch, and a letter corresponding to FAULT INDICATORS A through G. For example, if FAULT INDICATOR B is lighted when the TEST SELECTOR switch is in position 2, the fault isolation sequence is listed as test sequence 2B.

OPERATING INSTRUCTIONS FOR AN/APM-338

1. Connect power cable to J1 and plug into 115 VAC 400 Hertz power source.
2. Place all TEST SELECTOR switches in 0 position.
3. Place SENSITIVITY and MODULATOR switches in OFF position.
4. Seat buffer assemblies A34, A35, A36, A37, A38 with the appropriately marked RT-859 reference board.
5. Place POWER switch in ON position — allow one minute warm-up time.
6. Perform a system self-test as follows:
   NOTE: When an amber WAIT indicator lights, wait until the indicator turns off before proceeding to the next step.
   a. Press BUILT IN TEST switch — observe green lamp indication.
   b. Press OVERLOAD indicators, DELAY IN TEST indicators, and FAULT indicators. Observe that each indicator lights when depressed.
   c. Rotate A1 PROCESSOR switch clockwise through its indicated RT-859 test positions and observe that the white indicator above the switch lights and all red OVERLOAD, FAULT and amber ADJUST indicators remain off.

      Continue rotating the switch clockwise to 0. *NOTE:* Disregard any indicators that may come on while passing unmarked positions or RT-859A positions.

      Repeat the above for DL1 DELAY LINE, A2 DECODER, A3 MODE 4, A4 ENCODER CLOCK, A5 ENCODER CONTROL and A6 ENCODER GATING. *NOTE:* Use only POS 1 through 16 for the DECODER self test. When the ENCODER GATING switch is returned to 0, wait 30 seconds before additional testing is performed.
   d. Self Test of the VIDEO AMPLIFIER, POWER SUPPLY, MODULATOR and SENSITIVITY circuits can be performed by inserting a properly operating unit in the holding fixture, and operating the respective switches as in c.
   e. Self Test of the RT-859A A1 PROCESSOR, A3 MODE 4, and A6 ENCODER GATING circuitry can be performed by removing the reference printed wiring board and replacing it with a properly operating RT-859A board.

      Rotate the appropriate switch in a counter-clockwise direction observing the same lamp condition described in c.

      Continue rotating the switch counter-clockwise to 0. *NOTE:* Disregard any indicators that may come on while passing unmarked positions or RT-859 positions.
   f. Self Test of the RT–859A A2 DECODER can be performed by replacing the reference printed wiring board with a properly operating RT–859A board.

      Rotate the DECODER TEST SELECTOR switch clockwise through POS 17 observing the same lamp conditions described in c.

      Continue rotating the switch clockwise to 0. *NOTE:* Disregard any indicators that may come on while passing unmarked positions.
7. Test RT-859 boards A1, DL1, A2, A3, A4, A5 and A6 by substituting for the same reference board in the card cage and operating the TEST SELECTOR switch. If OVERLOAD, FAULT or ADJUST lights come on, consult the maintenance manual.
8. RT-859A Boards: Test A1 PROCESSOR, A3 MODE 4 and A6 ENCODER GATING assemblies of the RT-859A as described in 7; except rotate the TEST SELECTOR switch counter-clockwise from the 0 position.

   Test A2 DECODER by rotating the TEST SELECTOR switch clockwise through all 17 positions.
9. Test APX-72 assemblies AR3, PS1, A7 and A8 by inserting the assembly in its holding fixture and operating its TEST SELECTOR switch. If OVERLOAD, FAULT, or ADJUST lights come on, consult the maintenance manual.

Figure 5-1. Operating Instructions for Test Set AN/APM-338

b. Step No. This column lists the numbered steps to be taken to isolate the trouble which is causing a particular FAULT INDICATOR to light. For example, test sequence 1A for Processor (A1) lists three steps. Step 1 is performed first, then, depending upon the results obtained, the operator is directed to go to either step 2 (1A-2) or to step (1A-3).

c. Test Point. This column gives the test point location on the assembly under test which an oscilloscope or voltmeter as appropriate, is connected.

d. Normal Waveform. The conditions listed in this column for each step are normal at the test point for a properly operating assembly connected to the AN/APM-338 when the TEST SELECTOR switch is in the test sequence position. In comparing the amplitude and timing of observed waveforms with those shown in the tables, these facts should be kept in mind:

(1) Equipment employing IC's and transistors in digital circuits will tolerate greater deviation from average values than that to which the technician may be accustomed from other devices.

(2) Failures which cause fault lights to turn on will tend to be caused by major deviations from the illustrated waveforms, usually be complete absence of the waveform.

(3) DC levels of baselines or pulse peaks near the zero level may vary ±1 volt.

NOTE

Because of these circuit characteristics, variations of ±25% would be considered typical. Any waveforms to which the above does not apply will have appropriate limits indicated.

(4) DC levels representing the "l" outputs of IC gates, one shots, or flip-flops, will show considerable variation due to loading and wide tolerance in the device specification. Circuits driven by such outputs are always designed with ample safety factors.

(5) 'Timing, pulse width and amplitude designations in parenthesis are not significant to the particular test but are shown as a convenience in obtaining the oscilloscope presentation.

e. Action for Normal Waveform. The actions described in this column are taken if the normal waveform is present at the indicated test point. The waveforms illustrated and the voltage levels assigned are somewhat idealized. Small differences are to be expected from assembly to assembly. The quality of the test instruments used may result in small departures from the ideal. For example, waveforms may be influenced by the rise time of the oscilloscope used.

f. Action for Abnormal Waveform. When the correct waveform at the indicated test point is not obtained, the actions to be taken are described in this column l

5-30. The use of the fault isolation procedure table is predicated upon the following two rules.

a. Unless otherwise instructed in the tables, all fault indications which exist in position 1 of the TEST SELECTOR switch must be corrected before proceeding with position 2, and so on.

b. If more than one FAULT INDICATOR is lighted in a given position of the TEST SELECTOR switch, indicator A fault must be corrected before proceeding with indicator B fault, and so on, unless otherwise indicated.

NOTES FOR TABLE 5-3

PROCESSOR (Al), FAULT ISOLATION PROCEDURE FOR RT-859/APX-72

NOTE 1: Whenever this procedure indicates the replacement of an integrated circuit, first check that the dc power and ground connections are good. (Refer to schematic for pin numbers.)

NOTE 2. When it is suspected that an abnormal waveform could be caused by an integrated circuit having developed an input short, thereby loading the circuit being viewed, lift the input pin of the integrated circuit. If normal waveform is restored, replace the defective integrated circuit.

CAUTION

Integrated circuits can be damaged electrically if the soldering iron tip is not at ground potential.

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-8. X-72

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	Collector Q3	-0.5 V	Check connection between buffer A34 and TP4	If collector of Q3 is greater than +2V, go to 1A-2. If collector of Q3 is less than -3.6 V go to 1A-3
	2	Base Q5	+2.5 to -3 V	Check Q2, Q5 for C-E short	Check R21, R22 -6 V supply
	3	Base Q5	+2.5 V to -3 V	Check CR2, R6, Q1 for C-E short	Check R23, R22 +6 V supply
1B	1	A1TP6	-0.25 V	Check connection between buffer A34 and TP6	Check C1, Q2, Q25

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

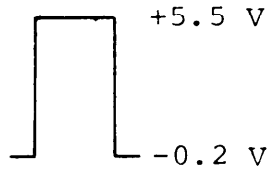
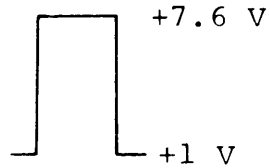
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1 CW ADJ	1	Collector Q3	Adjust R22 for +0.1 V to -0.5 V. If unobtainable, signal is abnormal.	Check connection between buffer A34 and TP4	Check Q5, R22
1 CCW ADJ	1	Collector Q3	Adjust R22 for -0.9 V to -0.3 V. If unobtainable, signal is abnormal.	Check connection between buffer A34 and TP4	Check Q5, Q1, R22
2A	1	A1TP6		Check connection between buffer A34 and TP6	Go to 2A-2
	2	Collector Q18		Check Q20, Q19, R60, R59, R58, C1, C15	Go to 2A-3

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

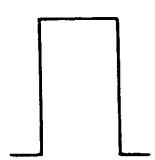
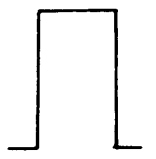
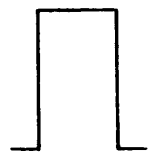
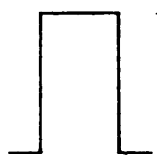
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	3	A1-22		Check Q18, R57, R55, R56, C13, L5	Check connection at XA1-22
2B	1	A1TP3		Check connection between buffer A34 and TP3	Go to 2B-2
	2	Anode CR3		Check CR3	Go to 2B-3
	3	DL1 IN		Replace DL1	Check track to R2, R3, C1

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

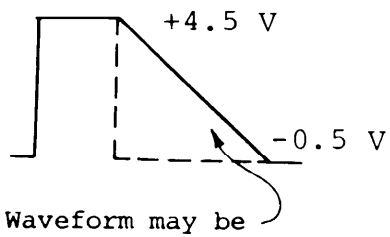
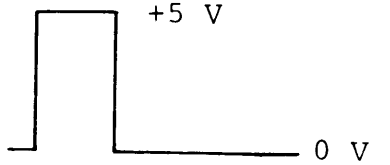
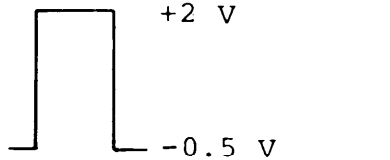
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2C	1	A1TP4		Check connection between buffer A34 and TP4	Go to 2C-2
	2	Collector Q1		Check Q2, C2	Check Q1, R2
2 CW/ CCW	1	Base Q1	-3.4 V to -5.2 V (Adjustment range of R6)	Check Q1, R3, R7	Check R1, CR2, R6
3A	1	A1TP2		Check connection between buffer A34 and TP2	Go to 3A-2

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

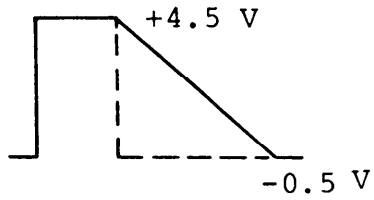
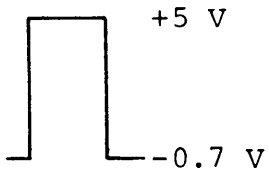
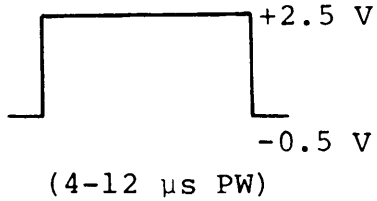
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A (Cont)	2	A1A1 Pin 3		Go to 3A-3	Check track to collector Q3
	3	A1A1 Pin 2		Check A1A1	Check track to junction R5 and CR3
3B	1	A1TP5		Check connection between buffer A34 and TP5	NOTE: Adjust A1R25 approximately 25 turns CCW. If lamp B remains lighted go to 3B-2
	2	A1A3 Pin 3	+2 V to -3.6 V	Go to 3B-4	Go to 3B-3

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

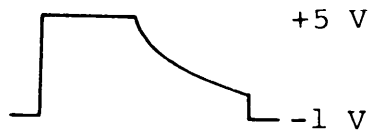
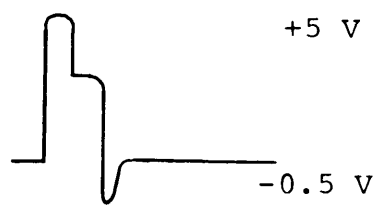
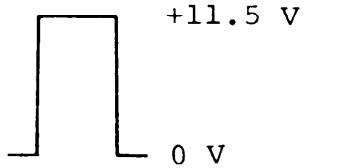
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3B (Cont)	3	Anode CR12	+2.5 V to -3 V	Check CR12	Check R25, R26
	4	A1A3 Pin 2		Check A1A3	Go to 3B-5
	5	Collector Q27		Check Q25, R87, C23	Check Q27, R83, R84, R85, R86, R54, VR2
3C	1	A1-11		Check connection at XA1-11	Go to 3C-2

Table 5-3. Processor (A1) , Fault Isolation Procedure for RT-859/APX-72 (Cont)

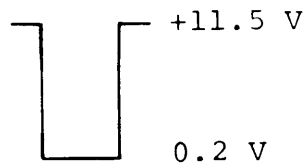
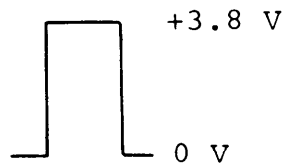
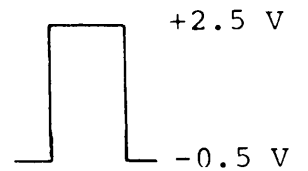
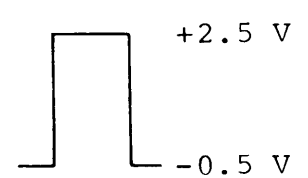
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3C (Cont)	2	Collector Q11		Check Q12, R39 L4, CR9	Go to 3C-3
	3	Collector Q9		Check Q11, R38, R52, R81, RT2	Go to 3C-4
	4	Base Q16		Check Q15, Q16, Q17, R31, R76, R37, R40, C12, R15, R18, R28	Go to 3C-5
	5	A1A2 Pin 7		Check R18 and track to Q16 Base	Go to 3C-6

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

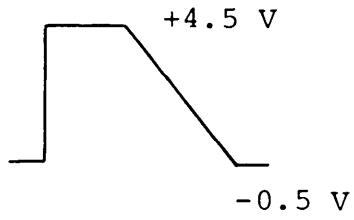
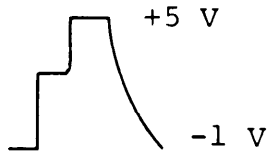
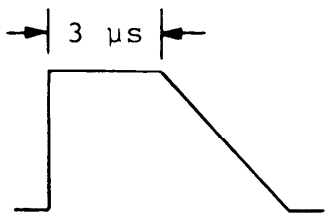
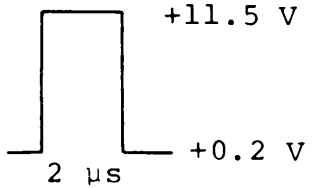
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3C (Cont)	6	A1A2 Pin 3		Go to 3C-7	Check track to Collector Q3
	7	A1A2 Pin 2		Check A1A2	Check CR16, R17, R16, CR8, C20
4A	1	A1TP4		Check connection between buffer A34 and TP4	Go to 4A-2
	2	Collector Q10		Go to 4B-2	Check Q10, CR4, R42, R43, R44, R45, C10

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

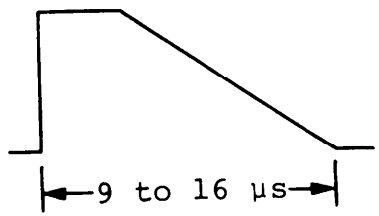
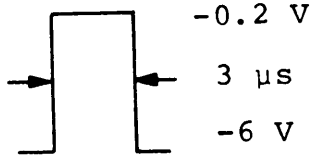
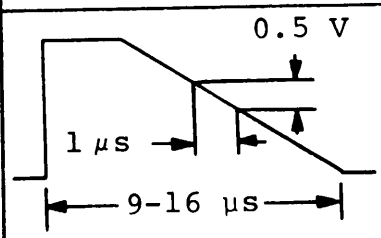
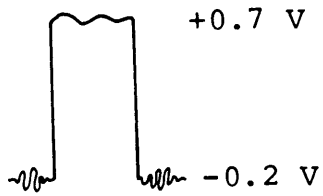
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4B	1	A1TP4		Check connection between buffer A34 and TP4	Go to 4B-2
	2	Collector Q4		Check Q3, R8, R9, R10, R11	Check Q4, R12, R13, R14, C4, C5, CR6, CR17
4 CW/ CCW	1	A1TP4		Check connection between buffer A34 and TP4	Check Q3, R8, R9, R10, R11, R12, Q4
5C	1	A1TP6		Check connection between buffer A34 and TP6	Go to 5C-2

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

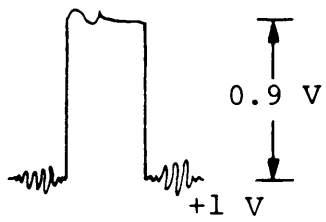
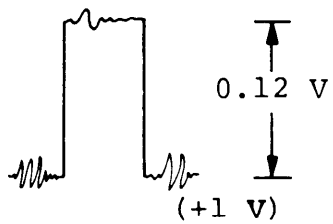
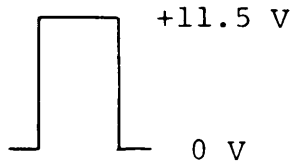
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5C (Cont)	2	Collector Q18		Check Q19, Q20, R58, R59, R60	Go to 5C-3
	3	A1-22		Check Q18, R55, R56, R57, C13	Check connection at XA1-22
5 CW/ CCW	1	Anode CR12	+2.5 V to -3 V (Adjustment range of R25)	Check CR12, R27, CR19, R88	Check R25, R24, R26
6A	1	A1-5		Check connection at XA1-5	Go to 6A-2

Table 5-3, Processor (A1), Fault Isolation Procedure for RT-859\APX-72 (Cont)

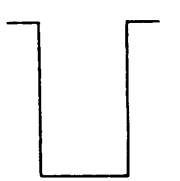
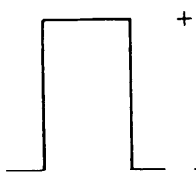
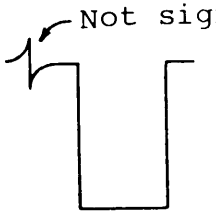
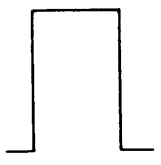
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6A (Cont)	2	Collector Q13		Check Q14, CR15, R48, R49, R46	Go to 6A-3
	3	Collector Q23		Check Q13, R51, R50, C19	Go to 6A-4
	4	Collector Q21		Check Q23, Q22, CR1, R71, R72, R69, R67, R70, C18, R68, R65, R77, C16, C17	Go to 6A-5
	5	A1-B		Check Q21, R64, R62, R100	Check connection at XA1-B

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

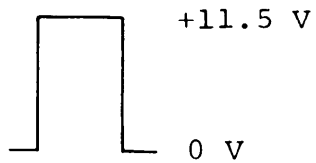
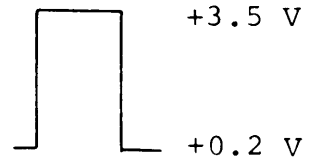
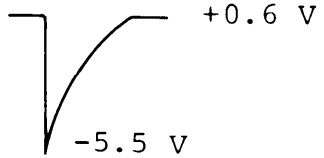
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B	1	A1-5	 PW = .6 to 1 µs	Check connection at XA1-5	Go to 6B-2
	2	Collector Q23	 PW = .6 to 1 µs	Check Q14, Q13, CR15, R46, R48, R49, R50, R51, C18	Go to 6B-3
	3	Base Q23		Check Q23, R71, R72, R51, C18, C19	C17, R69, R70, RT1
7A	1	A1TP2	-0.5 V No pulses present	Check connection at XA1-5	Go to 7A-2

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

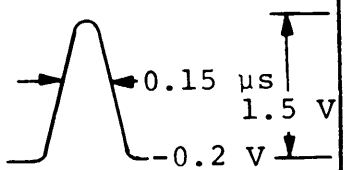
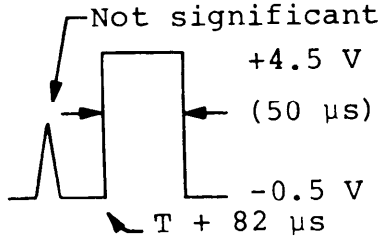
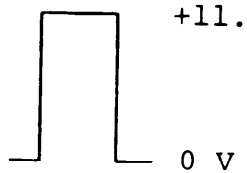
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A (Cont)	2	A1TP6		Check DL-1	Check connection at A1-22
8A	1	A1-5	0 V No pulses present	Check connection at XA1-5	Go to 8A-2
	2	A1-B		Check R66, track to collector Q21	Check connection at A1-B
8B	1	A1TP2		Check connection between buffer A34 and TP2	Go to 8B-2
	2	Emitter Q29	More positive than -0.6 V	Check Q29, CR24, R93, R89, R94	Go to 8B-3

Table 5-3. Processor (A1), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8B (Cont)	3	Emitter Q31	+11 V	Check Q30, CR25, R6	Check Q31, VR1, R98, R95, R97
9B	1	A1-11	 Single Pulse	Check connection at XA1-11	Check Q9, CR10, CR11, R35, R36, R41
10A	1	A1-5	0 V No pulses present	Check connection at XA1-5	Go to 10A-2
	2	A1-F	+12 V	Check Q26, CR18, CR14, R78, R79, R80, R82, R34	Check connection at XA1-F
11A	1	A1-Y	+5 V	Check CR13	Check connection at XA1-Y

NOTES FOR TABLE 5-4

PROCESSOR (A1), FAULT ISOLATION PROCEDURE FOR RT-859A/APX-72

NOTE 1: Whenever this procedure indicates the replacement of an integrated circuit, first check that the dc power and ground connections are good. (Refer to schematic for pin numbers.)

NOTE 2: When it is suspected that an abnormal waveform could be caused by an integrated circuit having developed an input short, thereby loading the circuit being viewed, lift the input pin of the integrated circuit. If normal waveform is restored, replace the defective integrated circuit.

CAUTION

Integrated circuits can be damaged electrically if the soldering iron tip is not at ground potential.

Table 5-4. Processor (A1), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

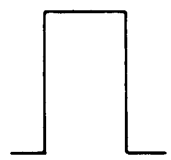
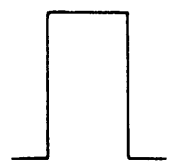
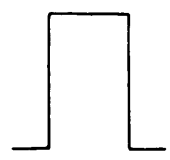
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2 CW ADJ.	1	A1A3 Pin 6	ADJ R-22 Range Full CW should read -1.9 to -1.3 volts (with CCW indicator ON). Full CCW should read +2 to +4 volts (with CW indicator ON). If unobtainable, or if obtainable and indicator is not ON, signal is abnormal.	Check connection between buffer A34 and TP4	Check Q13, CR6, R22, Q9, Q10 for C-E short, R99, A1A3
2 CCW ADJ.	1	A1A3 Pin 6		Check connection between buffer A34 and TP4	Check Q13, CR6, R22 A1A3
3A	1	A1TP6		Check connection between buffer A34 and TP6	Go to 3A-2
	2	A1A1 Pin 3		Check A1, A1A1, R16, R5, R4, R3, L5, L6, C27, C28, C29, C2	Go to 3A-3
	3	A1-22		Check R103, R1, R2, C1	Check connection at XA1-22

Table 5-4. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

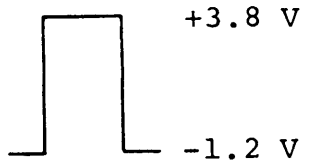
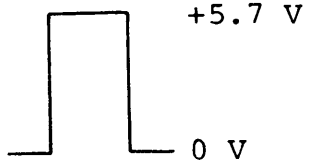
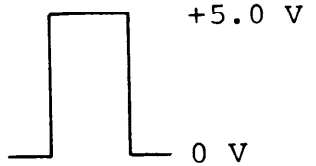
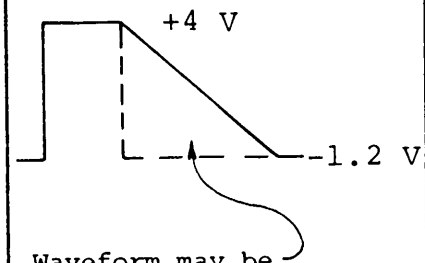
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3B	1	A1TP3		Check connection between buffer A34 and TP3	Go to 3B-2
	2	Anode CR3		Check CR3, CR4	Go to 3B-3
	3	DL1 IN		Check, replace DL1, R7	Check track to R7, R96
3C	1	A1TP4		Check connection between buffer A34 and TP4	Go to 3C-2

Table 5-4. Processor (Al), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

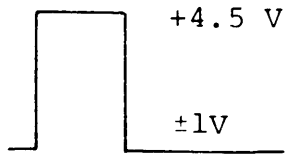
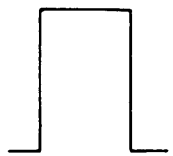
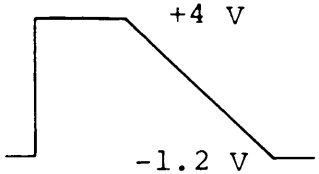
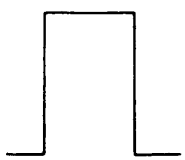
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3C (Cont)	2	Collector Q5	 (Depends on R6 setting)	Check Q9, Q10, C5	Check Q5, R96
3 CW/ CCW	1	Base Q5	-3.4 V to -5.2 V (Adjustment range of R6)	Check Q5, R26	Check CR2, R6, R24
4A	1	A1TP2		Check connection between buffer A34 and TP2	Go to 4A-2
	2	A1A3 Pin 13		Go to 4A-3	Check track to Emitter Q10
	3	A1A3 Pin 12		Check A1A3	Check track to junction R23 and CR4

Table 5-4. Processor (A1), Fault Isolation Procedure for RT-859A\APX-72 (Cont)

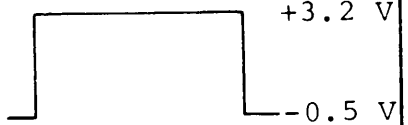
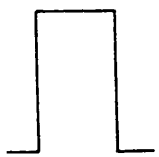
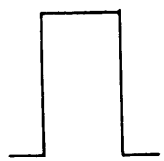
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4B	1	A1TP5	 +3.2 V -0.5 V	Check connection between buffer A34 and TP5	ADJ. A1R25 to approximately 25 turns C.W. If lamp B remains lighted go to 4B-2.
	2	A1A4 Pin 13	+5.2 V to -6 V Adjustable by A1R25	Go to 4B-3	Check CR17, R58, R25
	3	A1A4 Pin 12	 +3 V -0.5 V	Check, replace A1A4	Check Q15, R44, R45, R46. Go to 4B-4
	4	Collector Q7	 +3.5 V 0 V	Check Q8, R42, C7	Check Q7, R109, R41, R110, RT3, R37, R38
4C	1	A1TP1	 +11.5 V 0 V	Check connection at XA1-11	Go to 4C-2

Table 5-4. Processor (A1), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

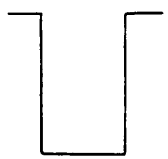
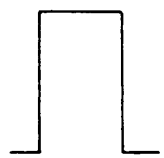
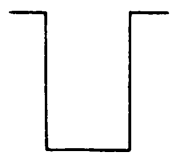
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4C (Cont)	2	Collector Q29	 +12.8 V +0.2 V	Check Q30, R51	Go to 4C-3
	3	A1A6 Pin 11	 +3 V -0.2 V	Check Q29, CR15, R68, R67, RT1, L4, R65, R64, R63, C13	Go to 4C-4
	4	A1A6 Pin 13	+3.3 V	Go to 4C-6	Go to 4C-5
	5	A1A5 Pin 5	-0.8 V	Replace A1A5	Check A1A5, A1A7 (lift Pin 3), Q3, R97 replace as required.
	6	A1A5 Pin 12	 +3.3 V +0.2 V	Check track to A1A6 Pin 12 replace A1A6	Go to 4C-7

Table 5-4. Processor (A1), Isolation Procedure for RT-859A/APX-72 (Cont)

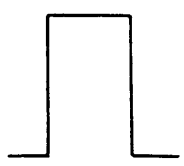
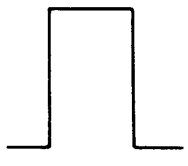
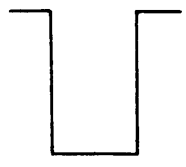
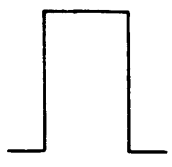
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4C (Cont)	7	A1A5 Pin 13	+2.5 V	Go to 4C-8	Check A1A7
	8	A1A5 Pin 1	 +3.3 V -0.5 V	Go to 4C-9	Go to 4A-1
	9	A1A5 Pin 2	 +3.3 V +0.2 V	Check, replace A1A5	Go to 4C-10
	10	A1A6 Pin 4	 +3.3 V 0.2 V	Check, replace A1A6	Go to 4C-11
	11	A1A7 Pin 11	 +3.3 V -0.5 V	Check, replace A1A7	Go to 4C-12

Table 5-4. Processor (A1), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

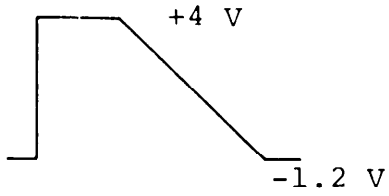
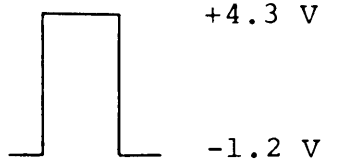
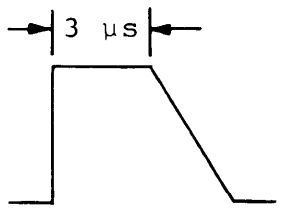
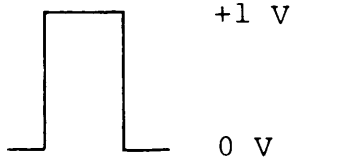
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4C (Cont)	12	A1A3 Pin 6		Go to 4C-13	Check R99, track to Emitter Q10
	13	A1A3 Pin 5		Replace A1A3	Check, Replace, CR7, CR8, R29
5A	1	A1TP4		Check connection between buffer A34 and TP4	Check Q28, CR21, A1A7 & A1A5, R47, R48, R49, R50, C11
5B	1	A1TP4		Check connection between buffer A34 and TP4	Check A1A5, A1A7, Q12, Q11, R30, R31, R32, R33, R34, R36, CR24, CR25, C6
6C	1	A1TP6		Check connection between buffer A34 and TP4	Return to Step 3A-1 and check A1A1 circuit for low gain (< 7)

Table 5-4. Processor (A1) , Fault Isolation Procedure for RT-859A/APX-72 (Cont)

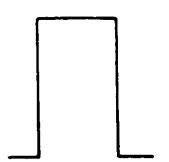
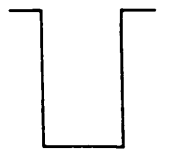
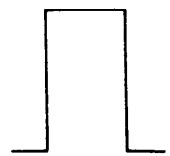
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6 CW/ CCW	1	A1A4 Pin 13	+5.2 V to -6 V, adjustable by A1R25	Check connection between buffer A34 and TP5	Check R25, CR17, R98, R43, CR98 and A1A4
7A	1		 +11.5 V 0 V	Check connection at XA1-5	Go to 7A-2
	2	Collector Q23	 +12.5 V 0 V	Check Q24, R82	Go to 7A-3
	3	Collector Q21	 +2.8 V +0.2 V	Check Q23, CR14, R81, R80, R77, R79, C18, R76	Lift collector Q17 if waveshape still abnormal go to 7A-7. If waveshape is restored go to 7A-4.
	4	A1A6 Pin 8	+0.2 V	Check Q17, R106, R107	Go to 7A-5

Table 5-4, Processor (Al), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

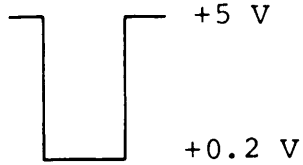
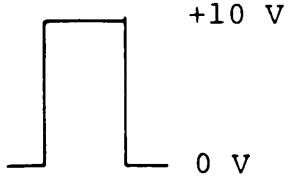
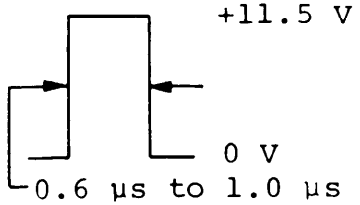
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A (Cont)	5	A1A6 Pin 9	+6 V	Go to 7A-6	Go to 9A-1
	6	A1A6 Pin 10	+3.3 V	Check, replace A1A6	Go to 11B-1
	7	Collector Q19		Check Q20, Q21, CR16, CR23, CR26, R74, R75, R73, R72	Go to 7A-8
	8	A1-B		Check Q19, R71, R70, R68	Check connection at XA1-B
7B	1	A1-5		Check connection at XA1-5	Go to 7B-2

Table 5-4. processor (Al), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

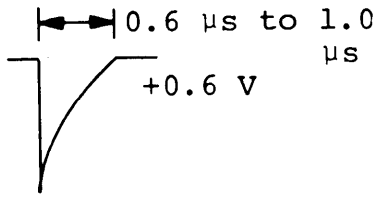
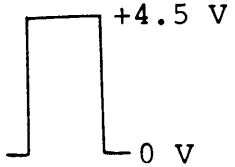
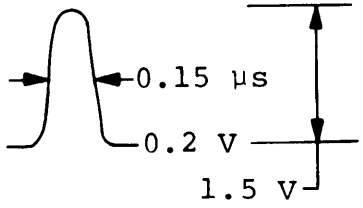
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7B (Cont)	2	Base Q21		Check Q21, C18, CR14, Q23, Q24	Check Q21, RT2, R74, R75, C19, CR16, CR26
7C	1	XA1-19		Check connection at XA1-19	Check Q22, R85, R86, R87, C22
8A	1	A1TP2	-0.5 V No pulses present	Check connection at XA1-5	Go to 8A-2
	2	A1TP6		Check DL-1	Check connection at A1-22

Table 5-4. Processor (A1), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

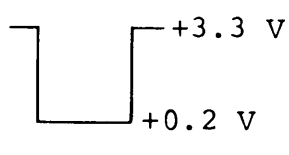
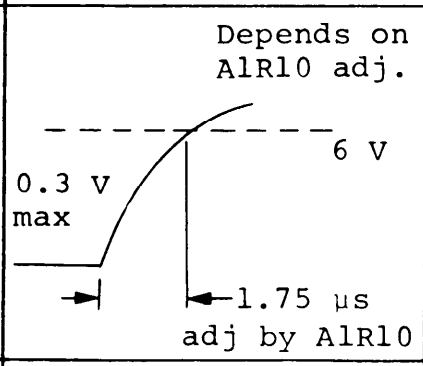
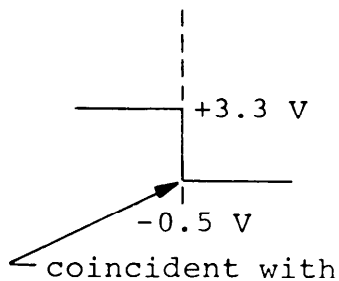
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A	1	A1-5	0 V No pulses present	Check connection at XA1-5	Go to 9A-2
	2	A1A5 Pin 12		Go to 9A-3	Return to Step 3A-1
	3	Collector Q25		Go to 9A-4	Check Q25, R52, R53, R54, R55, R10, CR12, C14
	4	A1A4 Pin 8		Go to 9A-5	Replace A1A4

Table 5-4. Processor (Al), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

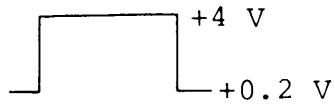
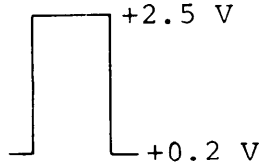
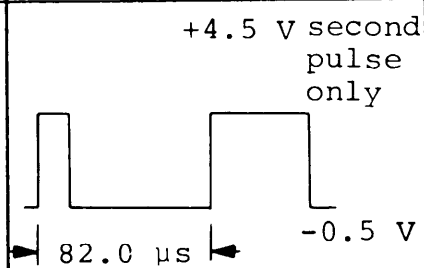
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A (Cont)	5	Collector Q27		Go to 9A-6	Check Q26, Q27, CR13, R56, R57, R58, R59, R60, R61, C15, C16
	6	A1A6 Pin 8		Check, replace Q17, R106, R107	Check, replace A1A6
9B	1	A1TP2		Go to 9B-2	Check connection between buffer A34 and TP2
	2	Base Q31	Same as 9B-1	Go to 9B-3	Check Q14, CR11, VR3, R19, R20, R21, R95
	3	A1A2 Pin 8	+11 V	Check VR1, R14	Check Q31, R100, R18, C4, R15, A1A2

Table 5-4. Processor (A1), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

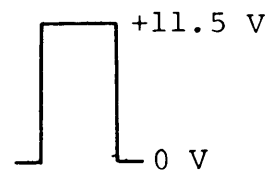
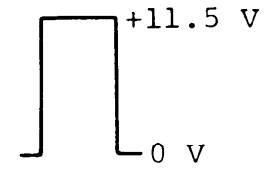
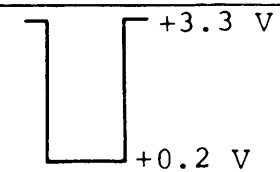
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10A	1	A1-5	0 V No pulses present	Check connection at XA1-5	Check Q2, CR10, CR5, R8, R9, R11
11A	1	A1-Y	+ 5 V	Check CR18	Check connection at XA1-Y
11B	1	A1-5	 Single Pulse	Check connection at XA1-5	If IND A is lighted go to 11A-1. If no pulses are present go to 11B-2
	2	A1-11	 Single Pulse	Go to 11B-8	Go to 11B-3
	3	A1A6 Pin 13		Replace A1A6	Go to 11B-4

Table 5-4. Processor (Al), Fault. Isolation Procedure for RT-859A\APX-72 (Cont)

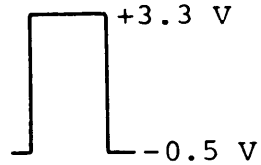
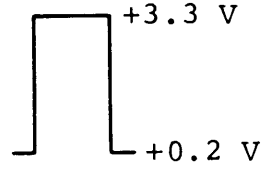
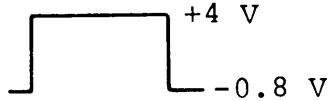
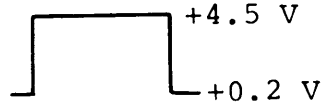
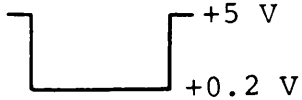
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11B (Cont)	4	A1A5 Pin 4		Go to 11B-5	Check track to A1A3 Pin 1. Replace A1A5
	5	A1A5 Pin 3		Go to 11B-6	Check track to A1A6 Pin 6. Replace A1A5
	6	A1A5 Pin 5		Replace A1A5	Go to 11B-7
	7	XA1-2		Check Q3, R97	Check connection at XA1-2
	8	A1A7 Pin 4		Go to 11B-9	Replace A1A7

Table 5-4. Processor (A1), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

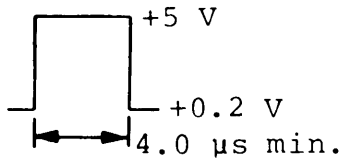
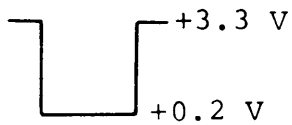
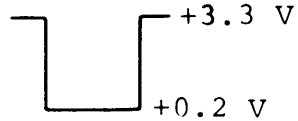
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11B (Cont)	9	Collector Q16		Go to 11B-10	Check, Replace Q16, R90, R89, R88, C8
	10	A1A7 Pin 6		Go to 11B-11	Replace A1A7
	11	A1A6 Pin 3		Check, replace A1A6	Check Q17, R106, R107

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	Collector Q32		Check for secure connection between buffer assembly A35 and the board under test	Go to 1A-2
	2	Cathode CR39		Check Q32, CR40, CR41, CR42, CR43	If Lamp B is not lighted, proceed to 1A-3. If Lamp B is lighted, proceed to Test Sequence 1B-1
	3	Collector Q45		Check CR39, CR31, CR32	Go to 1A-4
	4	A2-16		Replace Q45	Check for secure, connection between Decoder Board and Test Set

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1B	1	Collector Q24	+0.3 V max	Check connections between TP5 and Q24, TP5 and buffer assembly A35	Go to 1B-2
	2	Base Q24	+0.6 V	Check Q24	Replace Q24 if voltage is +6 VDC at base of Q24
1C	1	Rotate Switch to Position 2 and observe Lamp A. If Lamp A lights, proceed to Test Sequence 2A-1. If Lamp A remains off return Switch to Position 1 and proceed to Test Sequence 1C-2.			
	2	Collector Q43	+0.3 V max	Check connection between collector of Q43 and TP3; between TP3 and buffer assembly A35	Go to 1C-3
	3	Collector Q42	+6.4 V	Check Q43, R133, R134, R135, R136	Go to 1C-4

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859\APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1C (Cont)	4	Junction of CR35, CR36, CR37	-0.3 V	Check Q42, R130, R131	Go to 1C-5
	5	Anode CR35	+0.3 V	Proceed to 2A-1	Check Q26, R80, R81
2A	1	Anode CR36	-0.6 V	Check connections between CR36 and TP1, between TP1 and buffer assembly A35	Go to 2A-2
	2	Base Q40	+25 V	Check Q40, Q41 R127, R128	Disconnect C43 and observe base of Q40. If voltage level is +25 VDC check C43. If base voltage remains abnormal, check C45

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

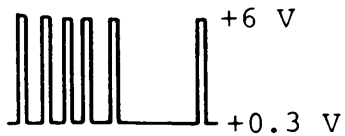
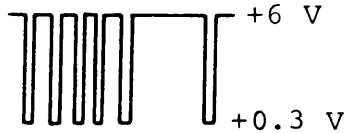
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2B	1	Collector Q33		Check connections between Q33 and TP7; between TP7 and buffer assembly A35	Proceed to 2B-2
	2	Collector Q34		Check Q33, CR25, CR26, CR27, CR28, CR29, C36, R106, R146	Check Q34, CR30, R109, R110, R111, C37
2C	1	Anode CR26	+0.3 V max	Go to 2C-2	Check C2, R5
	2	Anode CR27	+0.3 V max	Go to 2C-3	Check C12, R28

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

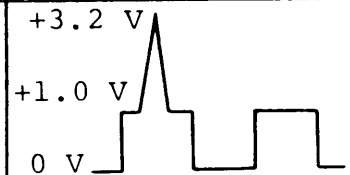
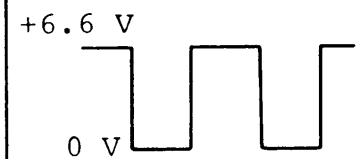
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2C (Cont)	3	Anode CR28	+0.3 V max	Go to 2C-4	Check C20, R63
	4	Anode CR29	-0.3 V	NA	Check C33, R102
3A	1	Collector Q9	 Temporarily remove buffer to observe true peak. Disregard fault indicators.	Check connections between Q9 and TP4, TP4 and buffer assembly A35	Go to 3A-2
	2	Collector Q8		Check Q9, R27, R29, R30, C13	Go to 3A-3

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72

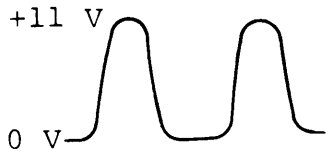
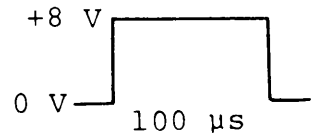
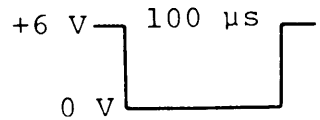
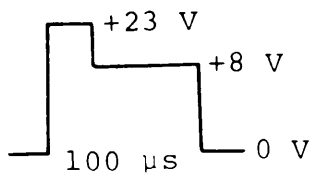
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A (Cont)	3	A2-60		Check Q8, CR4, CR5, R24, R25, R26, C11	Check connections between Pin 60 and Test Set
3B	1	Collector Q43		Check connections between Q3 and TP3 and between TP3 and XA2P1-35	Go to 3B-2
	2	Collector Q42		Check Q43, R133, R134, R135, R136	Go to 3B-3
	3	Cathode CR35		Check Q42, R130, R131	Go to 3B-4

Table 5-5. Decoder (A2), Fault Islation Procedure for RT-859/APX-72 (Cont)

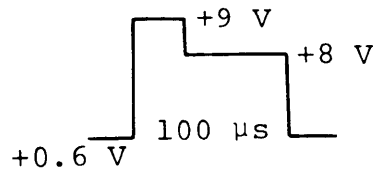
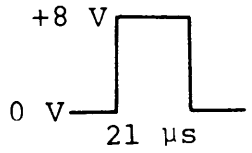
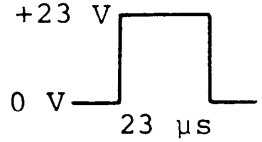
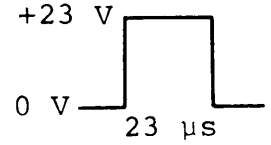
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3B (Cont)	4	Anode CR35		Check CR35, CR36	Go to 3B-5
	5	A2-31		Check Q25, Q26, CR16, C27, CR36, R78, R79, R80, R81, R75, R76, R77, C6	Check connection between Pin 31 and test set
3C	1	Emitter Q41		Check connections between TP1 and XA2P1-36	Go to 3C-2
	2	Collector Q40		Check Q41, CR35, CR36, R147, R148, R149, R150, R129	Go to 3C-3

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

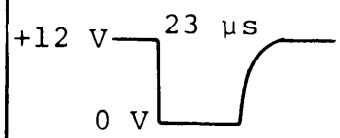
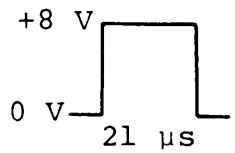
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3C (Cont)	3	Collector Q37		Check Q40, Q41, C42, C43, R121, R127	Go to 3C-4
	4	A2-39		Check Q37,R120, R119, R118, C42	Check connection at XA2-39
4A	1	Collector Q17	0 V	Check connections between TP2 and buffer assembly A35	If Indicator 4C is also lighted, go to 4C-1 If indicator 4C is not lighted, go to 4A-2
	2	Base Q18	+8 V	Go to 4A-3	Check CR12, Q18, R56, R57, R58

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	3	Base Q17	The dc voltage at this point must be equal to or greater than the voltage at the base of Q18	Check Q17, R55, R54	Go to 4A-4
	4	Collector Q28	+12 V	Go to 4A-5	Go to 4A-7
	5	Collector Q11	+12 V	Go to 4A-6	Go to 4A-12
	6	Collector Q15	+12 V	Visually inspect board for short circuit between track leading from XA2P1-2 and ground	Go to 4A-17

Table 5-5, Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	7	Base Q29	+0.3 V to +10 V depending on setting of R89	Go to 4A-8	Check Q29, CR44, R89, R88, R90, R155
	8	Base Q28	0 V	Check Q28, Q29, R85, R86	Go to 4A-9
	9	Base Q49	0 V	Check Q49, R154	Go to 4A-10
	10	Collector Q47	+17 V	Check Q27, C28, R83, R84	Go to 4A-11
	11	Collector Q26	+0.3 V max	Check Q47, R15, R16, R17, R13, R14, C6	Check Q26, R81, R80, C27

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	12	Base Q12	+4.2 V	Go to 4A-13	Check CR43, Q12, R39, R40, R153
	13	Base Q11	0 V	Check Q11, Q12, R37, R38	Go to 4A-14
	14	Base Q48	0 V	Check Q48, R152	Go to 4A-15
	15	Collector Q46	+16 V	Check Q10, R35, R36, C15	Go to 4A-16
	16	Base Q46	-1.0 V	Check Q46	Check C5, R8, R9

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	17	Base Q16	+2.0 V to +9.0 V depending on setting of R51	Go to 4A-18	Check CR10, Q16, R51, R50, R52
	18	Base Q15	0 V	Check Q15, Q16, R48, R47	Go to 4A-19
	19	Base Q14	0 V	Check Q14, Q15, R46	Go to 4A-20
	20	Emitter Q13	+12.6 V	Go to 4A-21	Check CR7, C17, R43
	21	Base Q13	A dc voltage approximately 1.2 V more positive than the emitter of Q13	Check Q13, R44, R45, C18	Check C52, C16, R41

Table 5-5, Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

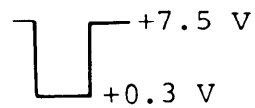
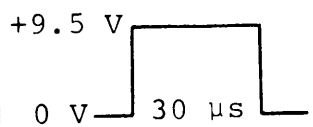
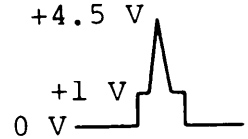
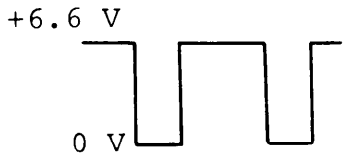
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4C	1	Collector Q45		Check CR39	Check Q45, R145, R144, R143, C53 Check connection at XA2-16
5A	1	Collector Q24		Check connections between TP5 and buffer A35	Go to 5A-2
	2	Collector Q36		Check Q23, Q24, Q44, CR15, C22, C24, C25, C26, C5, C35, R66, R67, R68, R69, R70, R71, R72, R73, R74	Go to 5A-3
	3	Collector Q35		Check Q36, C39, R115, R116, R117	Go to 5A-4

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5A (Cont)	4	A2 Pin 25	+10.5 V  0 V	Check Q35, R112, R113, C38, CR34, C39	Check connections at Pin 25
5B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 5B-2
	2	Base Q12	+4.2 V	Go to 5B-3	Check CR3, Q12, R39, R40, R153
	3	Base Q11	+4.5 V	Check Q11, Q12, R37, R38	Go to 5B-4
	4	Base Q48	+5 V	Check Q48, Q11, R152	Go to 5B-5
	5	Collector Q46	+17.5 V  0 V 30 µs	Check Q10, C15, R35, R36	Check Q46, R8, R9, R10, R11, R12

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

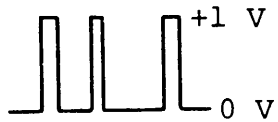
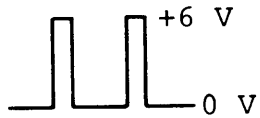
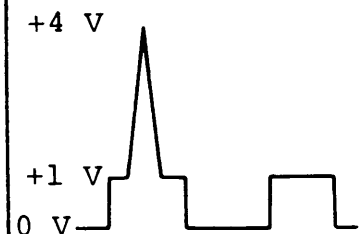
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5C	1	Collector Q9		Check connections between TP5 and XA2P1-57; between XA2P1-57 and the Test Set	If indicator 5A is also lighted, go to 5A-1 first. If indicator 5A is not lighted, go to 5C-2
	2	TP8		Check CR41	Check CR31
6A	1	Collector Q2		Check connections and interface between Pin 61 and the Test Set	Go to 6A-2
	2	Collector Q1		Check Q2, R7, R4, R6, C3	Go to 6A-3

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

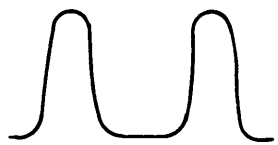
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6A (Cont)	3	Pin 63 of Decoder Board	+10 V  0 V	Go to 6A-4	Check connections and interface between Pin 61 and the Test Set
	4	Cathode CR1	-1 V	Check CR1, Q1, R1, R2, R3	Check connection and interface between Pin 62 and the Test Set
6B	1	Collector Q17	+8 V	Check connections between the collector of Q17 and TP2. Check interface between buffer A35 and TP2	If Lamp 6A is also lighted, refer to Test Sequence 6A-1. If Lamp 6A is not lighted go to 6B-2
	2	Base Q29	A dc voltage between +0.3 V and +10 V depending upon adjustment of R89	Take note of the dc voltage at base of Q29 and go to 6B-3	Check R89, CR44, R88, R90

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B (Cont)	3	Base Q28	A dc voltage more positive than the voltage at base of Q29	Check Q28, R86, CR11	If the voltage at the base of Q28 is greater than +1 VDC go to 6B-4 If the voltage at the base of Q28 is less than +1 VDC go to 6B-5
	4	Monitor the base of Q29 and simultaneously turn the R89 ADJ control (located on buffer A35) in a counter-clockwise direction. Turn until the voltage at the base of Q29 is less positive than the voltage at the base of Q28. At this point, indicator 6B should turn off. NOTE: Do not adjust R89 any further than required to turn off 6B. If the voltage at the base of Q29 does not vary as R89 is adjusted, check R89, CR44, R88. If the voltage at the base of Q29 can be adjusted to a value less positive than the voltage at the base of Q28, but indicator 6B does not turn off check Q28, Q29, CR11, R85, R86.			
	5	Base Q49	A dc voltage more positive than the voltage at base of Q29	Check Q49, R154	Go to 6B-6

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

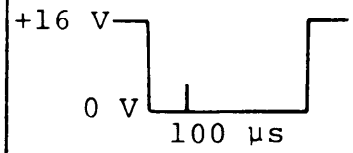
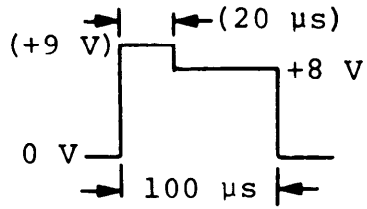
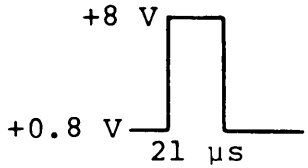
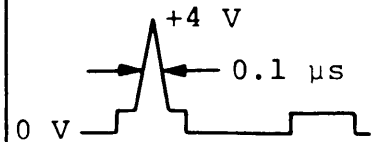
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B (Cont)	6	Collector Q47		Check Q27, C28, R83, R84	Go to 6B-7
	7	Collector Q26		Check Q47, R13, R14, R15	Go to 6B-8
	8	Pin 31 of Decoder Board		Check Q25, Q26, C27, CR16, R76, R77, R78, R80, R81, CR36, CR37	Check connection between Pin 31 of the Decoder board and the Test Set
6C	1	Collector Q2		NA	If pulse is wider than 0.2 µs check CR26

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

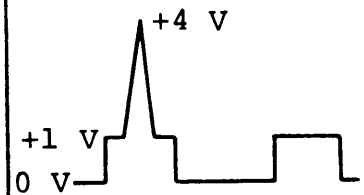
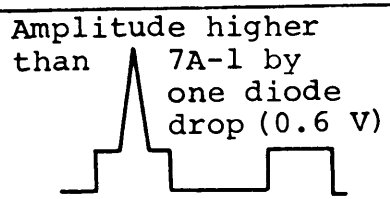
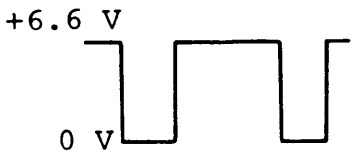
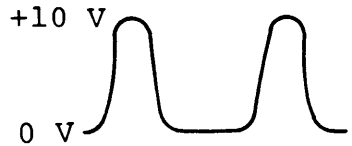
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A	1	Cathode CR21		Check track connection between cathode CR21 and Pin 15. Check connection between Pin 15 and the Test Set	Go to 7A-2
	2	Collector Q22		Check CR21	Go to 7A-3
	3	Collector Q21		Check Q22, CR24, R94, R96, R97	Go to 7A-4
	4	Pin 50		Go to 7A-5	Check connections between Pin 50 of Decoder and the Test Set Check C29

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A (Cont)	5	Cathode CR19	-1 V	Check CR19, Q21, R93, CR20, R91, R92	Check track between cathode CR19 and Pin 47 of Decoder Board. Check connection between Pin 47 and the Test Set
7B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	If Indicators 7A and 7C are both lighted refer to Test Sequence 7A-1 before proceeding with 7B-1. If Indicator 7C is lighted, refer to Test Sequence 7C-1 before proceeding with 7B-1. If Indicator 7B is the only lighted indicator, go to 7B-2.
	2	Base Q16	A dc voltage between +2 V and +9 V, depending upon adjustment of R51.	Take note of the dc voltage at the base of Q16 and go to 7B-3	Check R51, CR10, R50, R52

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7B (Cont)	3	Base Q15	A dc voltage more positive than the voltage at the base of Q16.	Check Q15, CR9, R48	If the voltage at the base of Q15 is greater than +2.0 VDC go to 7B-4. If the voltage at the base of Q15 is less than +2.0 VDC, go to 7B-5.
	4	Monitor the base of Q16 and simultaneously turn the R51 Adj. control (located on buffer A35) in a counter-clockwise direction. Turn until the voltage at the base of Q16 is less positive than the voltage at the base of Q15. At this point, indicator 7B should turn off. If the voltage at the base of Q16 does not vary as R51 is adjusted, check R51, CR10, R50. If the voltage at the base of Q16 can be adjusted to a value less positive than the voltage at the base of Q15 but Indicator 7B does not turn off, check Q15, Q16, R47.			
	5	Base Q14	A dc voltage 2.6 V or larger.	Check Q14, R46	Go to 7B-6

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

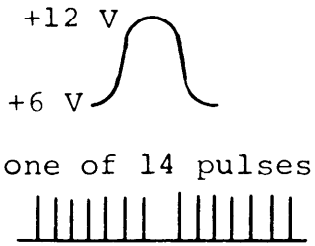
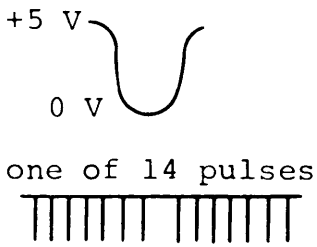
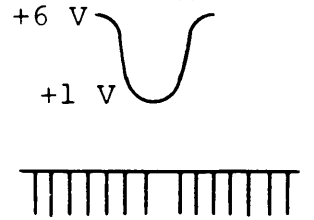
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7B (Cont)	6	Collector Q13		Check C18, R44, R45, Q14	Go to 7B-7
	7	A2 Pin 33		Check Q13, CR7, C17, C16, R141, R41, R42, R43	Check VR1, C52 Check connection between Pin 33 of Decoder Board and Test Set
7C	1	A2 Pin 32		Check connection between Pin 32 and the Test Set	Check C52, VR1, R142
8A	1	Collector Q17	0 V	Check connection between TP2 and buffer A35	Go to 8A-2

Table 5-5. Decoder (A2), Fault Isolation procedure for RT-859/APX-72 (Cont)

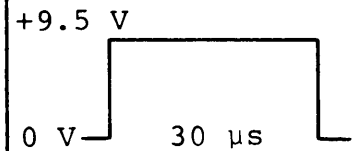
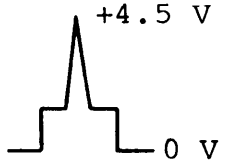
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8A (Cont)	2	Base Q12	+4.2 V	Go to 8A-3	Check CR3, R39, R40, R153
	3	Base Q11	A dc voltage less than +4.5 V	Check Q11, Q12, R37, R38	If pulses appear at the base of Q11 check C15, R35, R36
9A	1	Collector Q24		Check connection between TP5 and buffer A35	Go to 9A-2
	2	Collector Q36		Check Q23, Q24, Q45, CR15, C22, C24, C25, C26, C5, C35, R66, R67, R68, R69, R70, R71, R72, R73, R74	Go to 9A-3

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

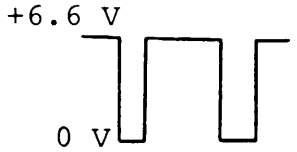
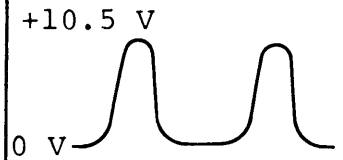
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A (Cont)	3	Collector Q35		Check Q36, C39, R115, R116, R117	Go to 9A-4
	4	A2 Pin 25		Check Q35, R112, R113, C38, CR34, C39	Check connections at Pin 25
9B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 9B-2
	2	Base Q12	+4.5 V	Go to 9B-3	Check CR3, Q12, R39, R40, R153

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

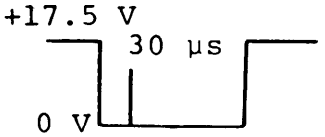
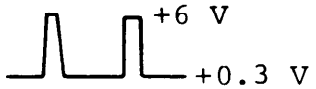
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9B (Cont)	3	Base Q11	+4.5 V	Check Q11, Q12, R37, R38	Go to 9B-4
	4	Base Q48	+5 V	Check Q48, Q11, R152	Go to 9B-5
	5	Collector Q46		Check Q10, C15, R35, R36	Check Q46, R8, R9, R10, R11, R12
9C	1	Collector Q22		Check connections between TP5 and XA2P1-15; between XA2P1-15 and the Test Set	If indicator 9A is also lighted, go to 9A-1 first. If indicator 9A is not lighted go to 9C-2.
	2	TP8		Check CR43, CR21	NA

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

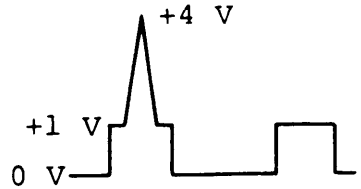
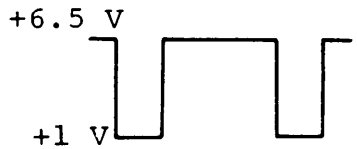
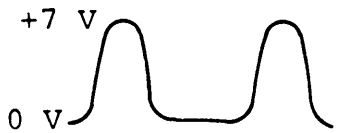
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10B	1	Collector Q20		Check track between collector Q20 and Pin 20, check connection between Pin 20 and the Test Set	Go to 10B-2
	2	Collector Q19		Check Q9, R30, R27, R29	Go to 10B-3
	3	Pin 21 of Decoder Board		Go to 10B-4	Check C19 Check connections between Pin 21 of Decoder and the Test Set
	4	Cathode CR13	-1 V	Check CR13, Q19, CR14, C21, R59, R60, R61	Check connection between Pin 54 and the Test Set

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

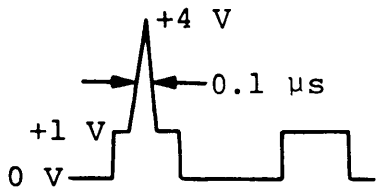
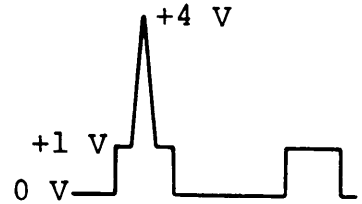
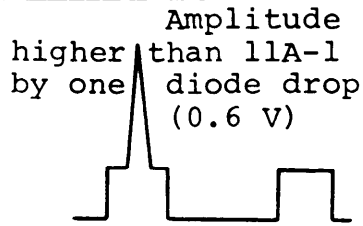
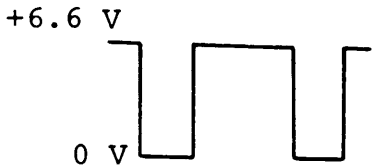
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10C	1	Collector Q20		NA	For a pulse wider than 0.2 µs check CR28
11A	1	Cathode CR24		Check track connection between cathode CR24 and Pin 15. Check connection between Pin 15 and the Test Set	Go to 11A-2
	2	Collector Q31		Check CR24	Go to 11A-3
	3	Collector Q30		Check Q31, CR21, R101, R103, R104	Go to 11A-4

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

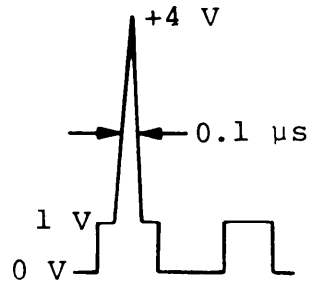
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11A (Cont)	4	Pin 43		Go to 11A-5	Check C32 Check connection between Pin 43 of Decoder and the Test Set
	5	Cathode CR22	-1 V	Check CR22, Q30, CR23, R98, R99, R100	Check track between cathode CR22 and Pin 41 of Decoder Board. Check connections between Pin 41 and the Test Set.
11C	1	Anode CR29			For a pulse wider than 0.2 µs, check CR29

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

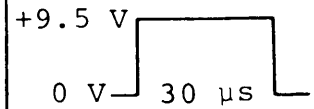
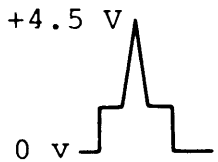
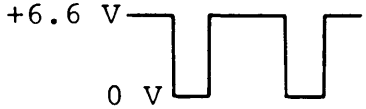
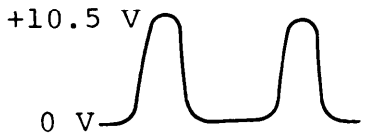
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12A	1	Collector Q24		Check connection between TP5 and buffer A35	Go to 12A-2
	2	Collector Q36		Check Q23, Q24, Q44, CR15, C22, C24, C25, C26, C5, C35, R66, R67, R68, R69, R70, R71, R72, R73, R74	Go to 12A-3
	3	Collector Q35		Check Q36, C39, R115, R116, R117	Go to 12A-4
	4	A2 Pin 25		Check Q35, R112, R113, C38, CR34, C39	Check connections at Pin 25

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

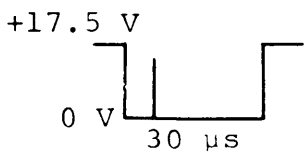
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 12B-2
	2	Base Q12	+4.5 V	Go to 12B-3	Check CR3, Q12, R39, R40, R153
	3	Base Q11	+4.5 V	Check Q11, Q12, R37, R38	Go to 12B-4
	4	Base Q48	+5.0 V	Check Q48, Q11, R152	Go to 12B-5
	5	Collector Q46		Check Q10, C15, R35, R36	Check Q46, R8, R9, R10, R11, R12

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

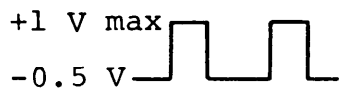
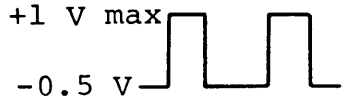
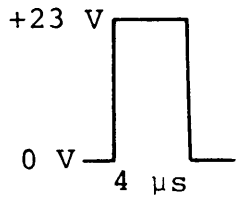
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12C	1	Anode CR40	0 V (base line)	Go to 12C-2	Check CR40
	2	Anode CR42		Go to 12C-3	Check CR42
	3	Anode CR43		NA	Check CR43
13A	1	Emitter Q41		Check track from emitter Q41 to Pin 36, Check connection between Pin 36 and Test Set.	Go to 13A-2

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

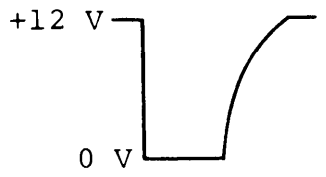
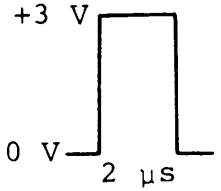
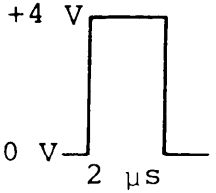
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
13A (Cont)	2	Collector Q39		Check C45, C46, R126	Go to 13A-3
	3	Emitter Q38		Check Q39, C44, R125, C41, R124	Go to 13A-4
	4	Pin 37		Check connections between Pin 37 and Test Set	Check Q38, C40, C41, R122, R123, R124
13B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 13B-2

Table 5-5. Decoder (A2), Fault Isolation Procedure for RT-859/APX-72 (Cont)

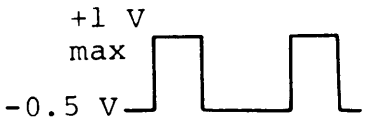
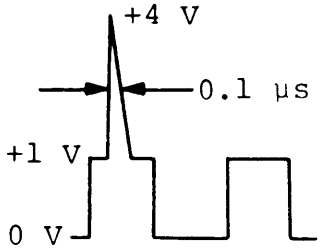
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
13B (Cont)	2	Base Q17	+7.5 V	NA	Check track connection between the base of Q17 and Pin 2
14C	1	Collector Q2		NA	Check C51, CR37, CR36
15C	1	Collector Q9		NA	If the pulse width is greater than 0.2 µs check CR27
16C	1	Collector Q9		NA	Check CR33

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72

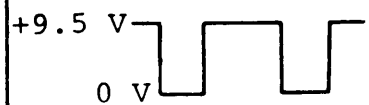
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	Collector Q32		Check for secure connection between buffer assembly A35 and the board under test	Go to 1A-2
	2	Cathode CR39		Check Q32, CR40, CR41, CR42, CR43	If Lamp B is not lighted, proceed to 1A-3. If Lamp B is lighted, proceed to Test Sequence 1B-1.
	3	Collector Q45		Check CR39, CR31, CR32	Go to 1A-4
	4	A2-16		Replace Q45	Check for secure, connection between Decoder Board and Test Set
1B	1	Collector Q24	+0.3 V max	Check connections between TP5 and Q24, TP5 and buffer assembly A35	Go to 1B-2

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1B (Cont)	2	Base Q24	+0.6 V	Check Q24	Replace Q24 if voltage is +6 VDC at base of Q24
1C	1	Rotate Switch to Position 2 and observe Lamp A. If Lamp A lights, proceed to Test Sequence 2A-1. If Lamp A remains off return Switch to Position 1 and proceed to Test Sequence 1C-2.			
	2	Collector Q43	0.3 V max	Check connection between collector of Q43 and TP3; between TP3 and buffer assembly A35	Go to 1C-3
	3	Collector Q42	+6.4 V	Check Q43, R133, R134, R135, R136	Go to 1C-4

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1C (Cont)	4	Junction of CR35, CR36, CR37	-0.3 V	Check Q42, R130, R131	Go to 1C-5
	5	Anode CR35	+0.3 V max	Proceed to 2A-1	Check Q26, R80, R81
2A	1	Anode CR36	-0.6 V	Check connections between CR36 and TP1; between TP1 and buffer assembly A35	Go to 2A-2
	2	Base Q40	+25 V	Check Q40, Q41 R127, R128	Disconnect C43 and observe base of Q40. If voltage level is +25 VDC check C43. If base voltage remains abnormal, check C45.

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A-APX-72 (Cont)

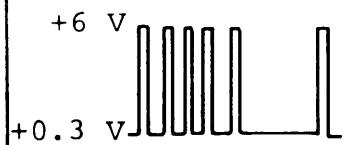
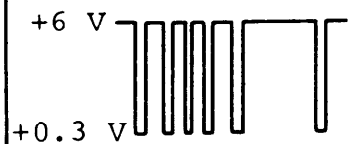
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2B	1	Collector Q33		Check connections between Q33 and TP7; between TP7 and buffer assembly A35	Proceed to 2B-2
	2	Collector Q34		Check Q33, CR25, CR26, CR27, CR28, CR29, C36, R106, R146	Check Q34, CR30, R109, R110, R111, C37
2C	1	Anode CR26	+0.3 V max	Go to 2C-2	Check C2, R5
	2	Anode CR27	+0.3 V max	Go to 2C-3	Check C12, R28
	3	Anode CR28	+0.3 V max	Go to 2C-4	Check C20, R63

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

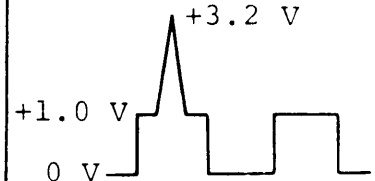
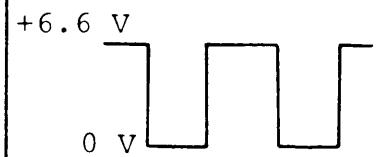
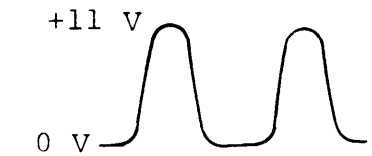
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2C (Cont)	4	Anode CR29	-0.3 V	NA	Check C33, R102
3A	1	Collector Q9	 Temporarily remove buffer to observe true peak. Disregard fault indicators.	Check connections between Q9 and TP4; TP4 and buffer assembly A35	Go to 3A-2
	2	Collector Q8		Check Q9, R27, R29, R30, C13	Go to 3A-3
	3	A2-60		Check Q8, CR4, CR5, R24, R25, R26, C11	Check connections between Pin 60 and Test Set

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

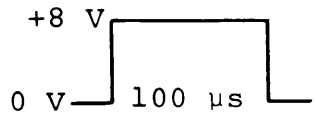
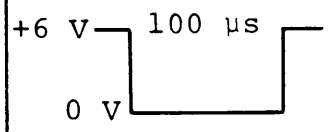
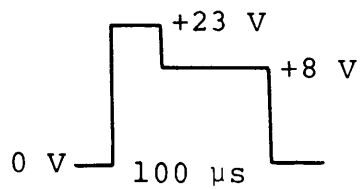
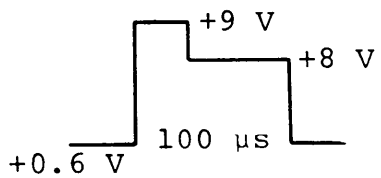
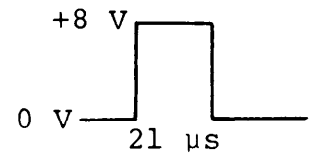
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3B	1	Collector Q43		Check connections between Q43 and TP3 and between TP3 and XA2P1-35	Go to 3B-2
	2	Collector Q42		Check Q43, R133, R134, R135, R136	Go to 3B-3
	3	Cathode CR35		Check Q42, R130, R131	Go to 3B-4
	4	Anode CR35		Check CR35, CR36	Go to 3B-5
	5	A2-31		Check Q25, Q26, CR16, C27, CR36, R78, R79, R80, R81, R75, R76, R77, C6	Check connections between Pin 31 and Test Set

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

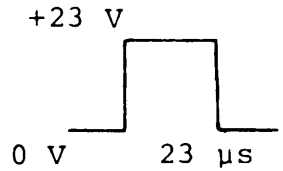
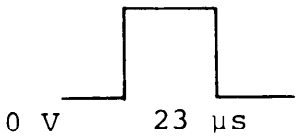
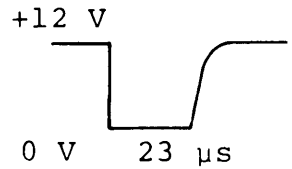
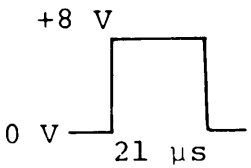
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3C	1	Emitter Q41		Check Connections between TP1 and XA2P1-36	Go to 3C-2
	2	Collector Q40		Check Q41, CR35, CR36, R147, R148, R149, R150, R129	Go to 3C-3
	3	Collector Q37		Check Q40, Q41, C42, C43, R121,, R127	Go to 3C-4
	4	A2-39		Check Q37, R120, R119, R118, C42	Check connection at XA2-39

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A	1	Collector Q17	0 V	Check connections between TP2 and buffer assembly A35	If Indicator 4C is also lighted, go to 4C-1. If Indicator 4C is not lighted, go to 4A-2.
	2	Base Q18	+8 V	Go to 4A-3	Check CR12, Q18, R56, R57, R58
	3	Base Q17	The dc voltage at this point must be equal to or greater than the voltage at the base of Q18.	Check Q17, R55, R54	Go to 4A-4
	4	Collector Q28	+12 V	Go to 4A-5	Go to 4A-7

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	5	Collector Q11	+12 V	Go to 4A-6	Go to 4A-12
	6	Collector Q15	+12 V	Visually inspect board for short circuit between track leading from XA2P1-2 and ground	Go to 4A-17
	7	Base Q29	A dc voltage +0.3 to +10 V depending on setting of R89	Go to 4A-8	Check Q29, CR44, R89, R88, R90, R155
	8	Base Q28	0 V	Check Q28, Q29, R85, R86	Go to 4A-9

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	9	Base Q49	0 V	Check Q49, R154	Go to 4A-10
	10	Collector Q47	+17 V	Check Q27, C28, R83, R84	Go to 4A-11
	11	Collector Q26	+0.3 V max	Check Q47, R15, R16, R17, R13, R14, C6	Check Q26, R81, R80, C27
	12	Base Q12	+4.2 V	Go to 4A-13	Check CR43, Q12, R39, R40, R153
	13	Base Q11	0 V	Check Q11, Q12, R37, R38	Go to 4A-14

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	14	Base Q48	0 V	Check Q48, R152	Go to 4A-15
	15	Collector Q46	+16 V	Check Q10, R35, R36, C15	Go to 4A-16
	16	Base Q46	-1.0 V	Check Q46	Check C5, R8, R9
	17	Base Q16	+2 V to +9 V depending on setting of R51	Go to 4A-18	Check CR10, Q16, R51, R50, R52
	18	Base Q15	0 V	Check Q15, Q16, R48, R47	Go to 4A-19

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A\APX-72 (Cont)

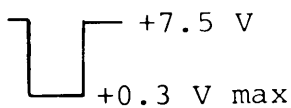
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A	19	Base Q14	0 V	Check Q14, Q15, R46	Go to 4A-20
	20	Emitter	+12.6 V	Go to 4A-21	Check CR7, C17, R43
	21	Base Q13	A dc voltage approximately 1.2 V more positive than the emitter of Q13.	Check Q13, R44, R45, C18	Check C52, C16, R41
4C	1	Collector Q45	 PW=0.4 us	Check CR39	Check Q45, R145, R144, R143, C53 Check connection at XA2-16

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

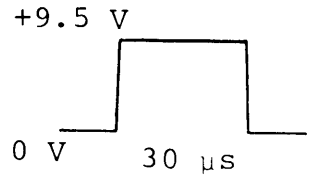
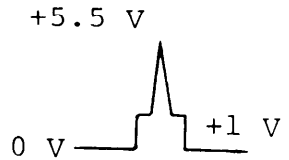
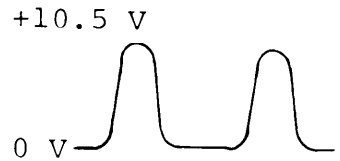
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5A	1	Collector Q24		Check connections between TP5 and buffer A35	Go to 5A-2
	2	Collector Q36		Check Q23, Q24, Q44, CR15, C22, C24, C25, C26, C5, C35, R66, R67, R68, R69, R70, R71, R72, R73, R74	Go to 5A-3
	3	Collector Q35		Check Q36, C39, R115, R116, R117	Go to 5A-4
	4	A2 Pin 25		Check Q35, R112, R113, C38, CR34, C39	Check connections at Pin 25

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 5B-2
	2	Base Q12	+4.5 V	Go to 5B-3	Check CR3, Q12, R39, R40, R153
	3	Anode CR3	+5 V	Disconnect the base of Q12 from track and go to 5B-4	Check R39, R40, R153
	4	Cathode CR3	+4.5 V	Check Q12, Q11	Go to 5B-5
	5	Flat pack A1-Pin 4	0 V	Replace flat pack A1	Check connection between Pin 4 of flat pack A1 and Pin 58 of Decoder board
	6	Base Q11	+4.5 V	Check Q11, Q12, R37, R38, CR8	Go to 5B-7

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

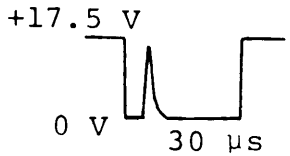
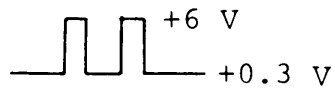
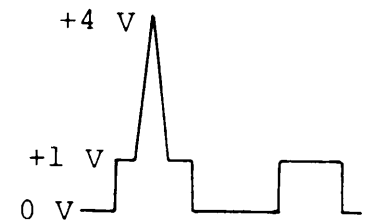
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5B (Cont	7	Base Q48	+5.0 V	Check Q48, Q11, R152	Go to 5B-8
	8	Collector Q46		Check Q10, C15, R35, R36	Check Q46, R8, R9, R10, R11, R12
5C	1	Collector Q9		Check connections between TP5 and XA2P1-57; between XA2P1-57 and the Test Set.	If indicator 5A is also lighted, go to 5A-1 first. If indicator 5A is not lighted go to 5C-2.
	2	TP8		Check CR41	Check CR31
6A	1	Collector Q2		Check connections and interface between Pin 61 and the Test Set	Go to 6A-2

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

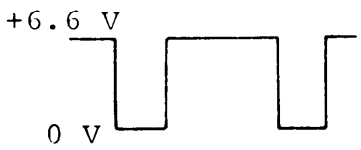
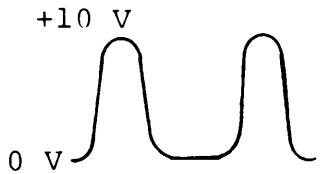
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6A (Cont)	2	Collector Q1		Check Q2, R7, R4, R6, C3	Go to 6A-3
	3	Pin 63 of Decoder Board		Go to 6A-4	Check connections and interface between Pin 61 and the Test Set
	4	Cathode CR1	-1 V	Check CR1, Q1, R1, R2, R3	Check connection and interface between Pin 62 and the Test Set
6B	1	Collector Q17	+8 V	Check connections between the collector of Q17 and TP2. Check interface between buffer A35 and TP2.	If Lamp 6A is also lighted, refer to Test Sequence 6A-1. If Lamp 6A is not lighted go to 6B-2 .

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B (Cont)	2	Base Q29	A dc voltage between +0.3 V and +10 V depending upon adjustment of R89	Take note of the dc voltage at base of Q29 and go to 6B-3	Check R89, CR44, R88, R90
	3	Base Q28	A dc voltage more positive than the voltage at base of Q29	Check Q28, R86, CR11	If the voltage at the base of Q28 is greater than +1 VDC go to 6B-4 If the voltage at the base of Q28 is less than +1 VDC go to 6B-5
	4	Monitor the base of Q29 and simultaneously turn the R89 ADJ control (located on buffer A35) in a counter-clockwise direction. Turn until the voltage at the base of Q29 is less positive than the voltage at the base of Q28. At this point, indicator 6B should turn off. NOTE: Do not adjust R89 any further than required to turn off 6B. If the voltage at the base of Q29 does not vary as R89 is adjusted, check R89, CR44, R88. If the voltage at the base of Q29 can be adjusted to a value less positive than the voltage at the base of Q28, but indicator 6B does not turn off check Q28, Q29, CR11, R85, R86.			

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A-APX-72 (Cont)

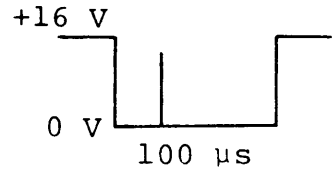
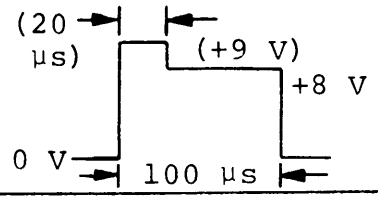
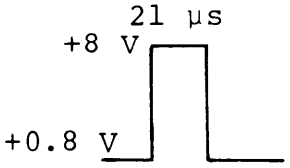
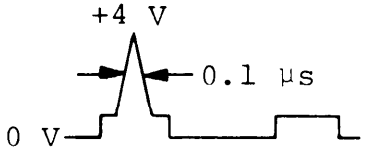
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B (Cont)	5	Base Q49	A dc voltage more positive than the voltage at the base of Q29	Check Q49, R154	Go to 6B-6
	6	Collector Q47		Check Q27, C28, R83, R84	Go to 6B-7
	7	Collector Q26		Check Q47, R13, R14, R15	Go to 6B-8
	8	Pin 31 of Decoder Board		Check Q25, Q26, C27, CR16, R76, R77, R78, R80, R81, CR36, CR37	Check connection between Pin 31 of the Decoder board and the Test Set
6C	1	Collector Q2			If pulse is wider than 0.2 µs check CR26

Table 5-6. Decoder (A2), Fault Isolation procedure for RT-859A/APX-72 (Cont)

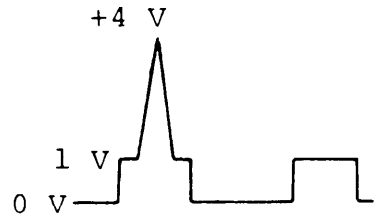
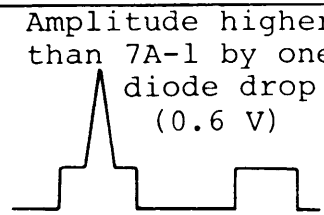
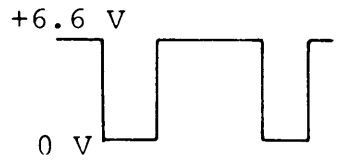
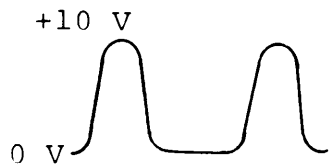
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A	1	Cathode CR21		Check track connection between cathode CR21 and Pin 15. Check connection between Pin 15 and the Test Set.	Go go 7A-2
	2	Collector Q22		Check CR21	Go to 7A-3
	3	Collector Q21		Check Q22, CR24, R94, R96, R97	Go to 7A-4
	4	Pin 50		Go to 7A-5	Check connections between Pin 50 of Decoder and the Test Set. Check C29.

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A\APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A (Cont)	5	Cathode CR19	- 1 V	Check CR19, Q21 R93, CR20, R91, R92	Check track between cathode CR19 and Pin 47 of Decoder Board. Check connection between Pin 47 and the Test Set.
7B	1	Collector Q17	+8	Check connection between TP2 and buffer A35	If Indicators 7A and 7C are both lighted refer to Test Sequence 7A-1 before proceeding with 7B-1. If Indicator 7C is lighted, refer to Test Sequence 7C-1 before proceeding with 7B-1. If Indicator 7B is the only lighted indicator, go to 7B-2.
	2	Base Q16	A dc voltage between +2 V and +9 V, depending upon adjustment of R51	Take note of the dc voltage at the base of Q16 and go to 7B-3	Check R51, CR10, R50, R52
	3	Base Q15	A dc voltage more positive than the voltage at the base of Q16	Check Q15, CR9, R48	If the voltage at the base of Q15 is greater than +2.0 VDC go to 7B-4. If the voltage at the base of Q15 is less than +2.0 VDC, go to 7B-5.

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

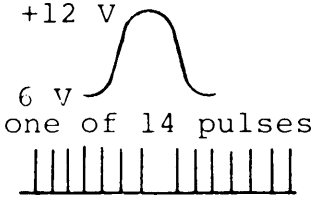
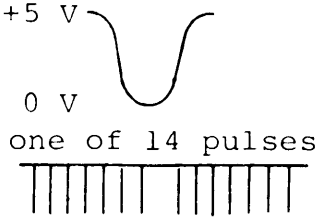
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7B (Cont)	4	Monitor the base of Q16 and simultaneously turn the R51 Adj. control (located on buffer A35) in a counter-clockwise direction. Turn until the voltage at the base of Q16 is less positive than the voltage at the base of Q15. At this point, indicator 7B should turn off. If the voltage at the base of Q16 does not vary as R51 is adjusted, check R51, CR10, R50. If the voltage at the base of Q16 can be adjusted to a value less positive than the voltage at the base of Q15 but Indicator 7B does not turn off, check Q15, Q16, R47.			
	5	Base Q14	A dc voltage 2.6 V or larger	Check Q14, R46	Go to 7B-6
	6	Collector Q13		Check C18, R44, R45, Q14	Go to 7B-7
	7	A2 Pin 33		Check Q13, CR7, C17, C16, R141, R41, R42, R43	Check VR1, C52 Check connection between Pin 33 of Decoder Board and Test Set

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

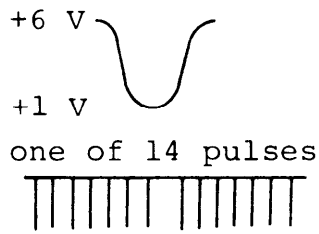
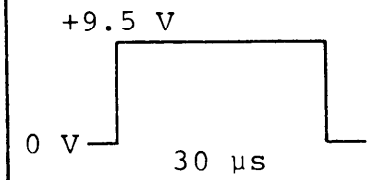
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7C	1	A2 Pin 32		Check connection between Pin 32 and the Test Set	Check C52, VR1, R142
8A	1	Collector Q17	0 V	Check connection between TP2 and buffer A35	Go to 8A-2
	2	Base Q12	+4.2 V	Go to 8A-3	Check CR3, R39, R40, R153
	3	Base Q11	A dc voltage less than +4.5 V	Check Q11, Q12, R37, R38	If pulses appear at the base of Q11 check C15, R35, R36
9A	1	Collector Q24		Check connection between TP5 and buffer A35	Go to 9A-2

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

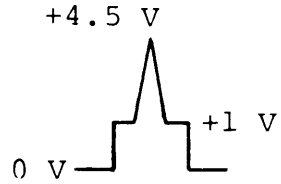
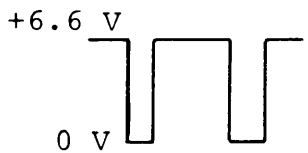
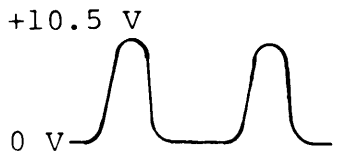
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A (Cont)	2	Collector Q36		Check Q23, Q24, Q45, CR15, C22, C24, C25, C26, C5, C35, R66, R67, R68, R69, R70, R71, R72, R73, R74	Go to 9A-3
	3	Collector Q35		Check Q36, C39, R115, R116, R117	Go to 9A-4
	4	A2 Pin 25		Check Q35, R112, R113, C38, CR34, C39	Check connections at Pin 25
9B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 9B-2

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9B (Cont)	2	Base Q12	+4.5 V	Go to 9B-6	Check CR3, Q12, R39, R40, R153
	3	Anode CR3	+5 V	Disconnect the base of Q12 from track and go to 9B-4	Check R39, R40, R153
	4	Cathode CR3	+4.5 V	Check Q12, Q11	Go to 9B-5
	5	Flat pack A1-Pin 1	0 V	Replace flat pack A1	Check connection between Pin 1 of flat pack A1 and Pin 47 of Decoder board
	6	Base Q11	+4.5 V	Check Q11, Q12, R37, R38, CR8	Go to 9B-7
	7	Base Q48	+5 V	Check Q48, Q11, R152	Go to 9B-8

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

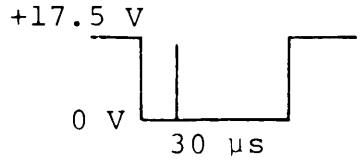
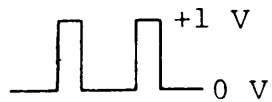
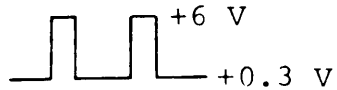
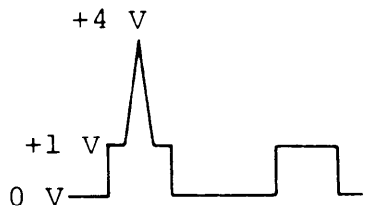
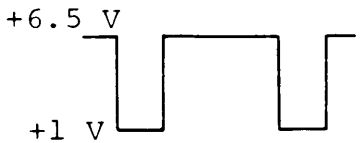
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9B (Cont)	8	Collector Q46		Check Q10, C15, R35, R36	Check Q46, R8, R9, R10, R11, R12
9C	1	Collector Q22		Check connections between XA2P1-15 and the collector of Q22	If indicator 9A is also lighted, go to 9A-1 first. If indicator 9A is not lighted go to 9C-2.
	2	TP8		Check CR43	Check CR31
10B	1	Collector Q20		Check track between collector Q20 and Pin 20 Check connection between Pin 20 and the Test Set	Go to 10B-2
	2	Collector Q19		Check Q9, R30, R27, R29	Go to 10B-3

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

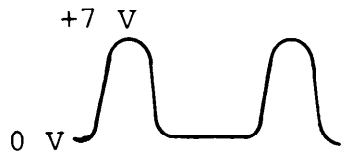
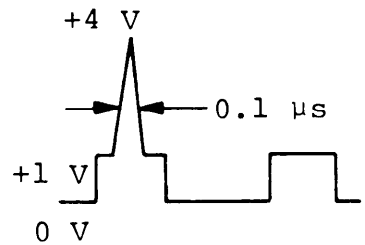
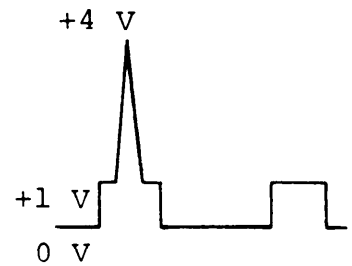
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10B (Cont)	3	Pin 21 of Decoder Board		Go to 10B-4	Check C19 Check connections between Pin 21 of Decoder and the Test Set
	4	Cathode CR13	- 1 V	Check CR13, Q19, CR14, C21, R59, R60, R61	Check connection between Pin 54 and the Test Set
10C	1	Collector Q20		NA	For a pulse wider than 0.2 µs check CR28
11A	1	Cathode CR24		Check track connection between cathode CR24 and Pin 15. Check connection between Pin 15 and the Test Set	Go to 11A-2

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

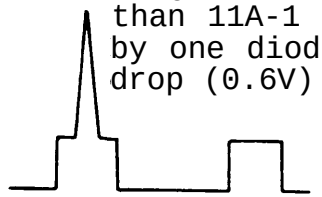
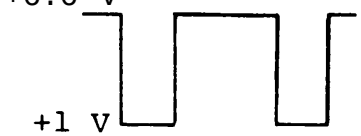
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11A Cont)	2	Collector Q31	Amplitude higher than 11A-1 by one diode drop (0.6V) 	Check CR24	Go to 11A-3
	3	Collector Q30	+6.6 V +1 V 	Check Q31, CR21, R101, R103, R104	Go to 11A-4
	4	Pin 43	+10 V 0 V 	Go to 11A-5	Check C32 Check connection between Pin 43 of Decoder and the Test Set
	5	Cathode	-1 V	Check CR22, Q30, CR23, R98, R99, R100	Check track between cathode CR22 and Pin 41 of Decoder Board Check connections between Pin 41 and the Test Set

Table 5-6. Decoder (A2), Fault. Isolation Procedure for RT-859A/APX-72 (Cont)

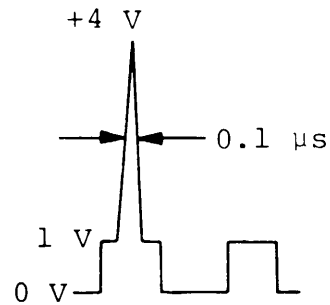
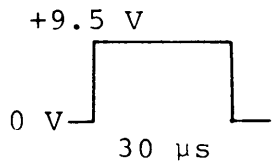
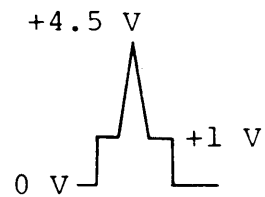
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11C	1	Anode CR29		NA	For a pulse wider than 0.2 µs, check CR29
12A	1	Collector Q24		Check connection between TP5 and buffer A35	Go to 12A-2
	2	Collector Q36		Check Q23, Q24, Q44, CR15, C22, C24, C25, C26, C5, C35, R66, R67, R68, R69, R70, R71, R72, R73, R74	Go to 12A-3

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

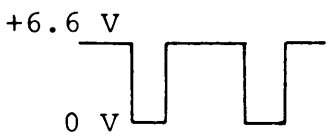
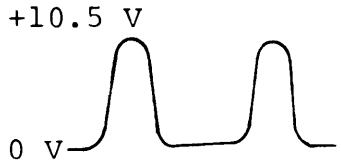
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12A	3	Collector Q35		Check Q36, C39, R115, R116, R117	Go to 12A-4
	4	A2 Pin 25		Check Q35, R112, R113, C38, CR34, C39	Check connections at Pin 25
12B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 12B-2
	2	Base Q12	+4.5 V	Go to 12B-3	Check CR3, Q12, R39, R40, R153
	3	Anode CR3	+5 V	Disconnect the base of Q12 from track and go to 12B-4	Check R39, R40, R153

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cent)

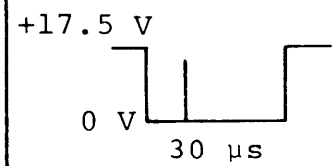
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12B (Cont)	4	Cathode CR3	+4.5 V	Check Q12, Q11	Go to 12B-5
	5	Flat pack A1-Pin 4	0 V	Replace flat pack A1	Check connection between Pin 2 of flat pack A1 and Pin 54 of Decoder board
	6	Base Q11	+4.5 V	Check Q11, Q12, R37, R38, CR8	Go to 12B-7
	7	Base Q48	+5.0 V	Check Q48, Q11, R152	Go to 12B-8
	8	Collector Q46		Check Q10, C15, R35, R36	Check Q46, R8, R9, R10, R11, R12

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

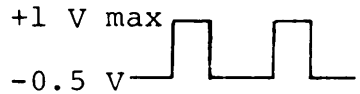
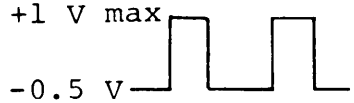
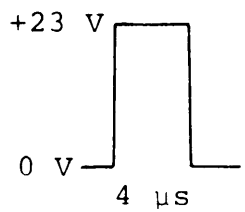
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12C	1	Anode CR40	0 V (base line)	Go to 12C-2	Check CR40
	2	Anode CR42	+1 V max -0.5 V 	Go to 12C-3	Check CR42
	3	Anode CR43	+1 V max -0.5 V 	NA	Check CR43
13A	1	Emitter Q41	+23 V 0 V 4 µs 	Check track from emitter Q41 to Pin 36. Check connection between Pin 36 and Test Set	Go to 13A-2

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APx-72 (Cont)

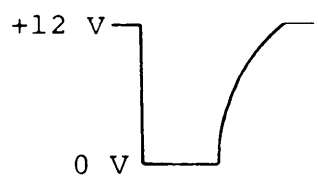
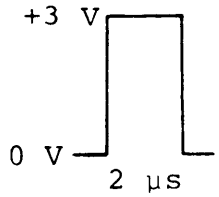
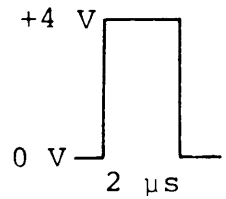
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
13A (Cont)	2	Collector Q39		Check C45, C46, R126	Go to 13A-3
	3	Emitter Q38		Check Q39, C44, R125, C41, R124	Go to 13A-4
	4	Pin 37		Check connections between Pin 37 and Test Set	Check Q38, C40, C41, R122, R123, R124
13B	1	Collector Q17	+8 V	Check connection between TP2 and buffer A35	Go to 13B-2

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A\APX-72 (Cont)

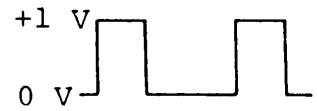
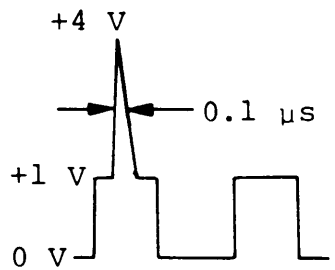
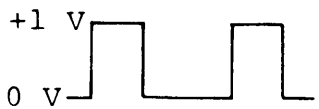
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
13B (Cont)	2	Base Q17	+8.5 V	NA	Check track connection between the base of Q17 and Pin 2
14C	1	Collector Q2		NA	Check C51, CR37, CR36
15C	1	Collector Q9		NA	If the pulse width is greater than 0.2 µs check CR27
16C	1	Collector Q9		NA	Check CR33

Table 5-6. Decoder (A2), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
17A	1	Anode CR3	A dc voltage more positive than +4.5 V	NA	Check connections between flat-pack A1 and the Decoder board. If connections are good, replace flat-pack A1.

NOTE

The delay line is a non-repairable board and no troubleshooting is normally performed. However, since a test switch is part of the AN/APM-338, these tables are included. An extender board for the delay line is not a part of the equipment and for this reason alternate test points are included so that the waveforms may be observed using extenders for the alternate boards. Such observation may be required when troubleshooting the test set.

Table 5-7. Delay Line (DL1), Fault Isolation Procedure

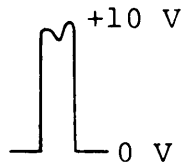
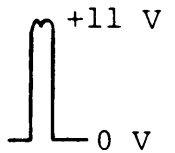
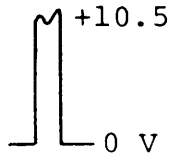
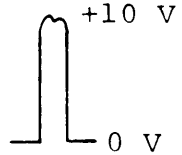
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	DL1-1 XA1-B		Check connection at XDL1-1	Replace DL1
2B	1	DL1-6 XA1-E		Check connection at XDL1-6	Replace DL1
	2	DL1-3 XA1-7		Check connection at XDL1-3	Replace DL1
	NOTE: Do not perform this test with an RT-859A/APX-72 processor (A1) card installed in the reference card slot.				
3A	1	DL1-10 XA2-63		Check connection at XDL1-10	Replace DL1

Table 5-7. Delay Line (DL1), Fault Isolation Procedure (Cont)

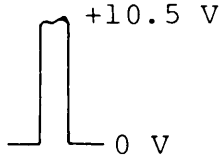
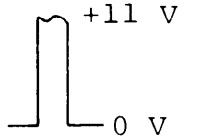
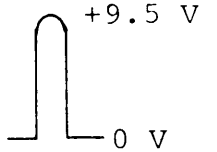
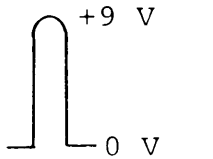
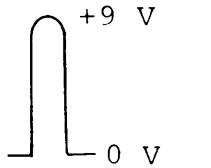
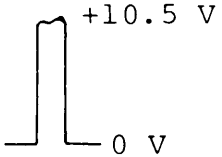
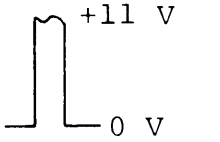
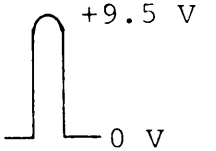
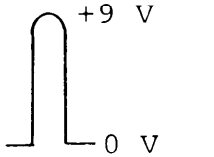
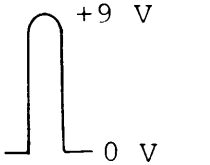
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9C	1	DL1-7 XA2-16		Check connection at XDL1-7	Replace DL1
10A	1	DL1-9 XA2-25		Check connection at XDL1-9	Replace DL1
	2	DL1-11 XA3-S		Check connection at XDL1-11	Replace DL1
	3	DL1-13 XA3-T		Check connection at XDL1-13	Replace DL1
	4	DL1-15 XA2-50		Check connection at XDL1-15	Replace DL1

Table 5-7. Delay Line (DL1), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9C	1	DL1-7 XA2-16		Check connection at XDL1-7	Replace DL1
10A	1	DL1-9 XA2-25		Check connection at XDL1-9	Replace DL1
	2	DL1-11 XA3-S		Check connection at XDL1-11	Replace DL1
	3	DL1-13 XA3-T		Check connection at XDL1-13	Replace DL1
	4	DL1-15 XA2-50		Check connection at XDL1-15	Replace DL1

NOTES FOR TABLE 5-8

MODE 4 (A3), FAULT ISOLATION PROCEDURE FOR RT-859/APX-72

NOTE 1: Whenever this procedure indicates the replacement of integrated circuit, first check that the dc power and ground connections are good. (Refer to schematic for pin numbers.)

NOTE 2: When it is suspected that an abnormal waveform could be caused by an integrated circuit having developed an input short, thereby loading the circuit being viewed, lift the input pin of the integrated circuit. If normal waveform is restored, replace the defective integrated circuit.

CAUTI0N

Integrated circuits can be damaged electrically if the soldering iron tip is not at ground potential.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

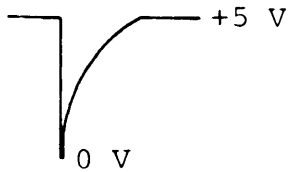
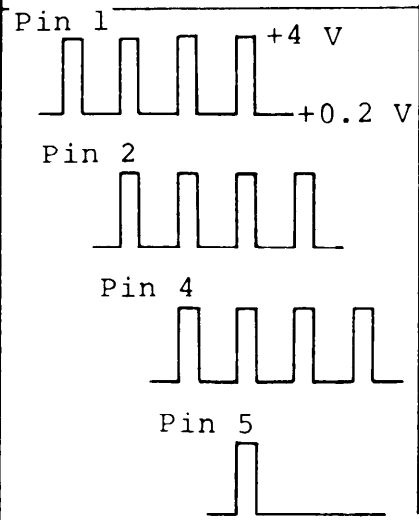
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	A3A3 Pin 6		If lamps B and C are not lighted, go to 2A-1. If lamps B and C are lighted, check connection between buffer A36 and TP7.	Lift A3A3 Pin 6 and attach test probe to lifted pin. If waveform is still abnormal, go to 1A-2. If normal waveform is restored, reconnect Pin 6 and lift A3A4 Pin 3, A3A6 Pin 1, and A3A15 Pin 1, each in turn. If lifting a lead restores normal waveform, replace the particular IC. If otherwise, go to 1A-2.
	2	A3A3 Pins 1, 2, 4, 5		Check, replace A3A3	Go to 1A-3

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cent)

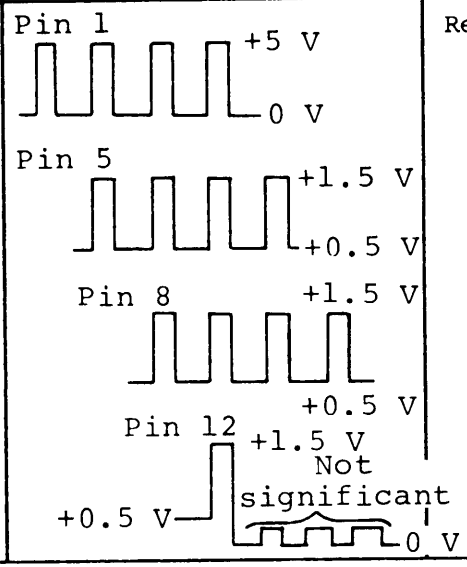
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A (Cont)	3	A3A2 Pins 3, 6, 8, 11	Same as 1A-2	Check track and connections between A3A3 and A3A2	Go to 1A-4
	4	A3A2 Pins 1, 5, 10, 13	Inverse of 1A-2	Replace A3A2	Go to 1A-5
	5	A3A1, Pins 3, 7, 11, 14	Same as 1A4	Check track and connections between A3A2 and A3A1	Go to 1A-6
	6	A3A1, Pins 1, 5, 8, 12, 9, 13		Replace A3A1	Abnormal waveform at: Pin 1. Check Pin Z for normal input to board then check R1, R2, C1, C22. Replace A3A1. Pin 5. Check Pin U for normal input to board then check R3, R4, C2. Replace A3A1. Pin 8. Check Pin S for normal input to board then check R5, R6, C3. Replace A3A1.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

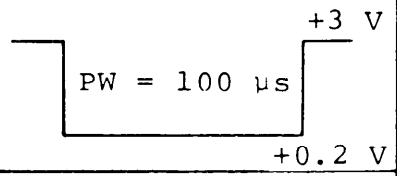
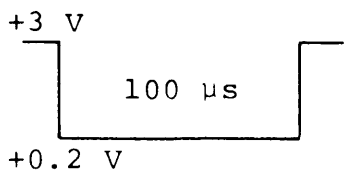
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A Step 6 (Cont)			Pin 9 +4 V		Pin 12. Check Pin T for normal input to board then check R7, R8, C4. Replace A3A1.
			Pin 13  		Pin 9. Go to 1A-7. Pin 13. Go to 1A-9.
	7	A3A3 Pin 8	+4.5 V	Check track from A3A3 Pin 8 to A3A1 Pin 9. Replace A3A1.	Go to 1A-8
	8	A3A3 Pin 9	+0.2 V	Replace A3A3	Check connection at XA3-18. Check track from Pin 9 A3A3 to A3 Pin 18.
	9	Collector Q1	 	Check track from collector Q1 to A3A1 Pin 13. Replace A3A1.	Go to 1C-2

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

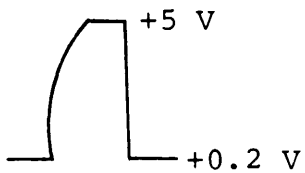
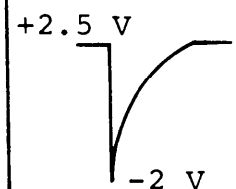
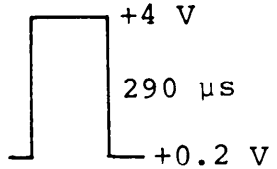
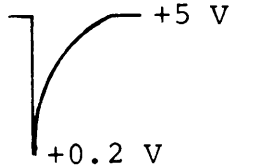
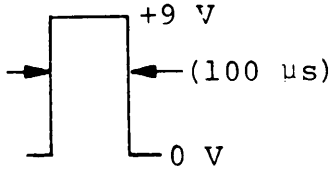
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1B	1	A3A5 Pin 8		Check connection between buffer A36 and TP8	If lamps A and C are lighted go to 1A-1. If lamps A and C are not lighted go to 1B-2.
	2	A3A5 Pin 9		Check, Replace A3A5	Go to 1B-3
	3	A3A4 Pin 6		Check R99, R110, C11	Go to 1B-4
	4	A3A4 Pin 3		Check, Replace A3A4	NA
1C	1	Collector Q2		Check connection to XA3-J	Go to 1C-2

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

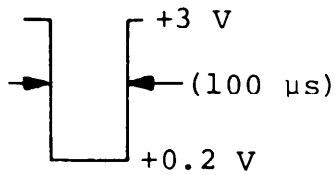
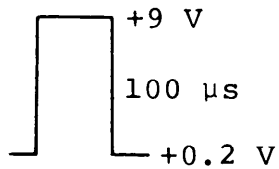
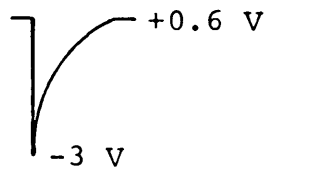
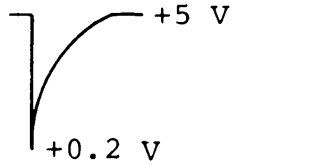
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1C (Cont)	2	Collector Q1		Check Q2, R16, R107	Go to 1C-3
	3	A3A6 Pin 11	+4 V	Go to IC-4	Go to 1C-7
	4	Collector Q34		Check CR2, Q1, R10, R11, R12, R13, R14, R15	Go to 1C-5
	5	Base Q34		Check Q34, Q33, R105, R104, R103, R102, R101, R100, CR14, C6	Go to 1C-6
	6	A3A3 Pin 6		Check CR13, R20, C5	NA

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

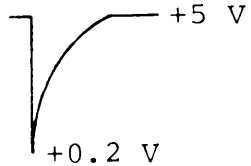
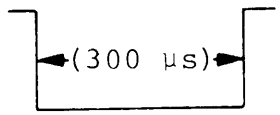
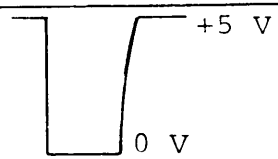
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1C (Cont)	7	A3A6 Pin 1		Go to IC-8	Check track to A3A3 Pin 6
	8	A3A6 Pin 4		Go to 1A-9	Check track to A3A4 Pin 1
	9	A3A6 Pin 5	+4 V	Check, Replace A3A6	Go to 1C-10
	10	A3A5 Pin 6	+4 V	Check track to A3A6 Pin 5	Go to 1C-11
	11	A3A5 Pin 5	0 V	Check, Replace A3A5	Check R35, C13
1D	1	A3A7 Pin 8		Check connection at TP2	Go to 1D-2

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

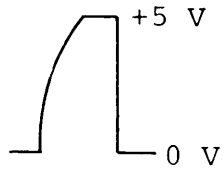
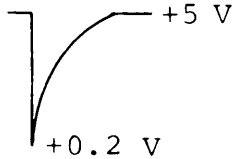
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1D (Cont)	2	A3A7 Pin 9		Go to ID-3	Check track connections to A3A5 Pin 8
	3	A3A7 Pin 11	+2.6 V min	Go to ID-4	Check track connection to A3A6 Pin 11
	4	A3A7 Pin 10	+2.6 V min	Check, Replace A3A7	Go to 1D-5
	5	A3A15 Pin 11	+2.6 V min	Check track to A3A7 Pin 10	Go to 1D-6
	6	A3A15 Pin 1		Check, Replace A3A15	Check track to A3A13 Pin 6
2A	1	A3A3 Pin 6	+5 V No pulse present	Check connection between buffer A36 and TP7	Pulse present - go to 2A-2

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

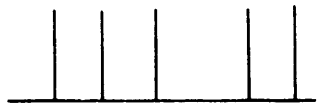
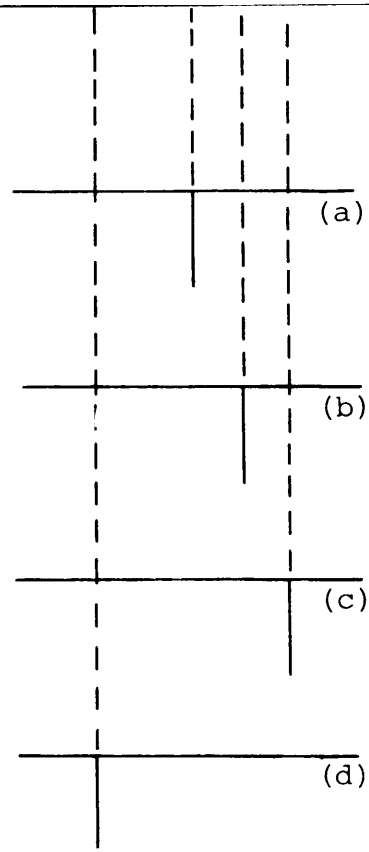
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	2	A3-Z		Waveform to be used for timing reference in following steps	Check connection at XA3-Z
		A3A3 Pin 6			Determine the pulse condition. If condition (a), go to 2A-3 If condition (b), go to 2A-9 If condition (c), go to 2A-16 If condition (d), go to 2A-23
	3	A3A3 Pin 1	5 positive pulses	Replace A3A3	Go to 2A-4

Table 5-8. Mode 4 (A3) Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	4	A3A2 Pin 3	5 positive pulses	Check track and connections, A3A3, pin 1 to pin 2	Go to 2A-5
	5	A3A2 Pin 1	5 negative pulses	Replace A3A2	Go to 2A-6
	6	A3A1 Pin 3	5 negative pulses	Check track and connections, A3A2 pin 1 to A3A1 pin 3.	Go to 2A-7
	7	A3A1 Pin 1	5 positive pulses	Replace A3A1	Go to 2A-8
	8	A3-Z	5 positive pulses	Check C1, R1, R2	NA
	9	A3-U	5 positive pulses	Go to 2A-10	Check connection at XA3-U

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	10	A3A3 Pin 2	5 positive pulses	Replace A3A3	Go to 2A-11
	11	A3A2 Pin 6	5 positive pulses	Check track and connections. A3A3 pin 2 to A3A2 pin 6	Go to 2A-12
	12	A3A2 Pin 5	5 negative pulses	Replace A3A2	Go to 2A-13
	13	A3A1 Pin 7	5 negative pulses	Check track and connections A3A2 pin 5 to A3A1 Pin 7	Go to 2A-14
	14	A3A1 Pin 5	5 positive pulses	Replace A3A1	Go to 2A-15
	15	A3-U	5 positive pulses	Check R3, R4, C2	NA

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	16	A3-S	5 positive pulses	Go to 2A-17	Check connection at XA3-S
	17	A3A3 Pin 4	5 positive pulses	Replace A3A3	Go to 2A-18
	18	A3A2 Pin 8	5 positive pulses	Check track and connections, A3A3 pin 4 to A3A2 pin 8	Go to 2A-19
	19	A3A2 Pin 10	5 negative pulses	Replace A3A2	Go to 2A-20
	20	A3A1 Pin 11	5 negative pulses	Check track and connections, A3A2 pin 10 to A3A1 pin 11	Go to 2A-21
	21	A3A1 Pin 8	5 positive pulses	Replace A3A1	Go to 2A-22

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	22	A3-S	5 positive pulses	Check R5, R6, C3	NA
	23	A3-T	5 positive pulses	Go to 2A-24	Check connection at XA3-T
	24	A3A3 Pin 5	5 positive pulses	Replace A3A3	Go to 2A-25
	25	A3A2 Pin 11	5 positive pulses	Check track and connections, A3A3 pin 5 to A3A2 pin 11	Go to 2A-26
	26	A3A2 Pin 13	5 negative pulses	Replace A3A2	Go to 2A-27
	27	A3A1 Pin 14	5 negative pulses	Check track and connections, A3A2 pin 13 to A3A1 pin 14	Go to 2A-28

Table 5-8. Mode 4 (243), Fault Isolation Procedure for RT-859/APX-72 (Cont)

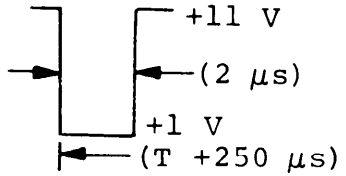
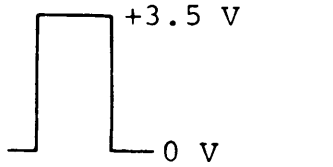
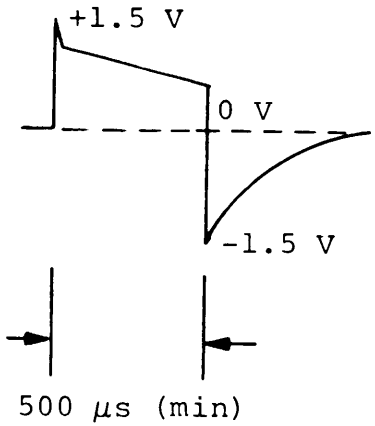
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	28	A3A1 Pin 12	5 positive pulses	Replace A3A1	Go to 2A-29
	29	A3-T	5 positive pulses	Check R7, R8, C4	NA
2B	1	Collector Q35		Check connection at XA3-L. Check CR6.	Go to 2B-2
	2	A3-K		Check Q35, CR17, R36, R38, R37, R39, C14, C15	Check connection at XA3-K
2C	1	A3-1		Check connection at XA3-1	1) If amplitude is less than 3 V p-p adjust R89 for maximum signal amplitude. 2) If pos. pulse width is shorter than 500 μs, go to 2C-2. 3) If no pulse is present or pulse amplitude is less than 3 V p-p go to 2C-3.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

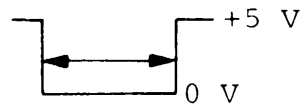
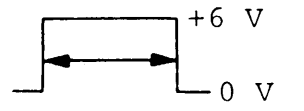
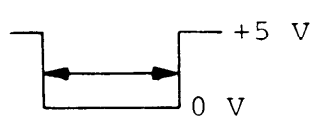
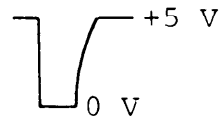
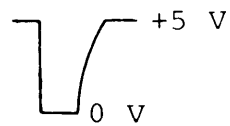
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2C (Cont)	2	A3A8		Check C32, T1, R89, C34	Check C17, R67, R109. Replace A3A8.
	3	Collector Q20		Check Q21, Q22, R83, R84, R85, R86, R87, R88	If collector Q20 is +7 VDC, go to 2C-5. If collector Q20 is 0 VDC, go to 2C-4.
	4	Junction C25, R62	+0.3 V max	Check Q19, R64	Check L2. Check connection at XA3-P.
	5	A3A8 Pin 1		Check Q20, CR8, R80, R81, R82	Go to 2C-6
	6	A3A8 Pin 4		Check, Replace A3A8	Check track to A3A12 Pin 1
2D	1	A3A12 Pin 1		Check connection between buffer A36 and TP4	Go to 2D-2

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

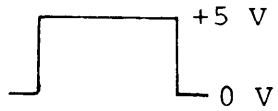
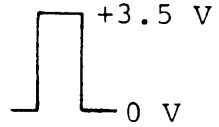
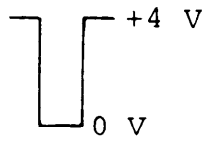
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2D (Cont)	2	A3A12 Pin 4		Go to 2D-3	Go to 2D-4
	3	A3A12 Pin 3		Check, Replace A3A12	Check track to R38
	4	A3A5 Pin 2		Check, Replace A5	Check track to A3 Pin 12. Check connection at XA3-12.
3A	1	A3A3 Pin 6	+5 V No pulses present	Check connection between buffer A36 and TP7	Go to 3A-2
	2	A3A1 Pin 9	0 V	Check, Replace A3A1	Go to 3A-3
	3	A3A3 Pin 8	0 V	Check track to A3A1 Pin 9	Go to 3A-4

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A (Cont)	4	A3A3 Pin 9	+2 V	Check, Replace A3A3	Check connection at A3-18
3B	1	Collector Q35	+11 V No pulses present	Check connection at A3-L	Go to 3B-2
	2	A3-N	+5 V	Check track from CR17 anode to emitter of Q35 for short	Check connection at XA3-N
3C	1	A3-R	+12 V	Check connection at XA3-R	Go to 3C-2
	2	Collector Q6	+12 V	Check track from ANODE side of CR4 to Pin R for shorts	Go to 3C-3
	3	Collector Q4	+0.3 V max	Check Q7, Q6, Q5, CR5, R27, R20	Check Q3, Q4, R21, R20, R19

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

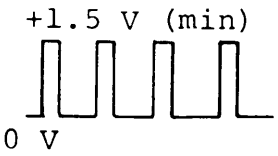
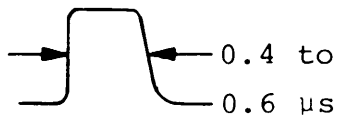
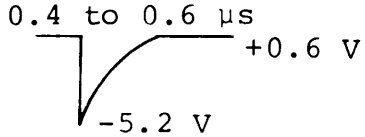
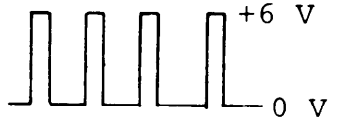
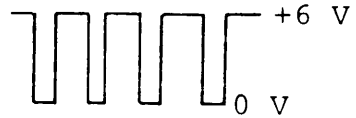
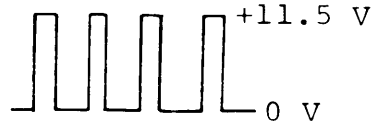
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3D	1	A3-V		Go to 3D-2	Go to 3D-4
	2	A3-V		Check connections at XA3-V	Go to 3D-3
	3	Base Q17		If Tf (step 3D-2) is greater than .2 µs, check R61	If the P.W. is narrow replace Q17. Replace R58, C23. Check R60, C24.
	4	Collector Q17		Check Q18	Go to 3D-5
	5	Collector Q16		Check Q17, R59, R58, C23	Go to 3D-6
	6	A3-Z		Check Q16, R57, R56, CR7, R55, C22	Check connection at XA3-Z

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

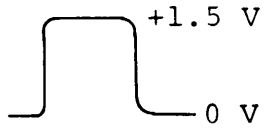
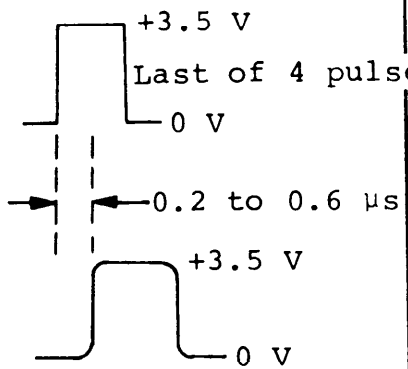
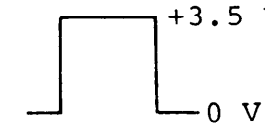
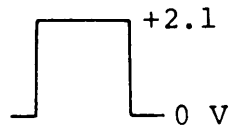
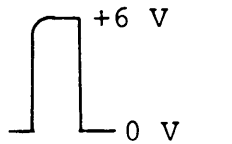
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A	1	A3-20		Go to 9A-2	Go to 4A-4
	2	A3-V A3-20		Go to 4A-3	Replace Q8, C7, R30
	3	A3-20		Check connection at XA3-20	Replace Q9, C9, R32, R34
	4	Collector Q9		Check Q10	Go to 4A-5
	5	Collector Q8		Check Q9, R33, R31, R32, C9	Go to 4A-6

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

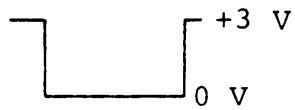
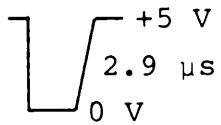
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	6	Collector Q1		Check Q8, CR16, R31, R30, R108, C7	NA
4B	1	A3A12 Pin 1	+5 V	Check connection at TP4	Go to 4B-2
	2	A3A12 Pin 4	+0.2 V	Replace A3A12	Go to 4B-3
	3	A3-12	+5 V	NA	Check connection at XA3-12
4C	1	A3A8 Pin 3		Check, Replace A3A8	Check track to A3A7 Pin 8
4D	1	Collector Q15	+0.2 V	Check connection between buffer A36 and TP3. Check connection at XA3-3.	Go to 4D-2

Table 5-8. Mode 4 (A3), Fault Isolation procedure for RT-859/APX-72 (Cont)

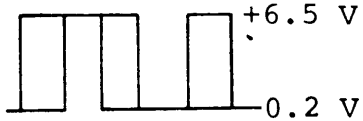
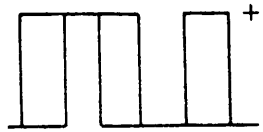
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4D (Cont)	2	Collector Q14	+11 V	Check Q15, R52	Go to 4D-3
	3	Collector Q12	+0.3 V max	Check Q13, Q14	Go to 4D-4
	4	Collector Q11		Check Q12, R47	Go to 4D-5
	5	A3A7 Pin 6		Check Q11, CR12, R43, R44, R45, R46	Go to 4D-6
	6a	A3A7 Pin 5		Go to 4D-6b	Go to 4D-7
	6b	A3A7 Pin 3		Go to 4D-6c	Go to 4D-10

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

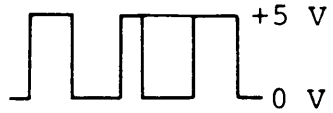
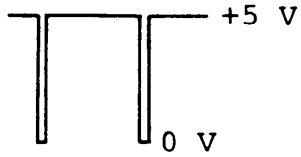
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4D (Cont)	6c	A3A7 Pin 4		Check, Replace A3A7	Go to 4D-16
	7	A3A9 Pin 10, 11	Same as 4D-6a	Check track to A3A7, Pin 5	Go to 4D-8
	8	A3A9 Pin 5, 6		Lift Pins 3, 4. Return to 4D-7 if still abnormal. Go to 4D-9. If normal replace A3A11.	Check track to A3A7 Pin 8
	9	A3A9 Pin 1		Check, Replace A3A9	Go to 4D-14
	10	A3A11 Pin 10, 11	Same as 4D-6b	Check track to A3A7 Pin 3	Go to 4D-11
	11	A3A11 Pin 5, 6	Same as 4D-6a	Go to 4D-13	Go to 4D-12

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

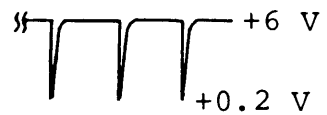
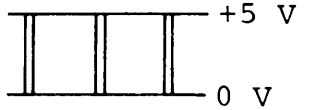
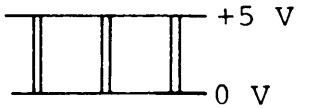
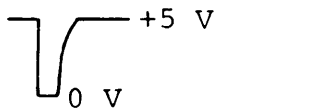
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4D (Cont)	12	A3A9 Pin 3, 4	Same as 4D-6a	Check track to A3A11 Pin 5, 6	Go to 4D-7
	13	A3A11 Pin 1		Check, Replace A3A11	Go to 4D-14
	14	Collector Q32		Check track to A3A9 Pin 1 and A3A11, Pin 1	Go to 4D-15
	15	A3A10 Pin 1	 Positive going pulses	Check Q32, R30 R41, C20	Go to 4D-16
	16	A3A10 Pin 6	 Negative going pulses	Check track to A3A7 Pin 4	Go to 4D-17
	17	A3A10 Pin 3		Check, Replace A3A10	Check track to A3A7 Pin 8

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

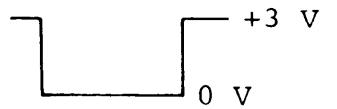
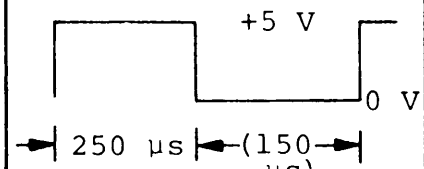
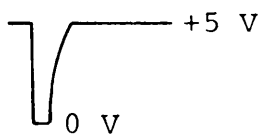
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5A	1	A3A1 Pin 13		Replace A3A1	Check track to Collector Q1
5B	1	A3TP2	+5 V	Check connection at TP2	Go to 5B-2
	2	A3A15 Pin 11		Check track to A3A7 Pin 10. Replace A3A7.	Go to 5B-3
	3	A3A15 Pin 5		Lift Pin 8 of A3A7. If lamp stays on, go to 11B-2. If lamp B goes out, replace A3A15.	Check track to A3A12
5C	1	A3-R	+5.5 V to +12 V	1) Adjust R29 CCW until the voltage is = 8 V; Lamp C will turn off. 2) Check connection at XA3-R. 3) Go to 5C-2. Leave R20 C.W. (25 turns)	Check for short along track from Q6 collector to A3 Pin R

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

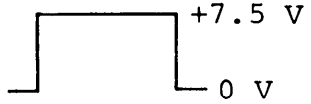
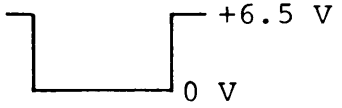
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5C (Cont	2	Collector Q6	+7 V	Replace CR4	Go to 5C-3
	3	Collector Q4		Check CR3, Q5, Q6, R26, R25, R27, R29	Go to 5C-4
	4	Collector Q3		Check Q4, CR3, C12, R23, R22	Check Q3, R19, R20, R21, R18, R17
5D	1	A3-D	+12 V	Check connection between buffer A36 and TP5. Check connection at XA3-D.	Go to 5D-2
	2	Collector Q29	+0.3 V max	Check Q30, R95	Go to 5D-3
	3	Collector Q28	+11 V	Check Q29, R93	Go to 5D-4

Table 5-8, Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

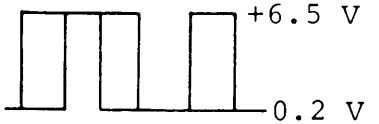
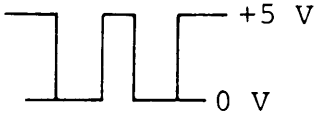
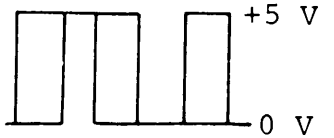
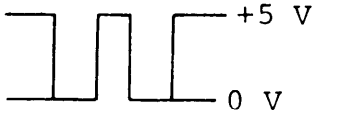
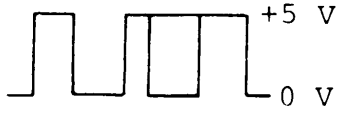
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5D (Cont)	4	Collector Q26	+0.3 V max	Check Q27, Q28 for C-E short	Go to 5D-5
	5	Collector Q25		Check Q26, R75	Go to 5D-6
	6	A3A7 Pin 12		Check Q25, CR11 R74, R73, R72, R97	Go to 5D-7
	7a	A3A7 Pin 13		Go to 5D-7b	Go to 5D-8
	7b	A3A7 Pin 1		Go to 5D-7c	Go to 5D-11
	7c	A3A7 Pin 2		Check, Replace A3A7	Go to 5D-17

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

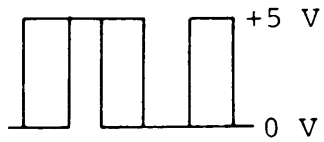
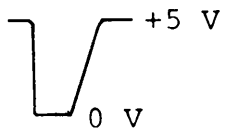
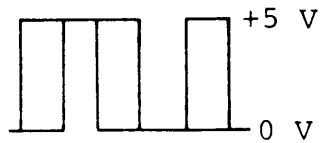
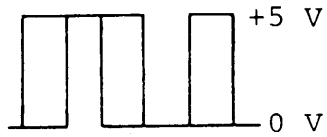
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5D (Cont)	8	A3A13 Pins 10, 11		Check track to A3A7 Pin 13	Go to 5D-9
	9	A3A13 Pins 5, 6		Lift pins 3, 4. Return to 5D-8. If still abnormal go to 5D-10. If normal, replace A3A14.	Check track to A3A12 Pin 1
	10	A3A13 Pin 1		Check, Replace A3A13	Go to 5D-15
	11	A3A14 Pins 10, 11		Check track to A3A7 Pin 1	Go to 5D-12
	12	A3A14 Pins 5,6		Go to 5D-14	Go to 5D-13
	13	A3A13 Pins 3, 4		Check track to A3A14 Pins 5, 6	Go to 5D-9

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cent!

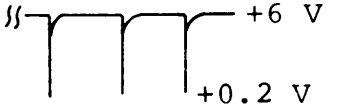
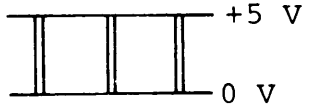
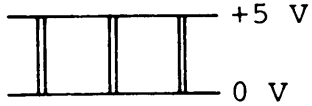
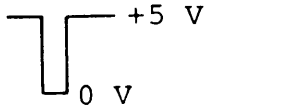
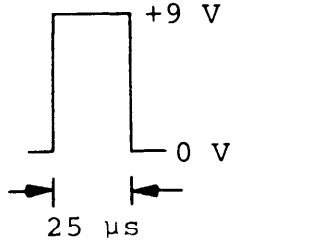
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5D (Cont)	14	A3A14 Pin 1		Check, Replace A3A14	Go to 5D-15
	15	Collector Q31		Check track to A3A13 or A3A14 Pin 1	Go to 5D-16
	16	A3A16 Pin 1	 Positive going pulses	Check Q31 R69, R70, C30	Go to 5D-17
	17	A3A16 Pin 6	 Negative going pulses	Check track to A3A7 Pin 2	Go to 5D-18
	18	A3A16 Pin 3		Check, Replace A3A16	Check track to A3 A12 Pin 1
6A	1	A3-J		Check connection at XA3-J	Check CR1, Check track from CR1 anode to Jct. R11, R10 and track from CR1 cathode to A3A6 Pin 11.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

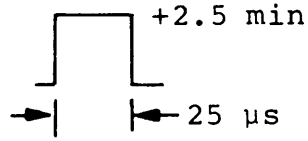
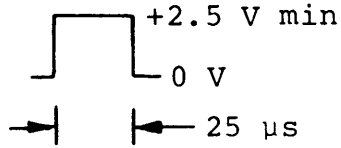
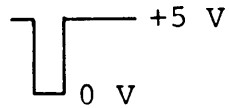
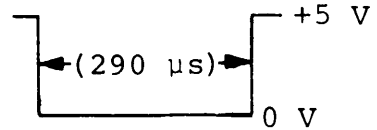
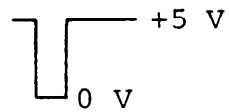
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B	1	A3A7 Pin 8	+5 V	Check connection between buffer A36 and TP2	Go to 6B-2
	2	A3A7 Pin 11		Replace A3A7	Go to 6B-3
	3	A3A6 Pin 11		Check track to A3A7 Pin 11	Go to 6B-4
	4	A3A6 Pin 5		Go to 6B-5	Go to 6B-6
	5	A3A6 Pin 4		Replace A3A6	Check track to A3A4. Pin 1.
	6	A3A5 Pin 6		Check track to A3A6 Pin 5	Go to 6B-7

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

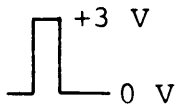
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B (Cont)	7	A3A5 Pin 5		Check, Replace A3A5	Check input at A3-M. Check C13, R35.
6C	1	Collector Q19	+0.3 V max	Check connection at XA3-1	Go to 6C-2
	2	A3-P	+4 V	Check Q19, R63, R62, C25	Check connection at XA3-P
6D	1	Collector Q24	+23.5 V	Check connection at XA3-3	Go to 6D-2
	2	Collector Q15	+1.2 V max	Check Q24, R91, Q23 for C-E short. Check C39 for short.	Go to 6D-3
	3	A3-B	+0.3 V max	Check connection at XA3-B	Check CR9, L1

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A	1	A3-3	* +23.5 V, 0.2 V PW = 2 to 5 s (Present when WAIT light is on)	Check connection at XA3-3	1) If PW is incorrect go to 7A-2 2) If no pulse present, go to position T1
	2	A3A10 Pin 6	* +5 V, 0 V PW = 70 ms min	Replace Q13, C21, R49	Replace R68, C19, A3A10
8A	1	A3-D	* +12 V, 0 V PW = 2 to 5 s	Check connection at XA3-D	1) If PW is incorrect go to 8A-2
	2	A3A16 Pin 6	* +5 V, 0 V PW = 70 ms min at 0.2 Hz	Replace Q27, C31, R77	Replace C29, R66, A3A16
9A	1	A3-3	+0.3 V max	Check connection at XA3-3	Go to 9A-2
	2	A3A7 Pin 6	+5 V no pulse present	Go to 9A-3	Go to 9A-7
	3	Collector Q15	+3 V	Check Q24, Q23, R22, R90	Go to 9A-4

* Approximately 7 seconds interpulse period

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

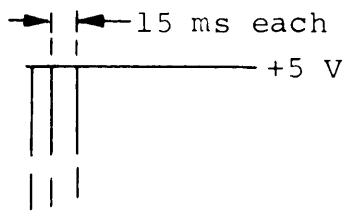
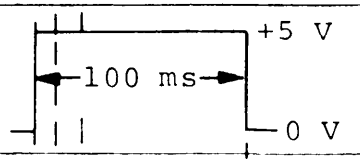
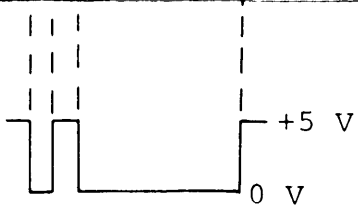
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A (Cont)	4	Collector Q14	+6 V	Check Q15, C33, R53	Go to 9A-5
	5	Collector Q12	+7.2 V	Check Q13, Q14, R50, R51	Go to 9A-6
	6	Collector Q11	+0.3 V max	Check Q12, C21	Check Q11, R43, R44
	7	A3A7 Pin 8		This wave form given as a timing reference for succeeding steps	
	8	A3A7 Pin 4		Go to 9A-9	Check track to A3A10 Pin 6. Replace A3A10.
	9	A3A7 Pin 5		Go to 9A-11	Check track to A3A9 Pins 10, 11. Go to 9A-10.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

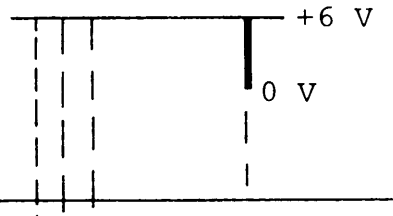
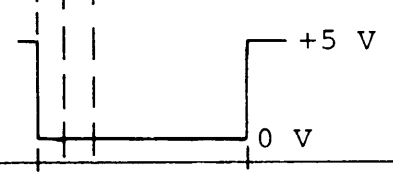
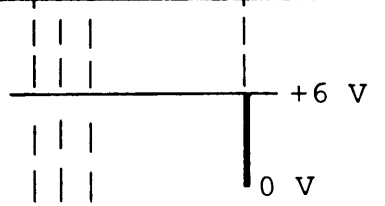
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A (Cont)	10	A3A9 Pin 1		Replace A3A9	Check Q32, R42, R40, R41, C20. Track to A3A10 Pin 1
	11	A3A7 Pin 3		Replace A3A7	Check track to A3A11 Pins 10, 11. Go to 9A-12.
	12	A3A11 Pin 1		Replace A3A11	Check track to collector Q32, return to 9A-10
9B	1	A3-D	0 V	Check connection at XA3-D	Go to 9B-2
	2	A3A7 Pin 12	+5 V no pulses present	Go to 9B-3	Go to 9B-7
	3	Collector Q29	+12 V	Check Q30	Go to 9B-4

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

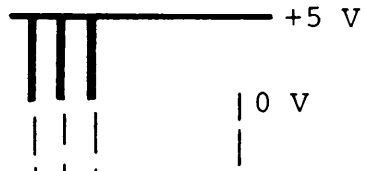
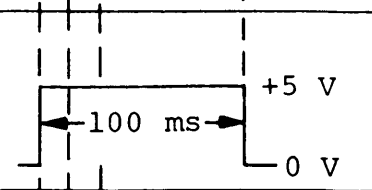
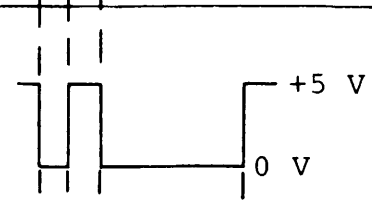
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9B (Cont)	4	Collector Q28	+6 V	Check Q29, R94	Go to 9B-5
	5	Collector Q26	+7.2 V	Check Q27, Q28, R78, R79	Go to 9B-6
	6	Collector Q25	+0.3 V max	Check Q26, C31, R76, R77	Check Q25, R72, R74, R77
	7	A3A12 Pin 1		This waveform given as a timing reference for succeeding steps	
	8	A3A7 Pin 2		Go to 9B-9	Check track to A3A13 Pin 6. Replace A3A16.
	9	A3A7 Pin 13		Go to 9B-11	Check track to A3A13 Pins 10, 11. Go to 9B-10.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX72 (Cont)

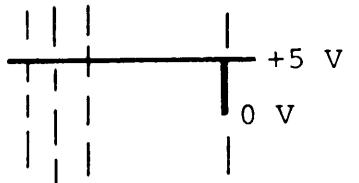
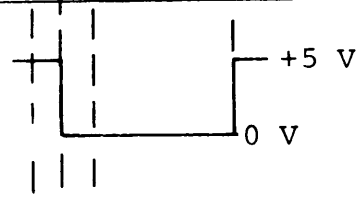
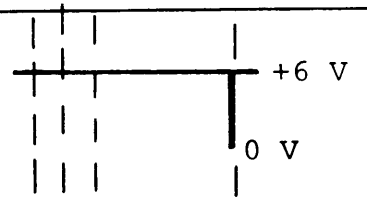
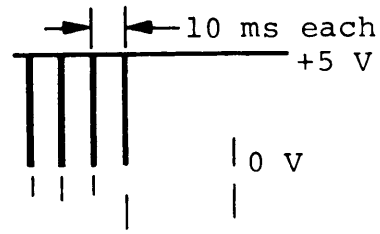
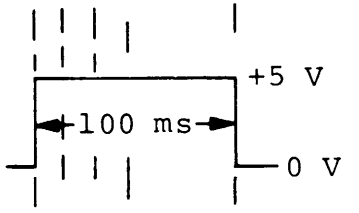
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9B (Cont)	10	A3A13 Pin 1		Replace A3A13	Check Q31, R71, R70, R69, C30. Track to A3A16 Pin 1.
	11	A3A7 Pin 1		Replace A3A7	Check track to A3A14 Pins 10, 11. Go to 9B-12.
	12	A3A14 Pin 1		Replace A3A14	Check track to collector Q31. Return to 9B-10.
T1	1	A3A7 Pin 8		The waveform is given as a timing reference for succeeding steps	
	2	A3A7 Pin 4		Go to T1-3	Check track to A3A10 Pin 6; replace A3A10.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

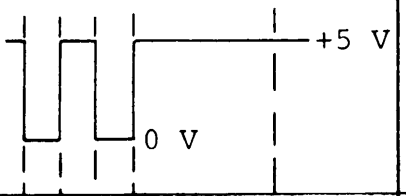
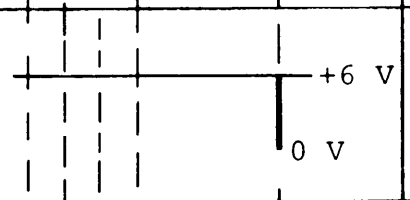
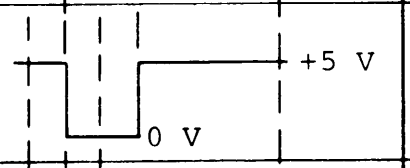
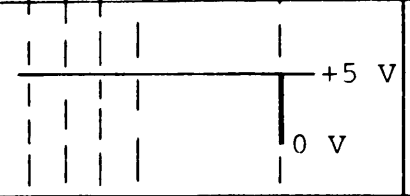
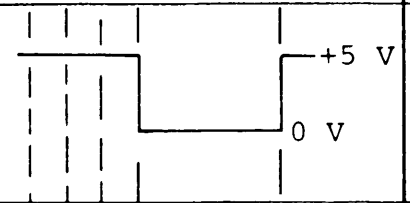
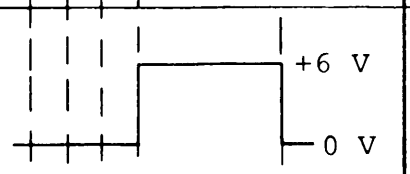
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
T1 (Cont)	3	A3A7 Pin 5		Go to T1-5	Check track to A3A9 Pins 10, 11. Go to T1.
	4	A3A9 Pin 1		Replace A3A9	Check Q32, R42, R40, R41, C20. Track to A3A10, Pin 1.
	5	A3A7 Pin 3		Go to T1-7	Check track to A3A11, Pins 10, 11. Go to T1-6.
	6	A3A11 Pin 1		Replace A3A11	Check track to collector Q32. Go to T1-4.
	7	A3A7 Pin 6		Go to T1-8	Replace A3, A7
	8	Collector Q11		Replace Q12	If amplitude is less than 3 V replace Q11

Table 5-8. Mode 4 (A3), Fault Isolation procedure for RT-859/APX-72 (Cont)

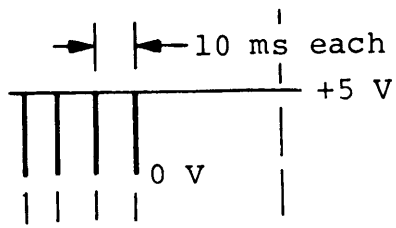
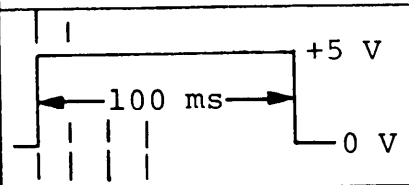
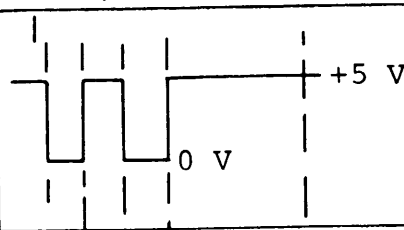
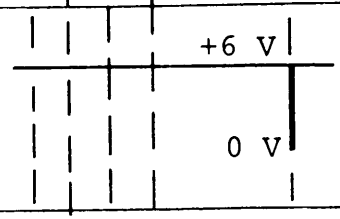
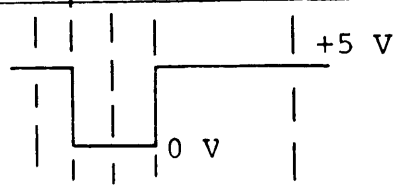
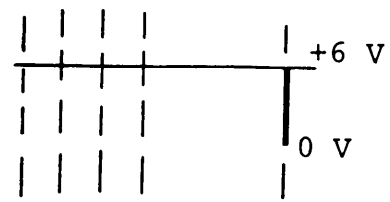
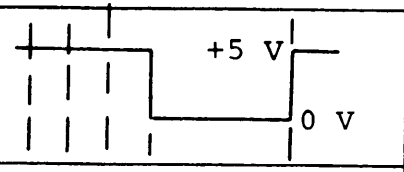
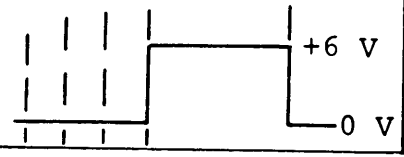
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
T2	1	A3A12 Pin 1		This waveform given as a timing reference for succeeding steps	
	2	A3A7 Pin 2		Go to T2-3	Check track to A3A16 Pin 6. Replace A3A1.
	3	A3A7 Pin 13		Go to T2-5	Check track to A3A13, Pin 10, 11. Go to T2-4.
	4	A3A13 Pin 1		Replace A3A13	Check Q31, R71, R70, R69, C30. Track to A3A16 Pin 1.
	5	A3A7 Pin 1		Go to T2-7	Check track to A3A14 Pins 10, 11. Go to T2-6.

Table 5-8. Mode 4 (A3), Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
T2	6	A3A14 Pin 1		Replace A3A14	Check track to collector Q31. Return to T2-4.
	7	A3A7 Pin 12		Go to T2-8	Replace A3A7
	8	Collector Q25		Replace Q26	If amplitude is less than 3 V, replace Q25

NOTES FOR TABLE 5-9

MODE 4 (A3), FAULT ISOLATION PROCEDURE FOR RT-859A/APX-72

NOTE 1: Whenever this procedure indicates the replacement of an integrated circuit, first check that the +5 Vdc and ground connections are good. (Refer to schematic for pin numbers.)

NOTE 2: When it is suspected that an abnormal waveform could be caused by an integrated circuit having developed an input short, thereby loading the circuit being viewed, lift the input pin of the integrated circuit. If normal waveform is restored, replace the defective integrated circuit.

CAUTION

Integrated circuits can be damaged electrically if the soldering iron tip is not at ground potential.

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cent)

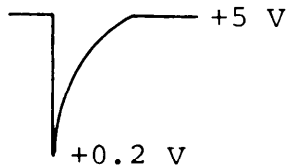
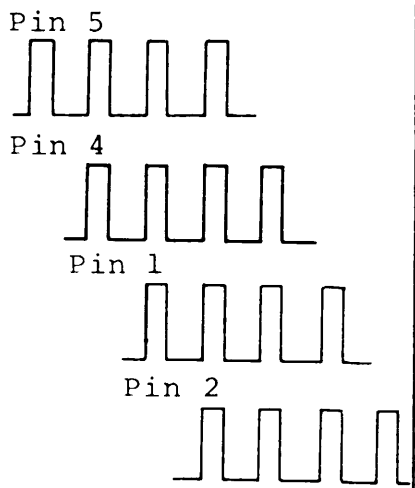
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A	1	A3A201 Pin 6		Check connection between buffer A36 and TP7	Lift A3A201 Pin 6 and attach a test probe to lifted pin. If waveform is still abnormal, go to 2A-2. If normal waveform is restored, reconnect Pin 6 and lift A3A203 Pin 1, A3A6 Pin 1, and A3A15 Pin 1, each in turn. If lifting a lead restores normal waveform, replace the particular I.C. if otherwise go to 2A-2.
	2	A3A201 Pins 5, 4, 1, & 2		If all inputs are normal check, replace A3A201	If Pin 5 abnormal go to 2A-3. If Pin 4 abnormal go to 2A-7. If Pin 1 abnormal go to 2A-8. If Pin 2 abnormal go to 2A-9.

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

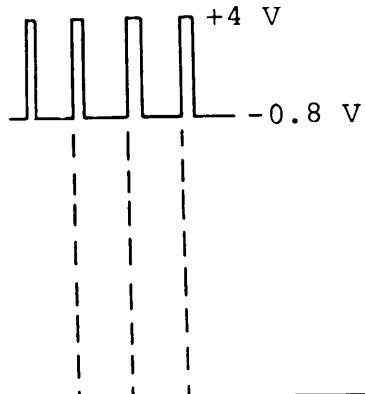
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	3	A3-Z		Check connection at XA3 Pin Z	Check R201, 202 and C201. If still abnormal go to 2A-4.
	4	A3A202 Pin 12	-1.0 V to +0.8 V	Go to 2A-6	Go to 2A-5
	5	A3A204 Pin 8	+6.2 V	Check R240 and VR-201	Check, replace A3A204
	6	A3A201 Pin 1		Return to 2A-3	Lift A3A202 Pin 11; if normal waveform is restored, check, replace A3A202; if still abnormal, lift A3A201 Pin 9; if normal waveform is restored check, replace A3A201
	7	A3-U		Check Q201, R204, 205, 203. Replace A3A201.	Check connection at XA3-U

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

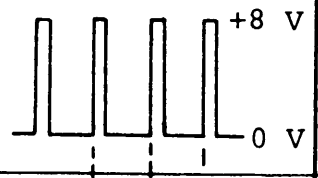
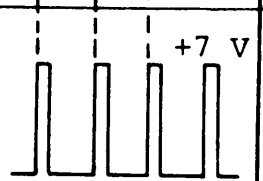
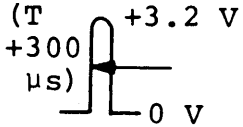
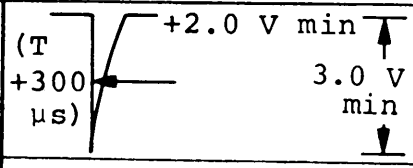
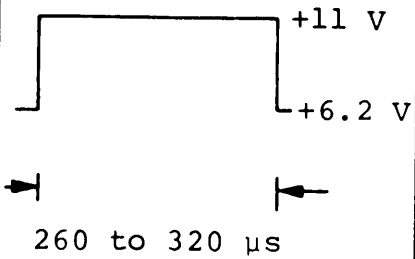
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A (Cont)	8	A3-S		Check Q202, R206, 207, 208. Replace A3A201	Check connection at XA3 Pin S
	9	A3-T		Check Q203, R209, 210, 211. Replace A3A201	Check connection at XA3 Pin T
2B	1	A3A5 Pin 8		Check connection between buffer A36 and TP8	Go to 2B-2
	2	A3A5 Pin 9		Check, replace A3A5	Go to 2B-3
	3	A3A204 Pin 8		Check R110, 99 C206	If PW is the only abnormality ADJ R224. If abnormality persists check R225, C205 then replace A3A204 If other abnormality go to 2B-4

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

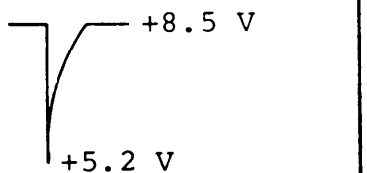
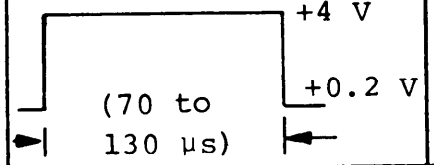
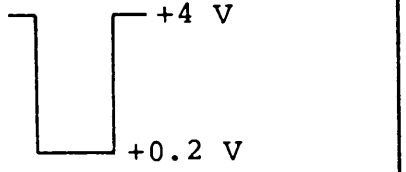
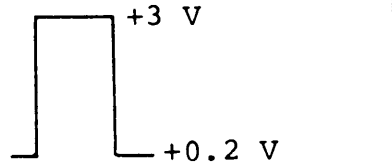
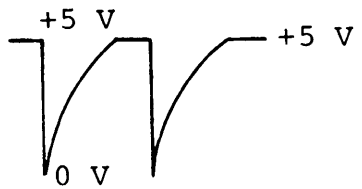
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2B (Cont)	4	A3A204 Pin 1		Check, replace A3A204	Check R222, 223, and C204. Check connection to A3A201 Pin 6. Go to 2A-1.
2C	1	A3-6		Check connection at XA3 Pin 6	If PW is only abnormality go to 2C-10 Go to 2C-2
	2	A3A202 Pin 10		Go to 2C-6	Go to 2C-3
	3	A3Q204 Collector		Check Q211, R214, R238, R239, C17	Go to 2C-4
	4	A3A201 Pin 8		Check Q204, CR201, R212, R213, C202	Go to 2C-5

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

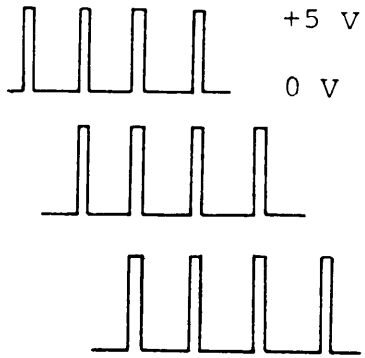
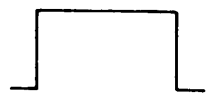
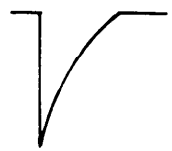
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2C (Cont)	5	A3A201 Pin 9 Pin 10 Pin 13		Check replace A3A201	Check connection to A3A201 Pin 5 Go to 2A-3. Check connection to A3A201 Pin 4 Go to 2A-7. Check connection to A3A201 Pin 1. Go to 2A-8.
	6	A3A202 Pin 9		Check, replace R217, A3A202	Go to 2C-7
	7	A3A202 Pin 1		Go to 2C-8	Go to 2C-10
	8	A3A202 Pin 2	+5 V	Check, replace A3A202	Go to 2C-9
	9	A3A6 Pin 1		Check, replace A3A6	Go to 2A-1

Table 5-9. Mode 4 (A3), Fault Isoltion Procedure for RT-859A/APX-72 (Cont)

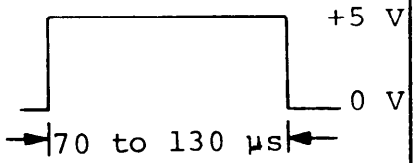
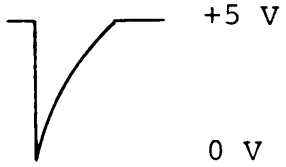
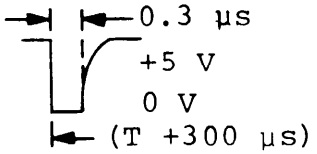
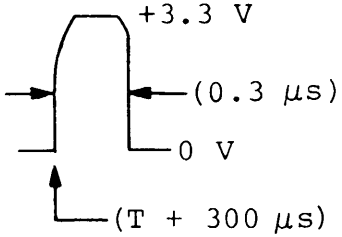
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2C (Cont)	10	A3A203 Pin 8		Check, replace A3A202	If PW is the only abnormality ADJ. R215. If abnormality persists check R216 C203 then replace A3A203. If other abnormality go to 2C-11.
	11	A3A203 Pin 1		Check, replace A3A203	Go to 2A-1
2D	1	A3A7 Pin 8		Check connection at TP2	Go to 2D-2
	2	A3A7 Pin 9		Go to 2D-3	Check track connection to A3A5 Pin 8

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

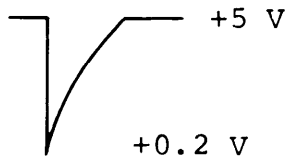
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2D (Cont)	3	A3A7 Pin 11	+5 V	Go to 2D-4	Check track connection to A3A6 Pin 11
	4	A3A7 Pin 10	+5 V	Check, replace A3A7	Go to 2D-5
	5	A3A15 Pin 11	+5 V	Check track to A3A7 Pin 10	Go to 2D-6
	6	A3A15 Pin 1		Check, replace A3A15	Check track to A3A3 Pin 6

Table 5-9. Mode 4 (A3), Faut Isoaltion Procedure for RT-859A/APX-72

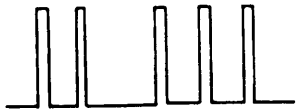
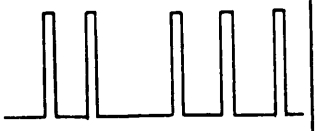
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A	1	A3A201 Pin 6	+5 V no pulses present	Check connection between buffer A36 and TP7	Go to 3A-2
	2	A3A201 Pins 5, 4, 1, & 2	Pin 5  Pin 4  Pin 1  Pin 2 	If all inputs are normal, check, replace A3A201	If Pin 5 is abnormal check R201, 202 and C201 If Pin 4 is abnormal check Q201, R204, 205, 203 If Pin 1 is abnormal check Q202, R206, 207, 208 If Pin 2 is abnormal check Q203, R209, 210, 211 Replace A3A201

Table 5-9, Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

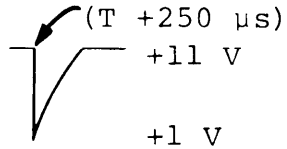
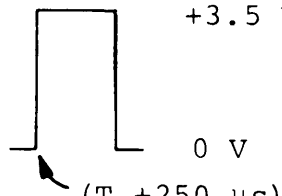
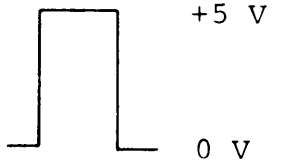
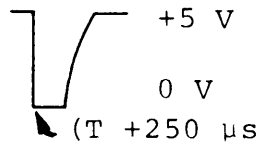
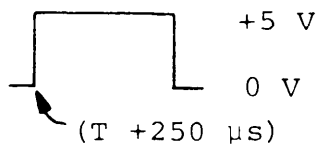
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3B	1	Collector Q35		Check CR6	Go to 3B-2
	2	A3-K		Check Q35, CR17, R36, R38, R37, R39, C14, C15	Check connection at XA3-K
3C	1	A3-6		Check connection at XA3-6	Perform step 2C-1 through 2C-5 while test switch is in position 3
3D	1	A3A12 Pin 6		Check connection between buffer A36 and TP4	Go to 3D-2
	2	A3A12 Pin 4		Go to 3D-3	Go to 3D-4

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

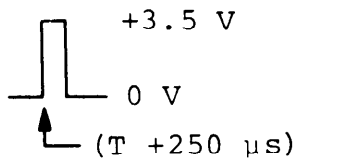
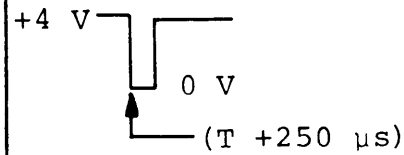
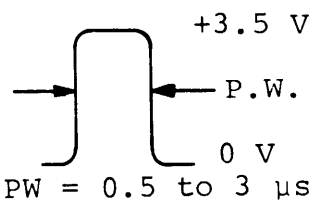
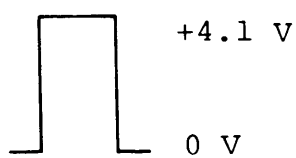
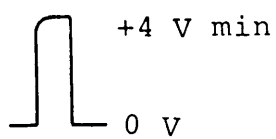
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3D (Cont)	3	A3A12 Pin 3		Check, replace A3A12, R65, C27	Check track to R38
	4	A3A5 Pin 2		Check, replace A5, R112, C40	Check track to A3 Pin 12. Check connection at XA3-12.
4A	1	A3-20		Check connection at XA3-20	If PW is abnormal replace Q9,C9, R32, R34. If amplitude is abnormal go to 4A-2.
	2	Collector Q9		Check Q10	Go to 4A-3
	3	Collector Q8		Check Q9, R33, R31, R32, C9	Go to 4A-4

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

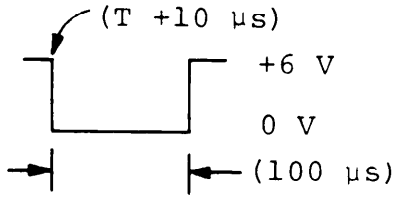
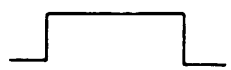
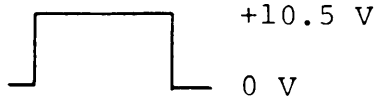
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A (Cont)	4	A3A202 Pin 3		Check Q8, CR16, R31, R30, R108, C7	Return to 2C-7
4B	1	Collector Q35	+11 V no pulses present	Check connection at A3-L	Go to 4B-2
	2	A3-N	+5 V	Check track from CR17 anode to emitter of Q35 for short	Check connection XA3-N
4C	1	A3-J		Check connection at XA3 Pin J	Go to 4C-2
	2	Collector Q205		Check Q206	Check Q205, R220, 219, 218 & connection to A3A203 Pin 6

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

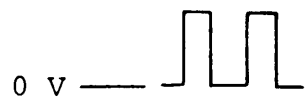
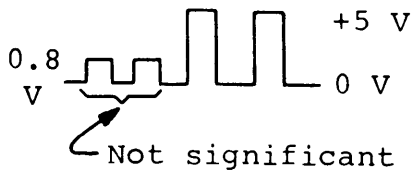
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4D	1	A3-V	 PW 0.4 to 0.6 µs (first pulse only)	Check connection at XA3 Pin V	If PW is only abnormality replace Q208, C207, R230. If other abnormality go to 4D-2.
	2	A3A202 Pin 6		Check Q209, CR203, R234	Go to 4D-3
	3	Collector Q207		Check, replace A3A202	Go to 4D-4
	4	Emitter Q210		Check Q207, Q208, R229, R230, R231, R232, R228, R227, C207	Go to 4D-5

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

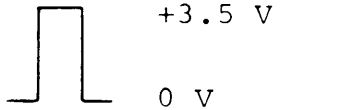
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4D (Cont)	5	A3-W		Check Q210, DL1, CR205, CR206, R237, R236	Check connection at XA3-W
5A	1	A3-V		Check connection at XA3-V	Check, replace CR207. Return to 4D-1.
5B	1	A3A12 Pin 6	+5.0 V no pulses present	Check connection between buffer A36 and TP4	Go to 5B-2
	2	A3A12 Pin 4	+0.2 V no pulses present	Check, replace A3A12	Go to 5B-3
	3	A3A5 Pin 2	+5.0 V no pulses present	Check replace A3A5, R112, C40	Check connection to XA3-12

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

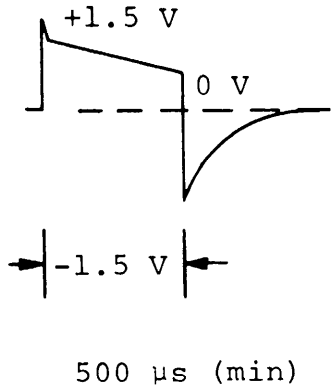
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5C	1	A3-1		Check connection at XA3-1	1) If amplitude is less than 3 V p-p adjust R89 for maximum signal amplitude. 2) If pos. pulse width is shorter than 500 µs, go to 5C-2. 3) If no pulse is present or pulse amplitude is less than 3 V p-p, go to 5C-3.
	2	A3A8 Pin 1		Check C32, T1, R89, C34	Check C17, R67, R109, replace A3A8
	3	Collector Q20		Check Q21, Q22, R83, R84, R85, R86, R87, R88	If collector Q20 is +7 VDC, go to 5C-5. If collector Q20 is 0 VDC, go to 5C-4.
	4	Junction C25, R62	+1 V max	Check Q19, R64	Check L2. Check connection at XA3-P.

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

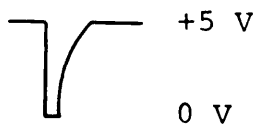
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5C (Cont)	5	A3A8 Pin 1		Check Q20, CR8, R80, R81, R82	Go to 5C-6
	6	A3A8 Pin 3		Check, replace A3A8	Check track to A3A7 Pin 8
5D	1	Collector Q24	+19 V min	Check connection at XA3 Pin 3	Go to 5D-2
	2	Collector Q15	+0.3 V max	Check Q24, Q23, for C-E short, check C39 for short	Go to 5D-3
	3	Collector Q14	+11 V	Check Q15, R52	Go to 5D-4
	4	Collector Q12	+0.3 V max	Check Q13, Q14	Go to 5D-5

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

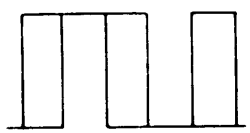
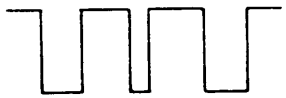
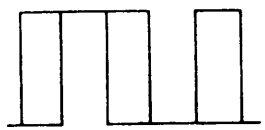
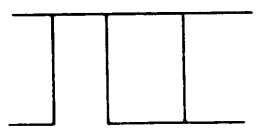
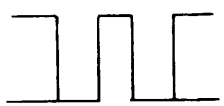
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5D (Cont)	5	Collector Q11	 +6.5 V 0.2 V	Check Q12, R47	Go to 5D-6
	6	A3A7 Pin 6	 +5 V 0 V	Check Q11, CR12, R43, R44, R45, R46	Go to 5D-7
	7a	A3A7 Pin 5	 +5 V 0 V	Go to 5D-7b	Go to 5D-8
	7b	A3A7 Pin 3	 +5 V 0 V	Go to 5D-7c	Go to 5D-11
	7c	A3A7 Pin 4	 +5 V 0 V	Check, replace A3A7	Go to 5D-17

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-359A/APX-72 (Cont)

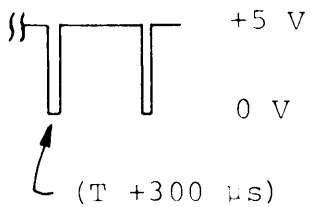
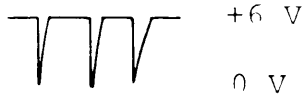
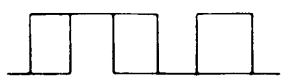
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5D (Cont)	8	A3A9 Pin 10, 11	Same as 5D-7a	Check track to A3A7, Pin 5	Go to 5D-9
	9	A3A9 Pin 5, 6		Lift Pins 3, 4. Return to 5D-8 if still abnormal Go to 5D-10. If normal replace A3A11.	Check track to A3A7 Pin 8
	10	A3A9 Pin 1		Check, replace A3A9	Go to 5D-15
	11	A3A11 Pin 10, 11	Same as 5D-7b	Check track to A3A7 Pin 3	Go to 5D-12
	12	A3A11 Pin 5, 6		Go to 5D-14	Go to 5D-13
	13	A3A9 Pin 3, 4	Same as 5D-12	Check track to A3A11 Pin 5, 6	Go to 5D-8

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

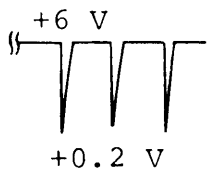
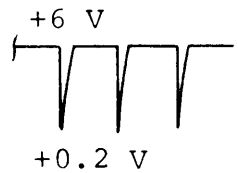
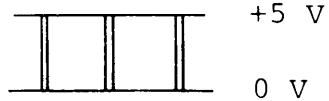
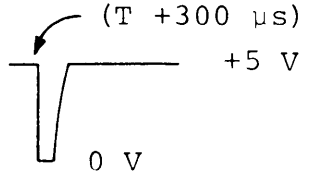
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5D (Cont)	14	A3A11 Pin 1		Check, replace A3A11	Go to 5D-14
	15	Collector Q32		Check track to A3A9 Pin 1 and A3A11, Pin 1	Go to 5D-16
	16	A3A10 Pin 1		Check Q32 R40, R41, C20	Go to 5D-17
	17	A3A10 Pin 6		Check track to A3A7 Pin 4	Go to 5D-18
	18	A3A10 Pin 3		Check, replace A3A10	Check track to A3A7 Pin 8

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

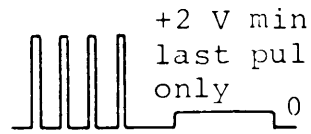
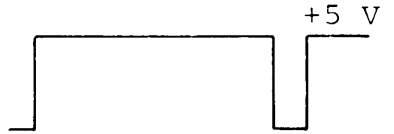
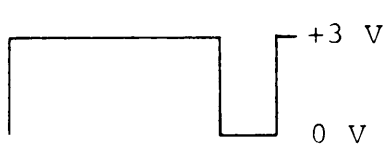
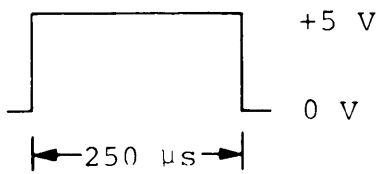
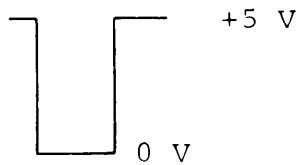
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6A	1	A3A201 Pin 5		Check connection between buffer assembly A36 and A3TP7	Go to 6A-2
	2	A3A202 Pin 12		Go to 6A-3	Check, replace VR201
	3	A3A202 Pin 13		Check, replace A3A202	Check R241 R243, CR210
6B	1	A3A15 Pin 11		Check track to A3A7 Pin 10. Replace A3A7.	Go to 6B-2
	2	A3A15 Pin 5		Lift Pin 8 of A3A7. If lamp stays on, go to 11A-2. If lamp B goes out, replace A3A15.	Check track to A3A12 Pin 6

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

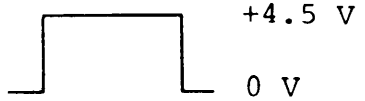
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6C	1	A3-R	+7 V	1) Adjust R29 CW until the voltage is = 7 V; Lamp C will turn off. 2) Check connection at XA3-R.	Check for short along track from Q6 collector to A3 Pin 4
	2	Collector Q6	+8 ± 2 V	Replace CR4	Go to 6C-3
	3	Collector Q4		Check CR3, Q5, Q6, R26, R25, R27, R29	Check Q4, CR3, C12, R23, R22, R19, R20, R21

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

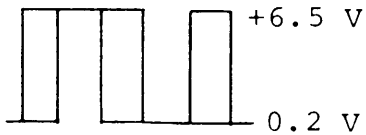
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6D	1	A3-D	+12 V	Check connection between buffer A36 and TP5. Check connection at XA3-D.	Go to6D-2
	2	Collector Q29	+0.3 V max	Check Q30, R95	Go to 6D-3
	3	Collector Q28	+11 V	Check Q29, R93	Go to 6D-4
	4	Collector Q26	+0.3 V max	Check Q27, Q28 for C-E short	Go to 6D-5
	5	Collector Q25		Check Q26, R75	Go to 6D-6

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

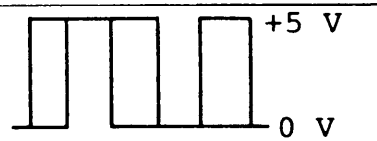
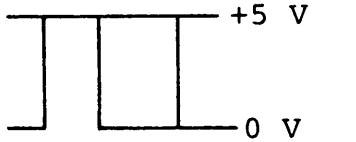
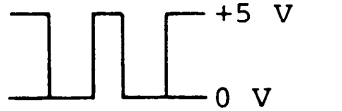
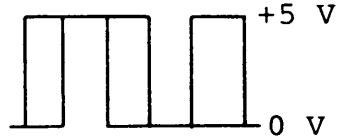
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6D (Cont)	6	A3A7 Pin 12		Check Q25, CR11, R74, R73, R72, R97	Go to 6D-7
	7a	A3A7 Pin 13		Go to 6D-7b	Go to 6D-8
	7b	A3A7 Pin 1		Go to 6D-7c	Go to 6D-11
	7c	A3A7 Pin 2		Check, replace A3A7	Go to 6D-17
	8	A3A13 Pin 10, 11		Check track to A3A7 Pin 13	Go to 6D-9

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

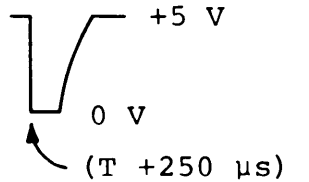
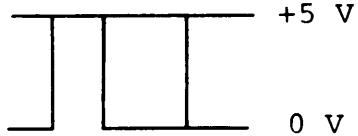
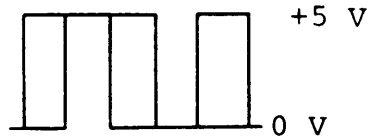
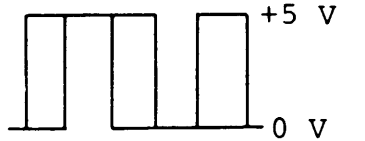
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6D (Cont)	9	A3A13 Pins 5, 6		Lift Pins 3, 4. Return to 5C-8. If still abnormal go to 5C-10. If normal, replace A3A14.	Check track to A3A12 Pin 6
	10	A3A13 Pin 1		Check, replace A3A13	Go to 6D-15
	11	A3A14 Pins 10, 11		Check track to A3A7 Pin 1	Go to 6D-12
	12	A3A14 Pins 5, 6		Go to 6D-14	Go to 6D-13
	13	A3A13 Pins 3, 4		Check track to A3A14 Pins 5, 6	Go to 6D-9

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

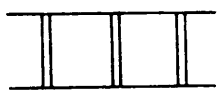
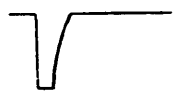
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6D (Cont)	14	A3A14 Pin 1	 +6 V 0 V	Check, Replace A3A14	Go to 6D-15
	15	Collector Q31	 +6 V 0 V	Check track to A3A13 or A3A14 Pin 1	Go to 6D-16
	16	A3A16 Pin 1	 +5 V 0 V	Check Q31 R69, R70, C30	Go to 6D-17
	17	A3A16 Pin 6	 +5 V 0 V	Check track to A3A7 Pin 2	Go to 6D-18
	18	A3A16 Pin 3	 +5 V 0 V	Check, Replace A3A16	Check track to A3A12 Pin 6

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

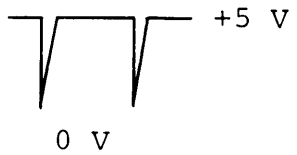
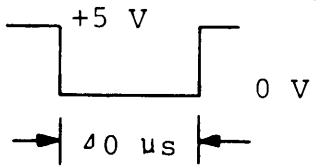
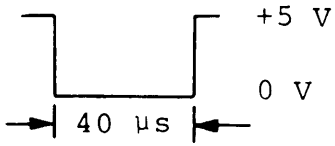
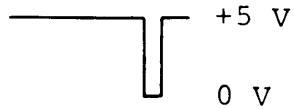
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A	1	A3A201 Pin 6		Check connector between buffer assembly A36 and A3TP7	If IND's B&D are on go to 7B-1. If IND A only is on, replace CR209.
7B	1	A3A7 Pin 8	+5 V	Check connection between buffer A36 and TP2	Go to 7B-2
	2	A3A7 Pin 11		Replace A3A7	Go to 7B-3
	3	A3A6 Pin 11		Check track to A3A7 Pin 11	Go to 7B-4
	4	A3A6 Pin 5		Go to 7B-5	Go to 7B-6

Table 5-9. Mode 4 (A3), Fault Isoaltion Procedure for RT-859A/APX-72 (Cont)

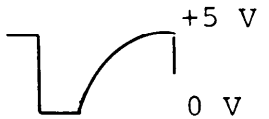
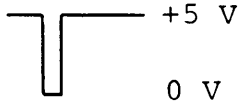
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7B (Cont)	5	A3A6 Pin 1		Replace A3A6	Check track from A3A6-1 to A201-6
	6	A3A5 Pin 6		Check track to A3A6 Pin 5	Go to 7B-7
	7	A3A5 Pin 5		Check, Replace A3A5	Check input at A3-M. Check R35.
7C	1	Collector Q19	+0.3 V max	Check connection at XA3-1	Go to 7C-2
	2	A3-P	+4.5 V	Check Q19, R63, R62, C25	Check connection XA3-P

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

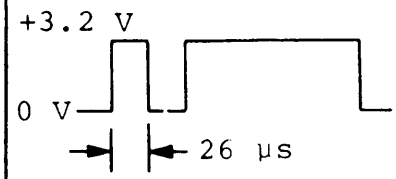
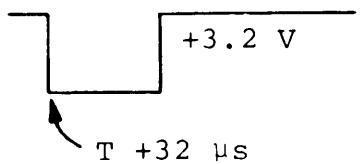
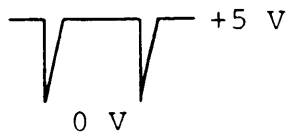
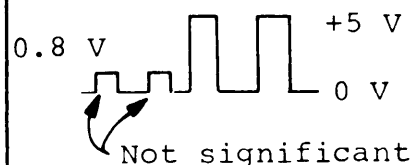
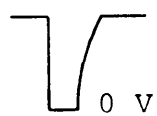
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7D	1	A3-6		Check connection at XA3-6	Go to 7D-2
	2	A3A202 Pin 2		Check, Replace A3A202	Check connection to A3A6 Pin 11. Go to 7B-3.
8A	1	A3A201 Pin 6		Check connection between buffer assembly A36 and A3TP7	Check, replace CR202
8B	1	A3A202 Pin 6		Check connection at XA3-V	Check, replace CR207
8C	1	A3A8 Pin 4		Check, Replace A3A8	Check track to A3A12 Pin 6

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

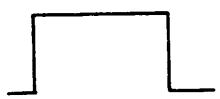
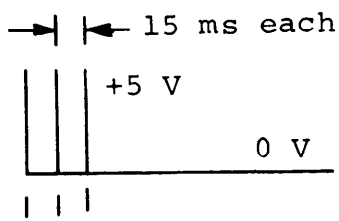
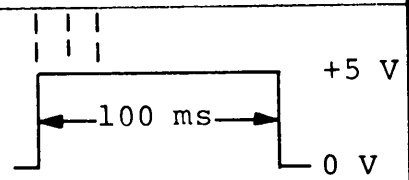
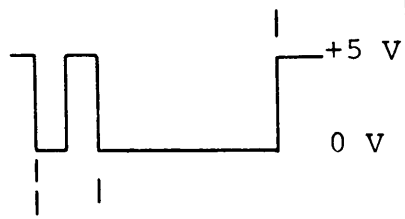
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8D	1	Collector Q15	+0.8 V	Check connection at XA3-3	Check, replace CR9, L1, R106, C33
9A	1	A3-3	 PW = 2 to 5 s	Check connection at XA3-3	1) If PW is incorrect go to 9A-2 2) If no pulse present, go to position T1
	2	A3A10 Pin 6	 PW = 70 ms min	Replac Q13, R49	Replace C19, R68, A3A10
10A	1	A3-D	 PW = 2 to 5 s	Check connection at XA3-D	1) If PW is incorrect go to 10A-2 2) If no pulse present, go to position T2
	2	A3A16 Pin 6	 PW = 70 ms min	Replace Q27, C31, R77	Replace C29, R66, A3A16

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11A	1	A3-3	+0.3 V max	Check connection at XA3-3	Go to 11A-2
	2	A3A7 Pin 6	+5 V no pulse present	Go to 11B-3	Go to 11A-7
	3	Collector Q15	+3 V	Check Q24, Q23, R22, R90	Go to 11A-4
	4	Collector Q14	+6 V	Check Q15, C33, R53	Go to 11A-5
	5	Collector Q12	+7.2 V	Check Q13, Q14, R50, R51	Go to 11A-6

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11A (Cont)	6	Collector Q11	+0.3 V max	Check Q12, C21, R48, R49	Check Q11, R43, R44, R46
	7	A3-Z		This waveform given as a timing reference for succeeding steps	
	8	A3A7 Pin 4		Go to 11A-9	Check track to A3A10 Pin 6. Replace A3A10.
	9	A3A7 Pin 5		Go to 11A-11	Check track to A3A9 Pins 10, 11. Go to 11A-10.

Mode 4 (A3), Fault Isolation Procedure
for RT-859A/APX-72 (Cont)

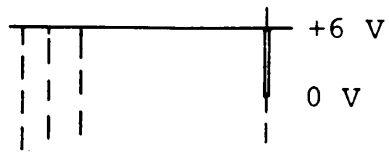
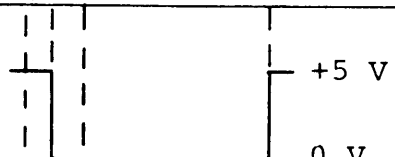
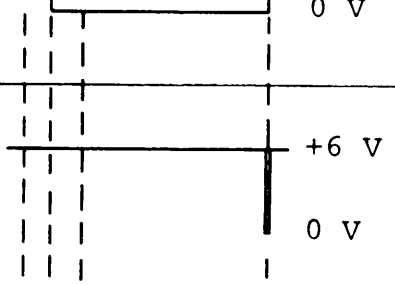
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11A	10	A3A9 Pin 1		Replace A3A9	Check Q32, R42, R40, R41, C20. Track to A3A10 Pin 1.
	11	A3A7 Pin 3		Replace A3A7	Check track to A3A11 Pins 10, 11. Go to 11A-12
	12	A3A11 Pin 1		Replace A3A11	Check track to collector Q32. Return to 11A-10.
11B	1	A3-D	0 V	Check connection at XA3-D	Go to 11B-2
	2	A3A7 Pin 12	+5 V no pulses present	Go to 12B-3	Go to 11B-3

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11B (Cont	3	Collector Q29	+12 V	Check Q30	Go to 11B-4
	4	Collector Q28	+ 6 V	Check Q29, R94	Go to 11B-5
	5	Collector Q26	+7.2 V	Check Q27, Q28, R78, R79	Go to 11B-6
	6	Collector Q25	+0.3 V max	Check Q26, C31, R76, R77	Check Q25, R72, R74, R75, R77

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

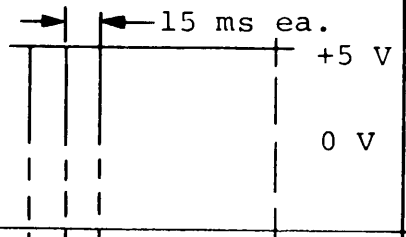
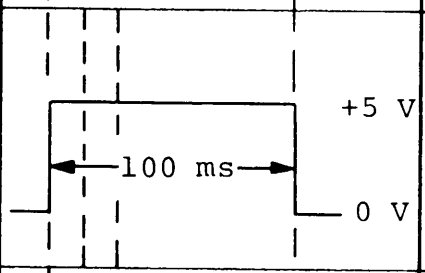
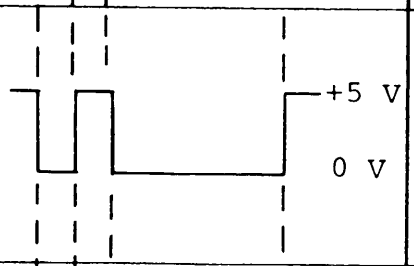
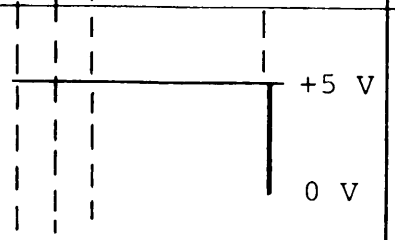
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11B (Cont)	7	A3A12 Pin 6		This waveform given as a timing reference for succeeding steps	
	8	A3A7 Pin 2		Go to 11B-9	Check track to A3A16 Pin 6. Replace A3A16.
	9	A3A7 Pin 13		Go to 11B-11	Check track to A3A13 Pins 10, 11. Go to 11B-10.
	10	A3A13 Pin 1		Replace A3A13	Check Q31, R71, R60, R69, C30. Track to A3A16 Pin 1.

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

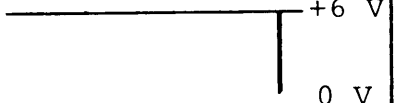
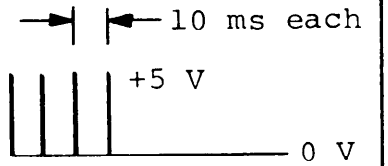
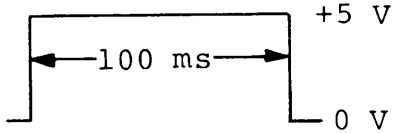
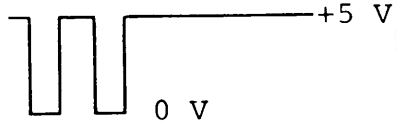
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVFFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11B (Cont)	11	A3A7 Pin 1		Replace A3A7	Check track to A3A14 Pins 10, 11. Go to 11B-12.
	12	A3A14 Pin 1		Replace A3A14	Check track to collector Q31, return to 11B-10
T1	1	A3-Z		The waveform is given as a timing reference for succeeding steps	
	2	A3A7 Pin 4		Go to T1-3	Check track to A3A10 Pin 6, replace A3A10
	3	A3A7 Pin 5		Go to T1-5	Check track to A3A9 Pins 10, 11. Go to T1-4.

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

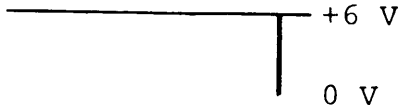
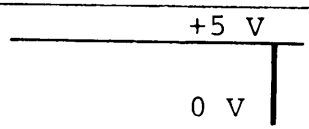
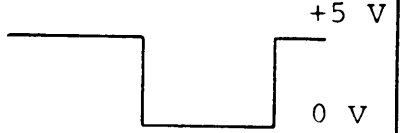
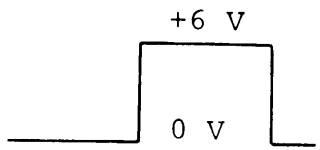
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
T1	4	A3A9 Pin 1		Replace A3A9	Check Q32, R42, R40, R41, C20 track to A3A10, Pin 1
	5	A3A7 Pin 3		Go to T1-7	Check track to A3A11, Pins 10, 11. Go to T1-6.
	6	A3A11 Pin 1		Replace A3A11	Check track to collector Q32. Go to T1-4.
	7	A3A7 Pin 6		Go to T1-8	Replace A3A7
	8	Collector Q11		Replace Q12	If amplitude is less than 3 V replace Q11

Table 5-9. Mode 4 (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

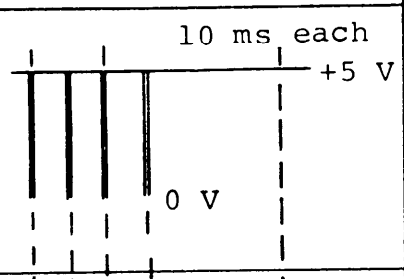
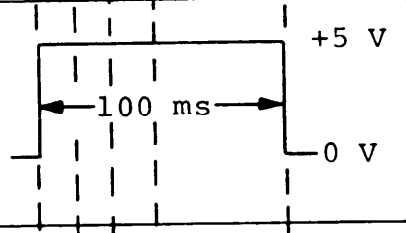
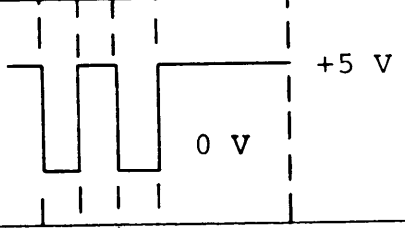
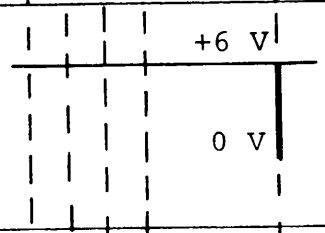
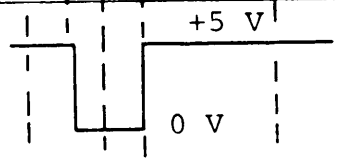
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
T2	1	A3A12 Pin 6		This waveform given as a timing reference for succeeding steps	
	2	A3A7 Pin 2		Go to T2-3	Check track to A3A16 Pin 6. Replace A3A16.
	3	A3A7 Pin 13		Go to T2-5	Check track to A3A13 Pin 10, 11. Go to T2-4.
	4	A3A13 Pin 1		Replace A3A13	Check Q31, R71, R70, R69, C30. Track to A3A16 Pin 1.
	5	A3A7 Pin 1		Go to T2-7	Check track to A3A14 Pins 10, 11. Go to T2-6.

Table 5-9. Mode 4, (A3), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

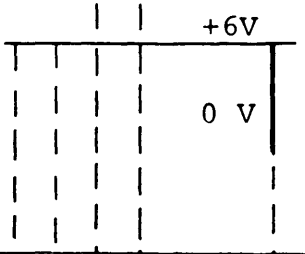
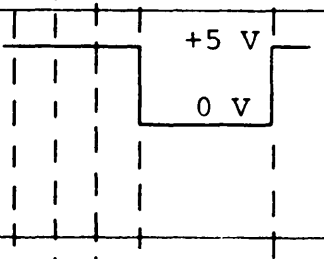
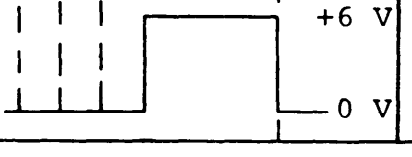
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
T2 (Cont)	6	A3A14 Pin 1		Replace A3A14	Check track to collector Q31. Return to T2-4.
	7	A3A7 Pin 12		Go to T2-8	Replace A3A7
	8	Collector Q25		Replace Q26	If amplitude is less than 3V, replace Q25

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure

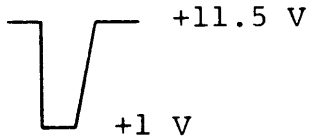
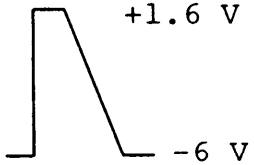
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	Collector Q21		Check connection between buffer A37 and TP4	If Lamp D is not lighted, proceed to 1A-2. If Lamp D is lighted proceed to Test Sequence 1D-1.
	2	Base Q21		Check Q21, R62	If the positive peak of the pulse goes to +6 V check Q21, CR79, R63 If the pulse is missing check VR1, R64, C20, R65
1B	1	Collector Q14	+0.3 V max	Check connection at XA4-14	Check Q14, R34, R31, C12, C11
1C	1	A4-J	-2.2 V	Check connection at XA4-J	Check RT1, C35

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

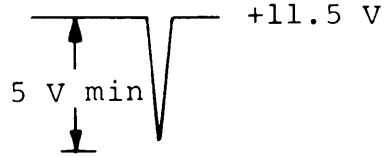
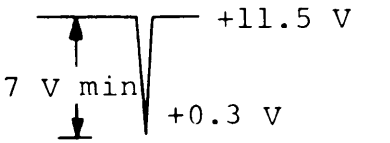
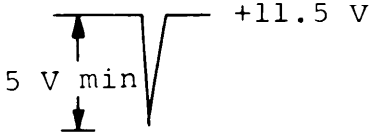
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1D	1	Collector Q22	+0.3 V max	Check connection at XA4-12	Go to 1D-2
	2	Collector Q40	+6 V	Check Q22	Check Q40, R131, R132, R133, R66, R67, R68
2A	1	A4-C		Check connection at XA4-C	If Lamps B and C are lighted, go to 2A-2. If Lamps B and C are not lighted, check C2.
	2	Collector Q15		Check connection at XA4-B	Check Q15, R37, R36, R35, C13
2B	1	A4-1		Check connection at XA4-1	Check CR9, C3, R38

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

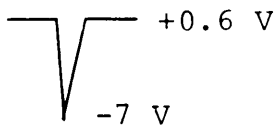
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2C	1	Anode of CR32	+11.5 V	Check connection at XA4-3. Go to 2C-2	Go to 2C-2
	2	Collector Q31	+0.3 V max	Go to 2C-3	Check Q31, R92, R94, Q27, CR33
	3	Collector Q32	+0.3 V max	Go to 2C-4	Check Q32, R96, R99, Q29, CR34
	4	Collector Q33	+0.3 V max	Go to 2C-5	Check Q33, R103, R102, Q29, CR35
	5	Base Q30		Check Q30, CR32, Q26, R73	Check CR43, R72, R91, C41

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

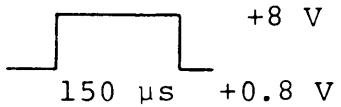
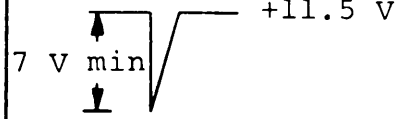
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A	1	A4-Z		Check connection at XA4-Z	If Lamps B and C are lighted, go to 3A-2 If Lamp B is lighted and Lamp C is out go to 3B-1 If Lamps B and C are out, go to 3A-3
	2	Collector Q16		Go to 3A-3	Check connection at XA4-D. Check Q16, R41, R40, R39, C14.
	3	Collector Q4		Check Q5, R11	Check Q4, Q3, Q2, CR77, CR4, CR2, R10, R9, R7, R5, R6, R8, C5, C4, CR5, CR3
3B	1	A4-1		Check connection at XA4-1	Check CR10, C3

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

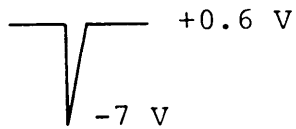
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3C	1	Anode of CR33	+11.5 V	Check connection at XA4-4. Go to 3C-2.	Go to 3C-2
	2	Collector Q30	+0.3 V max	Go to 3C-3	Check R88
	3	Collector Q32	+0.3 V max	Go to 3C-4	Check Q32, R97, R99, Q28, CR34
	4	Collector Q33	+0.3 V max	Go to 3C-5	Check Q33, R101, R102, Q29, CR35
	5	Base Q31		Check Q31, CR33, Q27, R75	Check CR44, R74, R94, C22

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

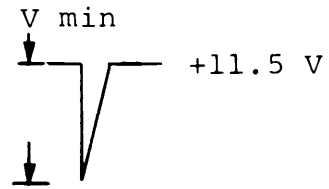
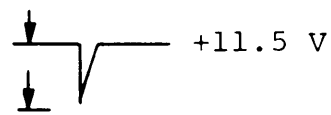
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A	1	A4-C	+11.5 V	Check connection at XA4-C	Check CR9
4B	1	A4-1		Check connection at XA4-1	If Lamp C is not lighted check CR11. If Lamp C is lighted go to 4B-2.
	2	Collector Q23		Check connection at XA4-F	Check Q23, R71, R70, R69, C21
4C	1	Anode of CR34	+11.5 V	Check connection at XA4-7. Go to 4C-2.	Go to 4C-2
	2	Collector Q30	+0.3 V max	Go to 4C-3	Check R89

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

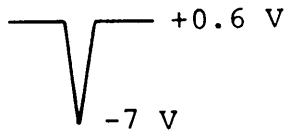
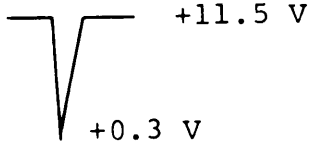
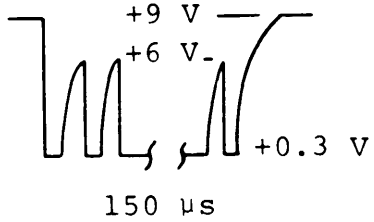
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4C (Cont)	3	Collector Q31	+0.3 V max	Go to 4C-4	Check R93
	4	Collector Q33	+0.3 V max	Go to 4C-5	Check Q33, R100, R102, Q29, CR35
	5	Base Q32		Check Q32, CR34, Q28, R77	Check CR45, R76, R99, C23
5A	1	Collector Q1		Check CR1	Check Q1, R3, R2, R1, C1. Lamp C may or may not be lighted.
5B	1	Collector Q8		Check connection between buffer A37 and TP7	Check Q10. Go to 5B-2.

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

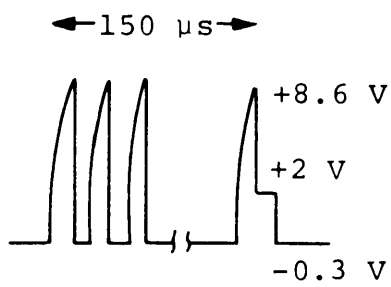
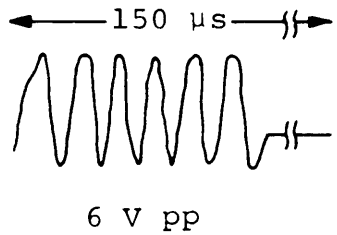
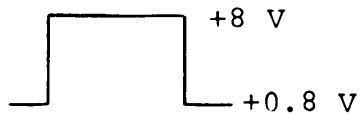
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5B (Cont)	2	Base Q9	-1 V	Go to 5B-3	Check R19, R20
	3	Collector Q7		Check Q8, R17, C8	Go to 5B-4
	4	Output A4A1 (Track to C7)		Check Q7, R16, R15, C7	Go to 5B-5
	5	Input A4A1 (Track from R11)		Replace A4A1 module	Check track & connection from Q5 emitter to A4A1 input

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

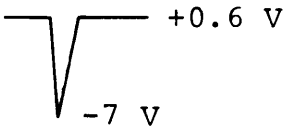
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5C	1	Anode CR35	+11.5 V	Check connection at XA4-6. Go to 5C-2	Go to 5C-2
	2	Collector Q30	+0.3 V max	Go to 5C-3	Check R90
	3	Collector Q31	+0.3 V max	Go to 5C-4	Check R95
	4	Collector Q32	+0.3 V max	Go to 5C-5	Check R98
	5	Base Q33		Check Q33, CR35, Q29, R79	Check CR46, R78, R102, C15

Table 5-10. Encloder Clock (A4), Fault Isolation Procedure (Cont)

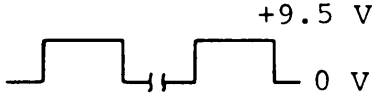
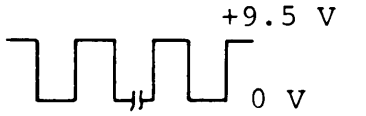
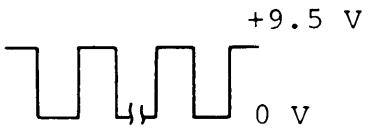
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6A	1	A4-13		Check connection at XA4-13. Go to 6A-2.	If Lamp B is not lighted, go to 6A-3. If Lamp B is lighted, go to 6A-4.
	2	A4-T		Check connection at XA4-T	Check Q37, Q38, CR68, CR67, CR66, R115, R116, R117, R118, R119, R120, R121, R122, R130, C37, C38, C39, C40
	3	Emitter Q36		Check R134, Q41	Check Q36, R114, R113, C36
	4	Collector Q34		Check connection at XA4-13	Check Q34, Q35, CR55, CR54, CR53, R104, R105, R106, R107, R108, R109, R110, R111, R129, C29, C30, C31, C32

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

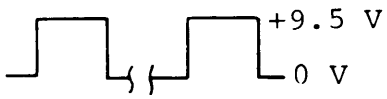
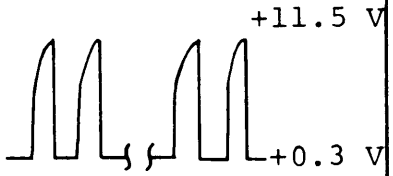
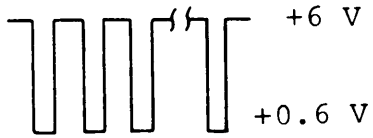
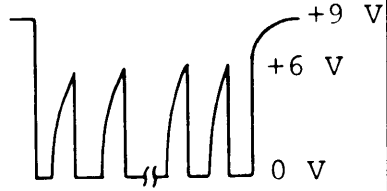
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B	1	A4-T		Check connection at XA4-T	Check Q38, Q37, CR68, CR67, CR66, R115, R116, R117, R118, R119, R120, R121, R122, R130, C37, C38, C39, C40
6C	1	Collector Q11		Check connection between buffer A37 and TP-6	Go to 6C-2
	2	Collector Q10		Check Q11, R25, R24, C10, CR25	Check Q10, R22, R21, R23, C9
7A	1	Collector Q8		Check connection between buffer A37 and TP-7	If Lamp B is lighted go to 7B-1. If Lamp B is not lighted check Q9, R20, R19.

Table 5-10, Encoder Clock (A4), Fault Isolation Procedure (Cont)

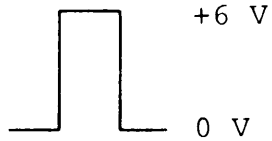
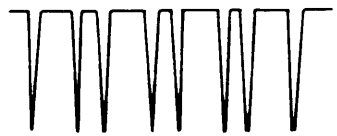
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVFFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7B	1	Collector Q14		Check connection between buffer A37 and TP5	Check Q14, Q13, Q12, CR8, R26, R27, R28, R29, R30, R31, R32, R33, R34
7C	1		Adjust A4A1C1 until Lamp C turns off		Go to 7C-2
	2	Collector Q20	+11.5 V 	Check connection between buffer A37 and TP4. Go to 7C-5.	Go to 7C-3
	3	Emitter Q19		Check Q20, CR78, R61, R60, R59	Go to 7C-4

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

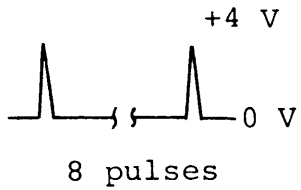
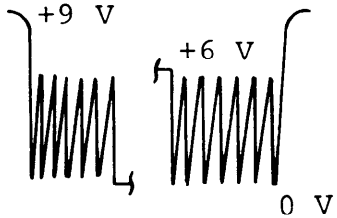
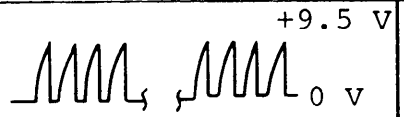
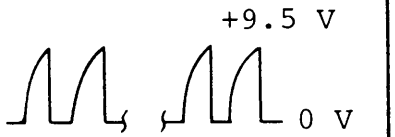
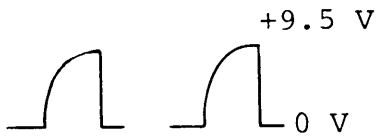
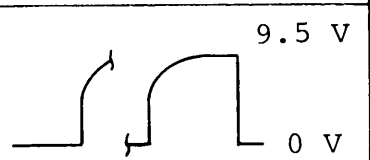
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7C (Cont)	4	Base Q19		Check Q19	Go to 7C-5
	5	Collector Q8		This waveform given as a timing reference in succeeding steps	
	6	Collector Q17		Go to 7C-7	Go to 8A-4
	7	Collector Q25		Go to 7C-8	Go to 8A-5
	8	Collector Q35		Go to 7C-9	Go to 8A-6
	9	Collector Q38		Replace Clock Module A4A1	Go to 8A-7

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
	8.	THE FOLLOWING WAVEFORMS ARE USED AS A TIMING REFERENCE IN TEST SEQUENCE 8.			

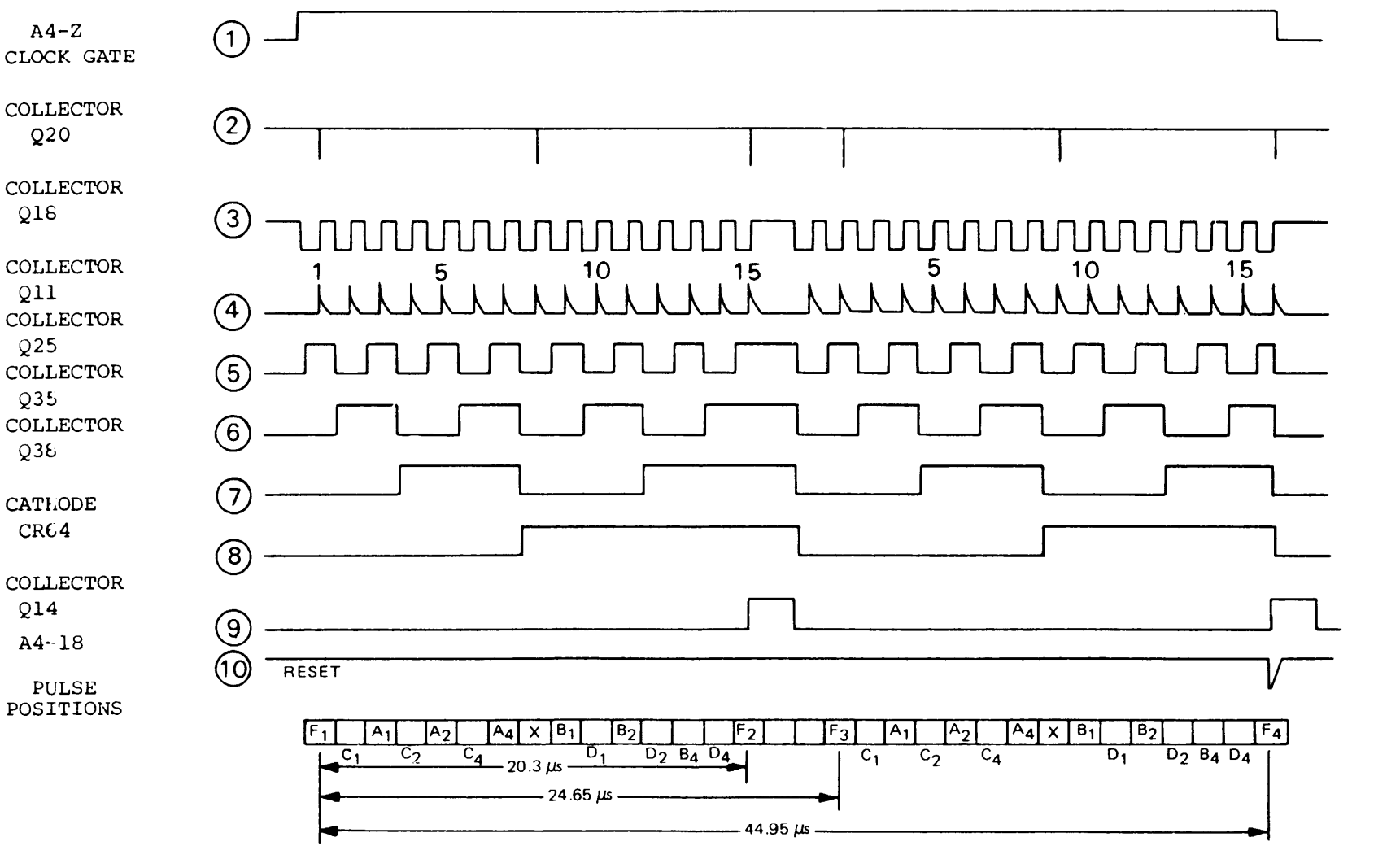


Table 4-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM	
8A	1	A4-Z	①	Check connection at XA4-Z	If Lamp B is not lighted go to 8A-2. If Lamp B is lighted go to 8B-1.	
	2	Base Q2	⑩	Check CR3	Go to 8A-3	
	3	A4-18	⑩	Check track to cathode CR3	Go to 8A-4	
	4	Collector Q18	③	Go to 8A-5	Check 2^0	
					0 Side Q18,R46,47, 48,49,C18, 19,CR15,16	1 Side Q17,R127,R42, 43,44,45,C16, 17,CR12,14

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM	
8A	5	Collector Q25	⑤	Go to 8A-6	Check 2[1]	
					0 Side Q24,R81,82,83, R84,C24,25, CR36,37	1 Side Q25,R128,R84, 85,86,87,C26, 27,CR38
	6	Collector Q35	⑥	Go to 8A-7	Check 2[2]	
					0 Side Q34,R104,105, 106,107,C29, 30,CR53,54	1 Side Q35,R129,R108, 109,110,111, C31,32,CR55
	7	Collector Q38	⑦	Go to 8A-8	Check 2[3]	
					0 Side Q37,R115,116, 117,118,C37, 38,CR66,67	1 Side Q38,R130,R119, 120,121,122, C39,40,CR68

Table 5-10, Encoder Clock (A4), Fault Isolation Procedure Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8A (Cont)	8	A4-T	(7)	Go to 8A-9	Check track to collector Q38
	9	A4-13	Same as (6) except pulses in first frame only	Check connection at XA4-13	Check Q41, Q36, R134, R113, R114, C36
8B	1	Collector Q14	(9)	Check connection between buffer A37 and TP5	1. Extra pulse at A4 in first frame, reset at A4 in second frame: Replace CR52. 2. Extra pulse at B2 in first frame, reset at B2 in second frame: Replace CR65. 3. Extra pulse at B4 in first frame, reset at B4 in second frame: Replace CR51. 4. Extra pulse at D4 in first frame, reset at D4 in second frame: Replace CR31. 5. No F2 pulse in first frame, reset at F2 in second frame: Replace CR7.

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

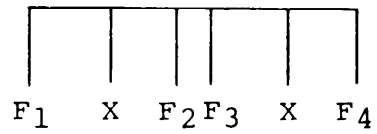
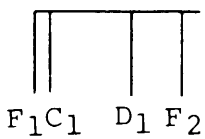
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8C	1	Collector Q20	② 	Check connection between buffer A37 and TP4	By comparison with the reference frame, identify the abnormal pulse/pulses. 1. X Pulse missing: Check Q39,CR73,CR74,R123, R124,R125 2. Extra pulse between F2,F3: Replace CR64. 3. B1 present: Replace CR30. 4. C1, D1 present: Replace CR50. 5. C2 D2 present: Replace CR63.
9C	1	Collector Q20		Check connection between buffer A37 and TP4	By comparison with the reference frame, identify the abnormal pulse/pulses. 1. X Pulse present: Check/Replace CR76, CR56. 2. A1, B2 present: Replace CR27. 3. C4, D4 present: Replace CR61.

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

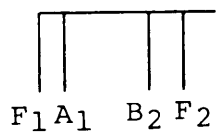
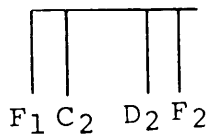
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10C	1	Collector Q20		Check connection between buffer A37 and TP4	By comparison with the reference frame, identify the abnormal pulse/pulses. 1. C1, D1 present: Replace CR40. 2. B1 present: Replace CR57. 3. A4 present: Replace CR62.
11C	1	Collector Q20		Check connection between buffer A37 and TP4	By comparison with the reference frame, identify the abnormal pulse/pulses. 1. A4, B4 present: Replace CR28. 2. C4, D4 present: Replace CR48. 3. X Pulse present: Replace CR69.

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

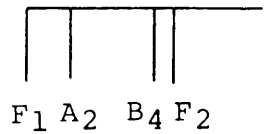
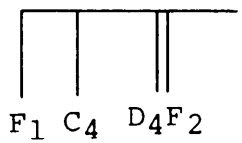
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12C	1	Collector Q20		Check connection between buffer A37 and TP4	By comparison with the reference frame, identify the abnormal pulse/pulses. 1. C2, D2 present: Replace CR41. 2. A4 present: Replace CR49. 3. B1 present: Replace CR70.
13C	1	Collector Q20		Check connection between buffer A37 and TP4	By comparison with the reference frame, identify the abnormal pulse/pulses. 1. A4 present: Replace CR29. 2. C2, D2 present: Replace CR58. 3. C1, D1 present: Replace CR71.

Table 5-10. Encoder Clock (A4), Fault Isolation Procedure (Cont)

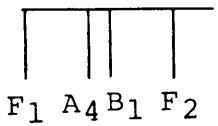
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
14C	1	Collector Q20		Check connection between buffer A37 and TP4	By comparison with the reference frame, identify the abnormal pulse/pulses. 1. C4, D4 present: Replace CR42. 2. A2, B4 present: Replace CR59. 3. A1, B2, D4 present: Replace CR72. 4. A1, B2 present: Replace CR47. 5. A2, B4 present: Replace CR60. 6. X Pulse present. Replace CR39.
15C	1	Collector Q20	+12 V	Check connection between buffer A37 and TP4	Go to 15C-2
	2	Collector Q40	+0.3 V max	Check Q22, R131, R132, R133	Go to 15C-3
	3	A4-11	+4.8 V	Check Q40, R66, R67, R68	Check connection at XA4-11

Table 5-11. Encoder Control (A5), Fault Isolation Procedure

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	A5-66	+7.9 V min	Check connection at XA5-66	Switch to position 8, if A&C faults indicated, check CR20. If no faults in position 8, check Q2.
1B	1	A5-33	+7.9 V min	Check connection at XA5-33	Observe indicator F. If fault is indicated check Q1. If no indicator F fault, check CR12.
1F	1	A5-41	+7.9 V min	Check connection at XA5-41	Check CR11
1G	1	A5-23, 24,25,57, 58,59	With board out of socket, 68K ohms from each terminal to A1Q1 collector with positive lead of ohm-meter on terminal.	Check connection at XA5-23,24,25, 57,58,59	Replace A1

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A	1	A5-66	+7.9 V min	Check connection at XA5-66	Fault is either A2Q1 or A2CR2. Replace A2.
2B	1	A5-33	+7.9 V min	Check connection at XA5-33	Fault is neither A1Q1 or A1CR2. Replace A1 (indicator F may also show fault.)
2F	1	A5-41	+7.9 V min	Check connection at XA5-41	Check CR21
2G	1	A5-20,21, 22,53,54, 55	With board out of socket, 68K ohms from each terminal to A2Q1 collector with positive lead of ohm-meter on terminal.	Check connection at XA5-20,21,22, 53,54,55	Replace A2

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A	1	A5-66	+7.9 V min	Check connection at XA5-66	Fault is either A4Q1 or A4CR2. Replace A4.
3B	1	A5-33	+7.9 V min	Check connection at XA5-33	Fault is either A3Q1 or A3CR2. Replace A3 (indicator F may also show fault)
3F	1	A5-41	+7.9 V min	Check connection at XA5-41	Check CR22
3G	1	A5-17, 18, 19, 50, 51, 52	With board out of socket, 68K ohms from each terminal to A3Q1 collector with positive lead of ohm-meter on terminal.	Check connection at XA5-17,18,19, 50,51,52	Replace A3

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A	1	A5-66	+7.9 V min	Check connection at XA5-66	Check Q4 and CR29
4B	1	A5-33	+7.9 V min	Check connection at XA5-33	Observe indicator F. If fault is indicated, check Q3. If indicator F does not indicate fault, check CR26.
4F	1	A5-41	+7.9 V min	Check connection at XA5-41	Check CR27
4G	1	A5-13,14, 15,47,48, 49	With board out of socket, 68K ohms from each terminal to A4Q1 collector with positive lead of ohm-meter on terminal.	Check connection at XA5-13,14,15, 47,48,49	Replace A4

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5B	1	A5-2	+7.9 V min	Check connection at XA5-2	Check CR19
5C	1	A5-10	+7.9 V min	Check connection at XA5-10	Fault is A2-CR1. Replace A2.
5D	1	A5-16	+7.9 V min	Check connection at XA5-16	Fault is A4-CR1. Replace A4.
5E	1	A5-63	+7.9 V min	Check connection at XA5-63	Check CR28
5G	1	A5-30	+7.9 V min	Check connection at XA5-30	Check CR24

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B	1	A5-2	+7.9 V min	Check connection at XA5-2	Check CR10
6C	1	A5-10	+7.9 V min	Check connection at XA5-10	Faults A1-CR1. Replace A1.
6D	1	A5-16	+7.9 V min	Check connection at XA5-16	Fault is A3-CR1. Replace A3.
6E	1	A5-63	+7.9 V min	Check connection at XA5-63	Check CR25
6G	1	A5-30	+7.9 V min	Check connection at XA5-30	Check CR23

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

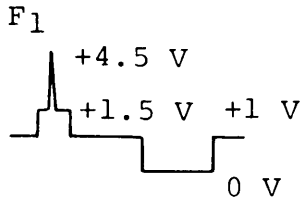
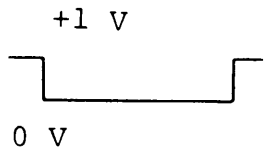
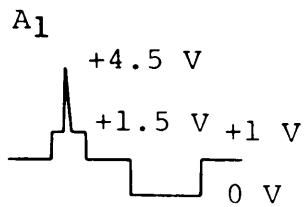
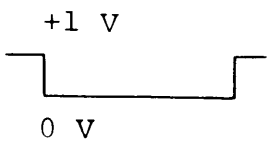
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A	1	TP7		Check connection at XA5-3	Check Q2, Q5, CR16
7B	1	TP2		Check connection at XA5-38	Check Q6, R83
7C	1	TP3		Check connection at XA5-37	Observe indicators. If C,E,G show fault, check CR25,CR11. If only C shows fault, observe waveform at TP3. If no pulses check Q7,CR1. If two pulses check CR17.
7D	1	TP8		Check connection at XA5-34	Check Q8, R82

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

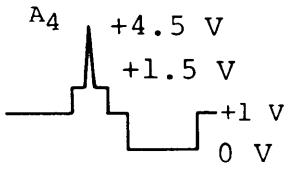
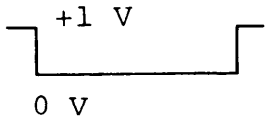
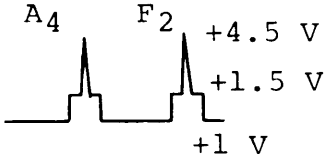
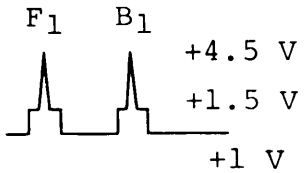
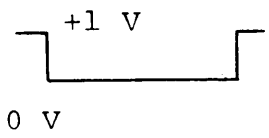
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7E	1	TP4		Check connection at XA5-36	If no pulses Q9, CR2. If two pulses Q9, CR18.
7F	1	TP5		Check connection at XA5-35	Check Q10, R81
7G	1	TP10		Check connection at XA5-4	If no pulses Q11. If one pulse CR3.
8A	1	TP7		Check connection at XA5-3	Check CR4
8B	1	TP2		Check connection at XA5-38	Check Q6,R83 (Previously checked in Step 7B)

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

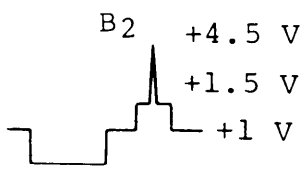
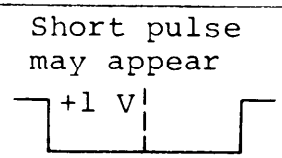
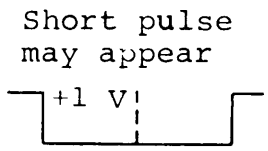
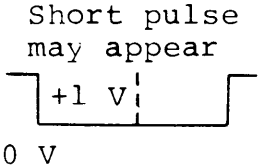
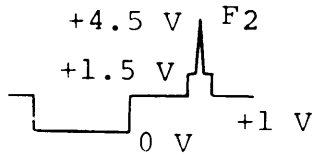
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8C	1	TP3		Check connection at XA5-37	If no pulses, CR5. If two pulses, Q1, CR13.
8D	1	TP8		Check connection at XA5-34	Check Q8,R82. (Previously checked in Step 7D)
8E	1	TP4		Check connection at XA5-36	Check CR14
8F	1	TP5		Check connection at XA5-35	Check Q10,R81. (Previously checked in 7F).
8G	1	TP10		Check connection at XA5-4	Check CR15

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

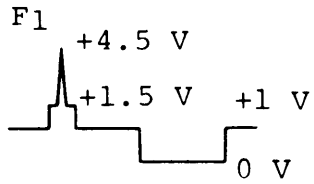
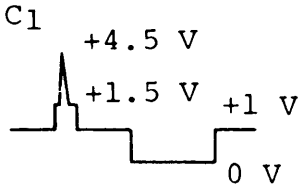
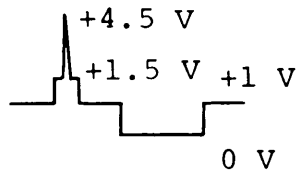
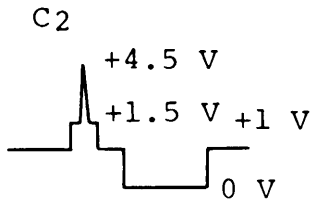
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A	1	TP7		Check connection at XA5-3	Fault is A2-Q1 or A2-CR3. Replace A2.
9B	1	TP2		Check connection at XA5-38	If two pulses, fault is A2-Q1 or A2-CR4, replace A2. If no pulses, fault is A1-CR9, replace A1.
9C.	1	TP3		Check connection at XA5-37	If two pulses, fault is A2-CR5, replace A2. If no pulses, fault is A1-CR10, replace A1.
9D	1	TP8		Check connection at XA5-34	If two pulses, fault is A2-CR6, replace A2. If no pulses, check Q8. If good, fault is A1-CR11 replace A1.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

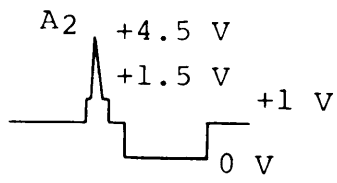
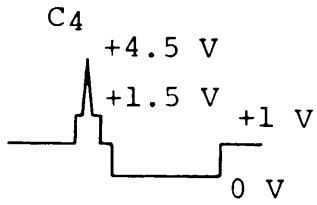
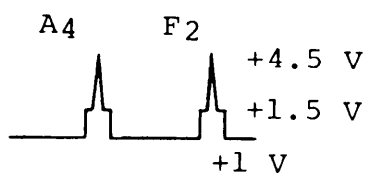
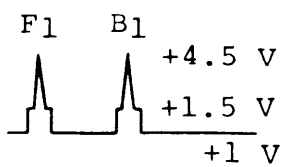
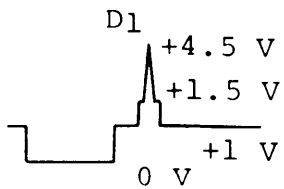
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9E	1	TP4		Check connection at XA5-36	If two pulses, fault is A2-CR7, replace A2. If one pulse, fault is A1-CR12, replace A1.
9F	1	TP5		Check connection at XA5-35	If two pulses, fault is A2-CR8, replace A2. If one pulse, check Q10. If good, fault is A1-CR13. Replace A1.
9G	1	TP10		Check connection at XA5-4	Fault is A1-CR14, replace A1
10A	1	TP7		Check connection at XA5-3	Fault is A2-CR9, replace A2
10B	1	TP2		Check connection at XA5-38	If two pulses, fault is A1-Q1 or A1-CR3 replace A1. If no pulses, fault is A2-CR9 replace A2.

Table 5-11. Encoder Control (A5), Fault Isoalation (Cont)

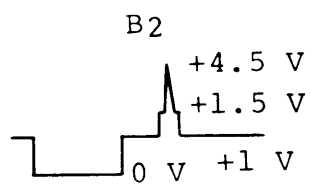
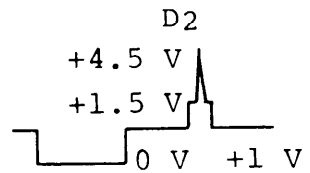
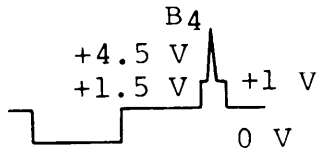
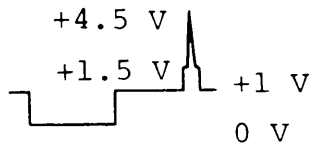
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10C	1	TP3		Check connection at XA5-37	If two pulses, fault is A1-CR4, replace A1. If no pulses, fault is A2-CR11, replace A2.
10D	1	TP8		Check connection at XA5-34	If two pulses, fault is A1-CR5 replace A1. If no pulses, fault is A2-CR12, replace A2.
10E	1	TP4		Check connection at XA5-36	If two pulses, fault is A1-CR6, replace A1. If no pulses, fault is A2-CR12 replace A2.
10F	1	TP5		Check connection at XA5-35	If two pulses, fault is A1-CR7, replace A1. If no pulses, fault is A2-CR14, replace A2.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

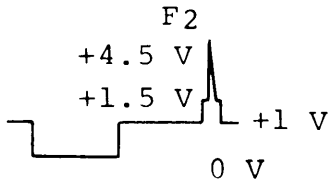
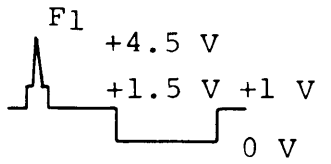
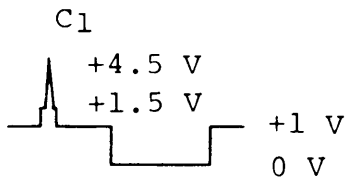
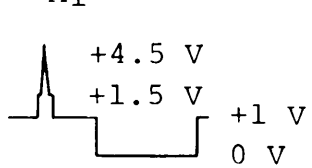
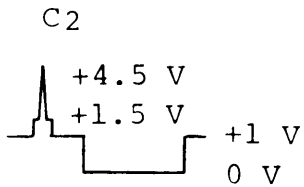
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10G	1	TP10		Check connection at XA5-4	Fault is A1-CR8; replace A1.
11A	1	TP7		Check connection at XA5-3	Fault is A4-Q1 or A4-CR3; replace A4.
11B	1	TP2		Check connection at XA5-38	If two pulses, fault is A4-CR4, replace A4. If no pulses, fault is A3-CR9. Replace A3.
11C	1	TP3		Check connection at XA5-37	If two pulses, fault is A4-CR5, replace A4. If no pulse, fault is A3-CR10, replace A3.
11D	1	TP8		Check connection at XA5-34	If two pulses, fault is A4-CR6, replace A4. If no pulse, fault is A3-CR11. Replace A3.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

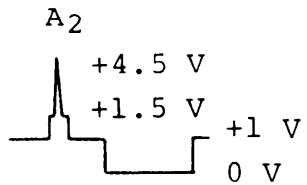
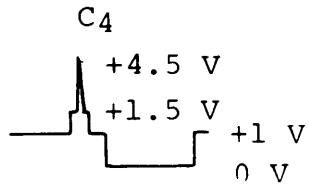
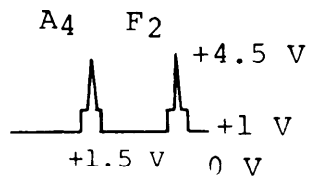
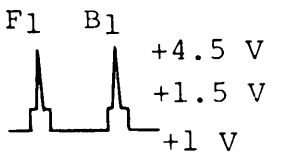
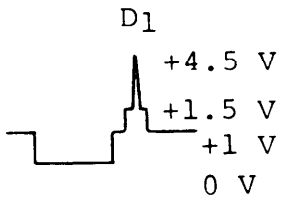
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
11E	1	TP4		Check connection at XA5-36	If two pulses, fault is A4-CR7, replace A4. If no pulse, fault is A3-CR12, replace A3.
11F	1	TP5		Check connection at XA5-35	If two pulses, fault is A4-CR8, replace A4. If no pulse, fault is A3-CR13, replace A3.
11G	1	TP10		Check connection at XA5-4	Fault is A3-CR14; replace A3.
12A	1	TP7		Check connection at XA5-3	Fault is A4-CR9; replace A4.
12B	1	TP2		Check connection at XA5-38	If two pulses, fault is A3-Q1 or A3-CR3. Replace CR3. If no pulse, fault is A4-CR10, replace A4.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

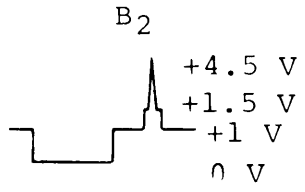
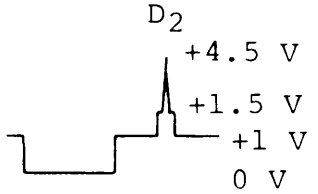
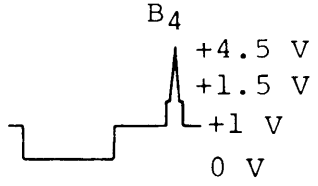
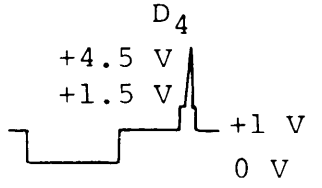
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
12C	1	TP3		Check connection at XA5-37	If two pulses, fault is A3-CR4. Replace A3. If no pulse, fault is A4-CR11, replace A4.
12D	1	TP8		Check connection at XA5-34	If two pulses, fault is A3-CR5. Replace A3. If no pulse, fault is A4-CR12, replace A4.
12E	1	TP4		Check connection at XA5-36	If two pulses, fault is A3-CR6, replace A3. If no pulse, fault is A4-CR13. Replace A4.
12F	1	TP5		Check connection at XA5-35	If two pulses, fault is A3-CR7. Replace A3. If no pulse, fault is A4-CR14, replace A4.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

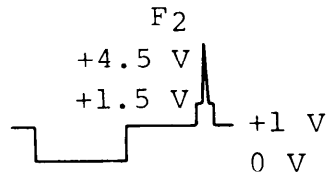
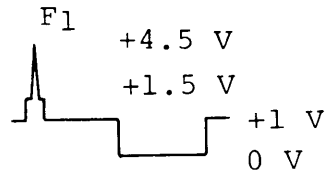
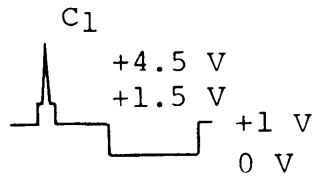
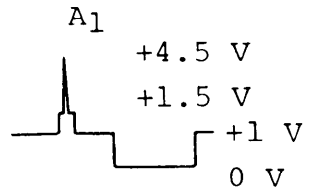
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	* ACTION FOR ABNORMAL WAVEFORM
12G	1	TP10		Check connection at XA5-4	Fault is A3-CR8, replace A3.
13A	1	TP7		Check connection at XA5-3	Check Q4, CR47
13B	1	TP2		Check connection at XA5-38	If two pulses, check CR48, R28. If no pulse, check CR30,C2,R56,R34.
13C	1	TP3		Check connection at XA5-37	If two pulses, check CR49, R29. If no pulse, check CR31,C3,R57,R35.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

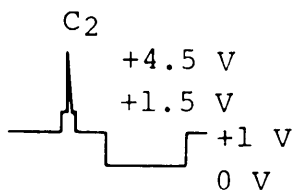
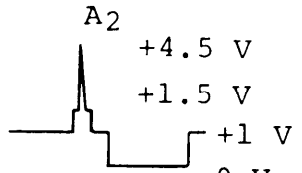
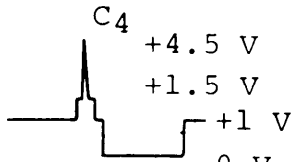
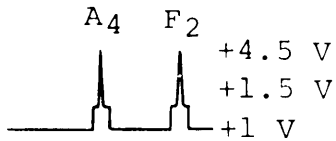
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
13D	1	TP8		Check connection at XA5-34	If two pulses, check CR50, R30. If no pulse, check CR32,C4,R58,R36.
13E	1	TP4		Check connection at XA5-36	If two pulses, check CR51, R31. If no pulse, check CR33,C5,R59,R37.
13F	1	TP5		Check connection at XA5-35	If two pulses, check CR52, R32. If no pulses, check CR34,C6,R60, R38.
13G	1	TP10		Check connection at XA5-4	Check CR35, C7, R61, R39.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

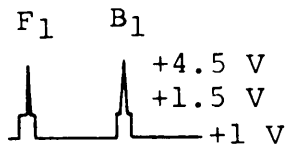
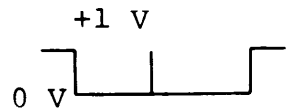
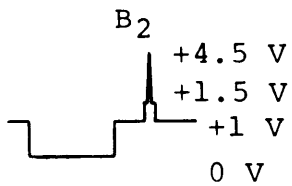
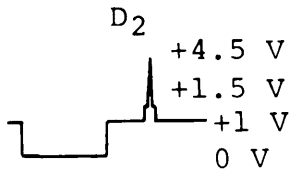
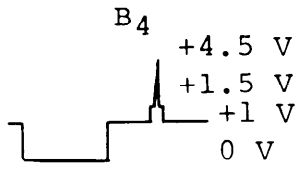
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
14A	1	TP7		Check connection at XA5-3	Check CR36, C8, R62, R40
14B	1	TP2		Check connection at XA5-38	Check CR41, R21
14C	1	TP3		Check connection at XA5-37	If two pulses, check CR42, R22. If no pulse, check CR37, C9, R63, R41.
14D	1	TP8		Check connection at XA5-34	If two pulses, check CR43, R23. If no pulse, check CR38, C10, R64, R42.
14E	1	TP4		Check connection at XA5-36	If two pulses, check CR44, R24. If no pulse, check CR39, C11, R65, R43.

Table 5-11. Encoder Control (A5), Fault Isolation Procedure (Cont)

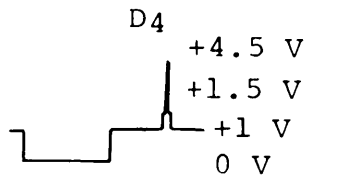
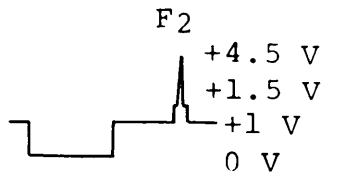
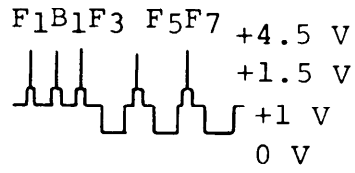
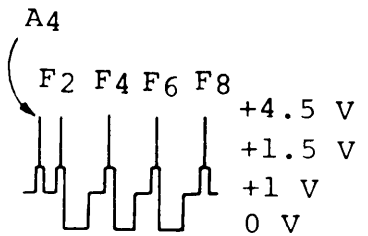
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
14F	1	TP5		Check connection at XA5-35	If two pulses, check CR45, R25. If no pulse, check CR40,C12,R66,R44.
14G	1	TP10		Check connection at XA5-4	Check CR46, R26
15A	1	TP7		Check connection at XA5-3	Check CR7, CR8
		All circuits associated with 15B thru		15F previously checked	
15G	1	TP10		Check connection at XA5-4	Check CR6-CR9

Table 5-12. Encoder Gating (A6), Fault Isolation Procedure for RT859/APX-72

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A	1	Collector Q5	+0.3 V max	Check connection between buffer A38 and TP2	Go to 1A2
	2	Anode CR9	+5.1 V	Check Q5	Check Q5, CR9, R19, R20, R21, C9
1B	1	Collector Q19	+11.6 V	Check connection between buffer A38 and TP3	Go to 1B2
	2	Anode CR36	+0.2 V max	Check Q19, R73, R74	Check CR36. If good, go to 1B3.
	3	Collector Q20	+0.3 V max	NA	Check CR40, Q20. If good, ground the collector of Q20 and go to 1B4.

Table 5-12. Encoder Gating (A6), Fault Isolation Procedure for RT-859/APX-72 (Cont)

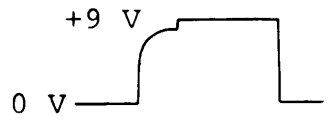
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1B	4	Collector Q21	+15 V	Check R80, R78	Check CR39, Q21. If good, leave the ground at Q20 collector on and proceed with remainder of Test Sequences 1 through 7. Trouble-shooting of this circuit is continued when Test Sequence 8 is performed.
1C	1	Cathode CR8	+11.8 V	Check connection between buffer A38 and TP8	Go to 1C2
	2	Collector Q11	+11.8 V	Check R51	Check C15, CR26, CR24
2A	1	A6-21		Go to 2A-2	Check connection at XA6-21
	2	Collector Q17		Check connection at XA6-20	Temporarily open Q16 collector and go to 2A3

Table 5-12. Encoder Gating (A6), Fault Isolation Procedure for RT-859/APX-72 (Cont)

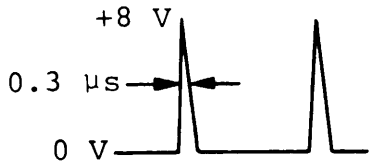
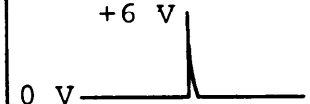
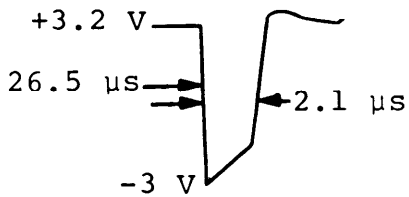
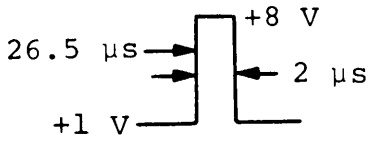
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A	3	Collector Q17		Check Q16, CR30, CR31, R64, R62, C20. Restore open connection.	Check Q17, CR32, R65, R96, R60, R61, R63, C21, C18, C19. Restore open connection.
2B	1	Collector Q9		Check connection between buffer A38 and TP6	Check Q8, Q9, CR17, CR19, R36, R37, R38, R39, R40, R41, R42, R95, C11, C12
2C	1	Collector Q1	+10.0 V	Check connection between buffer A38 and TP7	Check Q1, Q2, CR1, CR3, R1, R2, R3, R4, R5, R6, R7, R8, R94, C3, C4, C5, C6
3A	1	Cathode CR3		Check connection at XA6-T	If pulse present but wrong DC level, check R10-R13. If pulse width wrong or no pulse, go to 3A2.
	2	Anode CR7		Check Q3, Q4, CR41, R9, R11, R12, R14, R16, R91, R15, R17, R18, CR8, C16, CR28	Go to 3A3

Table 5-12. Encoder Gating (A6), Fault Isolation Procedure for RT-859/APX-72 (Cont)

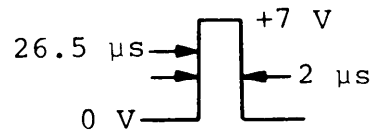
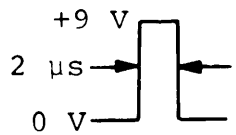
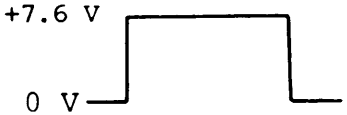
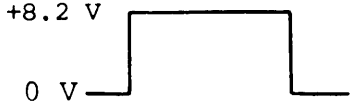
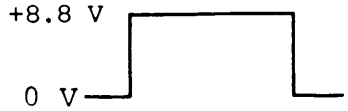
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A (Cont)	3	Cathode CR7		Check CR7	Check connection at XA6-U
3B	1	Collector Q14	0.3 V max	Check connection between buffer A38 and TP4	Go to 3B2
	2	Collector Q15		Check Q14, R34, R32	Check Q15, CR29, R30, R93, R31, R33, R35, R92
3C	1	Emitter Q6		Check connection at XA6-F	Go to 3C2
	2	Base Q6		Check Q6	Go to 3C3
	3	Anode CR13		Check CR13	Check CR10, CR11

Table 5-12. Encoder Gating (A6) , Fault Isolation Procedure for RT-859/APX-72 (Cont)

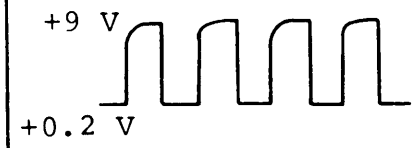
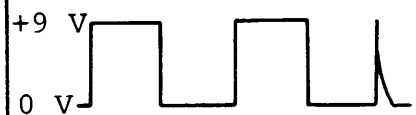
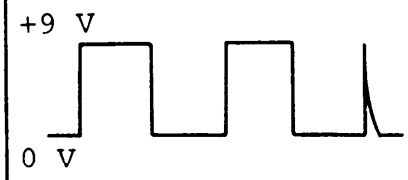
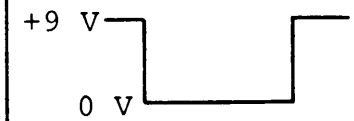
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A	1	Collector Q17		Go to 4A2	Check connection at XA6-21
	2	Collector Q9		Check connection between buffer A38 and TP6	Temporarily open Q8 collector and go to 4A3
	3	Collector Q9		Check Q8, CR17, CR19, R41, R39, C13	Check Q9, CR18, CR20, CR22, R37, R42, R95, R38, R40, C11, C12. Reconnect Q8 connector.
4B	1	Collector Q9		Check connection between buffer A38 and TP6	NA (See 4A2)
	2	Collector Q1		Check connection between buffer A38 and TP7.	Temporarily open Q2 collector. Go to 4B3.

Table 5-12. Encoder Gating (A6), Fault Isolation Procedure for RT-859/APX-72 (Cont)

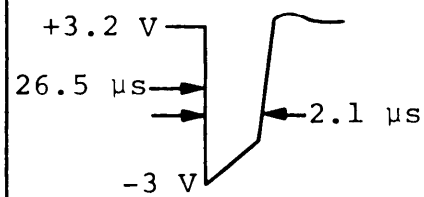
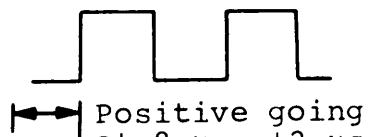
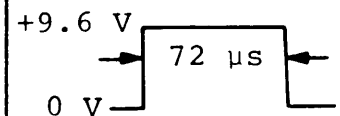
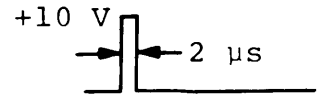
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4B	3	Collector Q1		Check Q2, CR2, CR4, R3, R5, C6, R8	Q1, CR1, CR3, R2, R7, R94, R6, R4, C5, C3, C4. Reconnect Q2 collector.
5C	1	Cathode CR3		Check connection at XA6-T	Go to 5C2
	2	TP6		Check CR6, CR7	Check CR22, R26, R25
6A	1	Collector Q14		Check connection between buffer A38 and TP4	Note whether abnormal waveform is 12 V or 0 V. If 12 V, check Q7 and if good, go to 6A2. If 0 V, open Q14 collector and go to 6A2.
	2	Collector Q15		Check Q14, CR28, C16	Check connection at XA6-T. Check Q15, CR29, R30, R93, R31, R33. Reconnect Q14 collector.

Table 5-12. Encoder Gating (A6. Fault Isolation Procedure for RT-859/APX-72 (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6B	1	Emitter Q6	+7.6 V, 0 V, 72 µs	Check connection at XA6-F	Go to 6B2
	2	Base Q6	+8.3 V, 0 V, 72 µs	Check Q6	Check Q6, if good go to 6B3
	3	Emitter Q7	+8.9 V, 0 V, 72 µs	Check CR10 If good, go to 6B4	Check Q7 and track
	4	Collector Q5	+0.3 V max	Check CR15	Check Q5
6C	1	Anodes CR14, CR15, CR16	+4 V, 31 µs, +0.8 V, 72 µs (At all anodes)	Check connection at XA6-M and -15 & -16. Check track from CR14 to XA6-M, CR15 to XA6-15, CR16 to XA6-16	Replace diode which has abnormal waveform

Table 5-12, Encoder Gating (A6), Fault Isolation Procedure for RT-859/APX-72 (Cont)

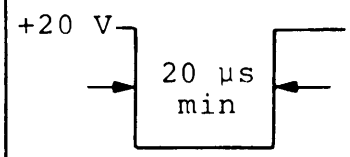
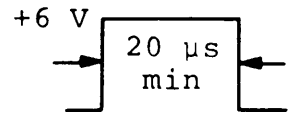
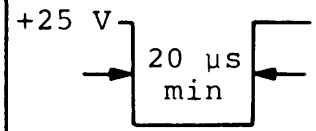
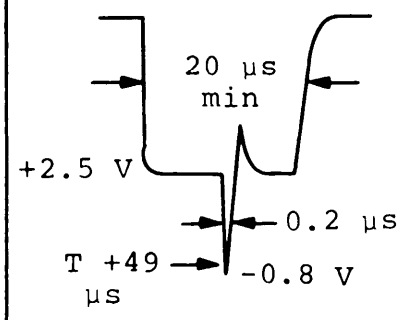
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A	1	Collector Q12		Check connection at XA6-14	Check CR27, if good go to 7A2
	2	Collector Q13		Check Q12, R56, R54	Go to 7A-3
	3	Base Q13		Check Q13	If baseline more positive than .6 V, check Q13. If no pulse, go to 7A4.
	4	XA6-13		Check C17, R71, R72, Q13	Check connection at XA6-13
7C	1	Cathode CR8		Check connection between buffer A38 and TP8	If 12 VDC, check connection at XA6-5. If connection is good go to 7C2. If wide portion of waveform present but no narrow pulse go to 7C3.

Table 5-12. Encoder Gating (A6) Fault Isolation Procedure for RT-859/APX-72 (Cont)

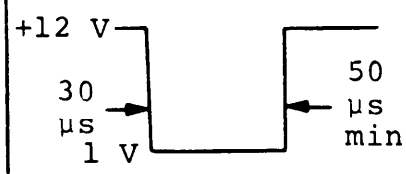
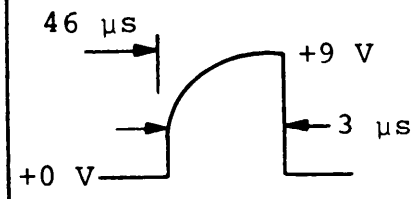
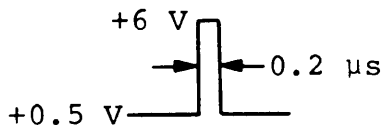
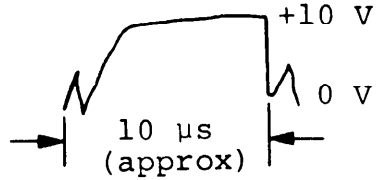
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7C	2	Collector Q11		Check R51	Check Q11, CR27, R55, R53
	3	Collector Q9		Go to 7C4	Check CR26
	4	Anode CR23		Check Q10, C15, R48, R49, R47, R45, R48, R44	Check CR21, CR23
8A	1	If, in Step 1B4, a ground was left on the collector of Q20, remove the ground, temporarily open the collector of Q21 and go to 8A3.			
	2	Emitter Q18	+0.3 V max	Check connection between buffer A38 and TP3	Temporarily open the collector of Q21 and go to 8A3
	3	Emitter Q18		Check Q21, CR38, CR39, R77, R79	Temporarily ground cathode of CR37 and go to 8A4

Table 5-12. Encoder Gating (A6), Fault Isolation Procedure for RT-859/APX-72 (Cont)

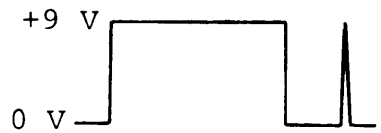
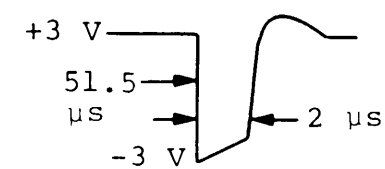
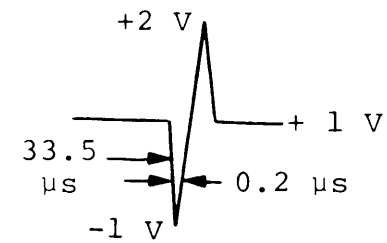
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8A	4	Collector Q20	+25 V	Go to 8A5	Check CR37, Q20. Correct, and restore connections at Q21 and CR37 to normal.
	5	Emitter Q18	+0.3 V max	Check C22, R89	Check Q19, Q18, R73, R75, R76. Correct and restore connections at Q21 and CR37 to normal.
8B	1	Collector Q9		Go to 8B2	Check CR20, R46, R70
	2	Collector Q1		Check connection between buffer A38 and TP7	Check CR2
8C	1	Cathode CR3		Check connection at XA6-7	Check CR6, CR5
9B	1	Cathode CR8		Check connection between buffer A38 and TP8	Go to 9B2

Table 5-12. Encoder Gating (A6) Fault Isolation Procedure for RT-859A/APX-72 (Cont)

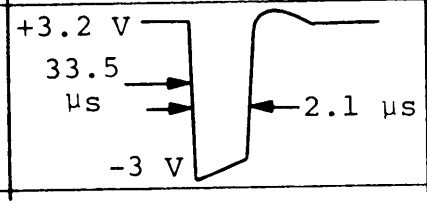
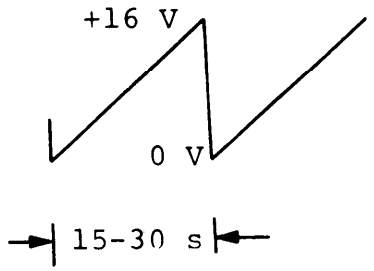
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9B	2	Collector Q18	+0.6 V max	CR24-CR25	Go to 9B3
	3	Cathode CR35	+1.2 V max	Check Q18	Check Q18. If good, go to 9B4.
	4	Cathode CR33	+5.4 V min	Check CR35, R67, R68	Go to 9B5
	5	Anode CR33	+6.0 V min	Check CR33, CR34	Check connection at XA6-K
9C	1	Cathode CR3		Check connection at XA6-T	Check CR8
10D		NOTE: If lamp 10D lights, rotate test switch to position 9 to perform the following analysis:			
	1	Emitter Q22		Check CR39, CR42, C23, R82	If sawtooth is present but time is wrong, check C24, RT1, R85, R90. If no sawtooth, check Q22, R84.

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A	1	Collector Q5	+0.3 V max	Check connection between buffer A38 and TP2	Go to 2A2
	2	Anode CR9	+5.1 V	Check Q5	Check Q5, CR9, R19, R20, R21, C9
2B	1	Collector Q19	+11.6 V	Check connection between buffer A38 and TP3	Go to 2B2
	2	Anode CR36	+0.2 V max	Check Q19, R73, R74	Check CR36. If good, go to 2B3.
	3	Collector Q20	+0.3 V max	NA	Check CR40, Q20, If good, ground the collector of Q20 and go to 2B4.
	4	Collector Q21	+15 V	Check R80, R78	Check CR39, Q21. If good, leave the ground at Q20 collector on and proceed with remainder of Test Sequences 1 through 8. Trouble-shooting of this circuit is continued when Test Sequence 9 is performed.
2C	1	Cathode CR8	+11.8 V	Check connection between buffer A38 and TP8	Go to 2C2
	2	Collector Q11	+11.8 V	Check R51	Check C15, CR25, CR24

Table 5-13. Encoder Gating (A6) Fault Isolation Procedure for RT-859A/APX-72, Cont)

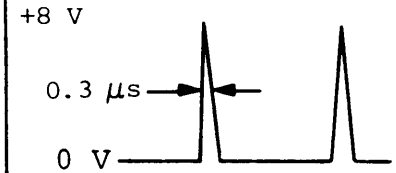
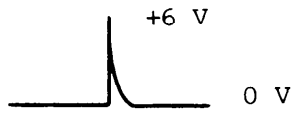
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A	1	A6-21		Go to 3A2	Check connection at XA6-21
	2	Collector Q17		Check connection at XA6-20	Temporarily open Q16 collector and go to 3A3
	3	Collector Q17		Check Q16, CR30, CR31, R64, R62, C20. Restore open connection.	Check Q17, CR32, R65, R96, R60, R61, R63, C21, C18, C19. Restore open connection.
3B	1	Collector Q9		Check connection between buffer A38 and TP6	Check Q8, Q9, CR17, CR19, R36, R37, R38, R39, R40, R41, R42, R95, C11, C12
3C	1	Collector Q1	+10 V	Check connection between buffer A38 and TP7	Check Q1, Q2, CR1, CR3, R1, R2, R3, R4, R5, R6, R7, R8, R94, C3, C4, C5, C6

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

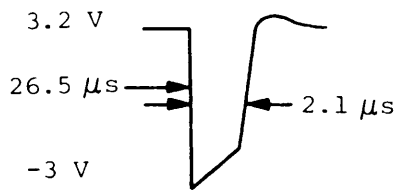
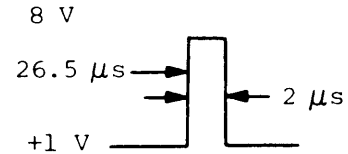
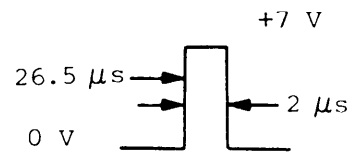
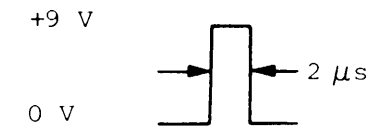
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4A	1	Cathode CR3		Check connection at XA6-T	If pulse present but wrong DC level, check R10-R13. If pulse width wrong or no pulse, go to 4A2.
	2	Anode CR7		Check Q3, Q4, CR41, R9, R11, R12, R14 R16, R91, R15, R17, R18, CR8, C16, CR28	Go to 4A3
	3	Cathode CR7		Check CR7	Check connection at XA6-U
4B	1	Collector Q14	+0.3 V max	Check connection between buffer A38 and TP4	Go to 4B2
	2	Collector Q15		Check Q14, R34, R32	Check Q15, CR29, R30, R93, R31, R33, R35, R92

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

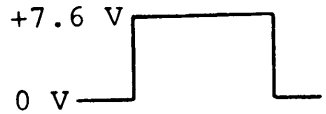
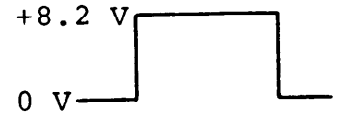
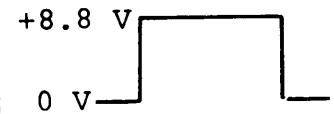
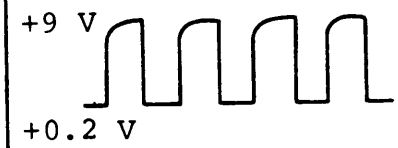
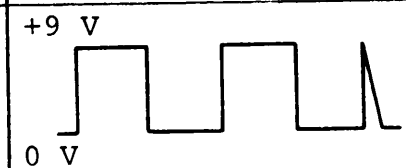
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
4C	1	Emitter Q6		Check connection at XA6-F	Go to 4C2
	2	Base Q6		Check Q6	Go to 4C3
	3	Anode CR13		Check CR13	Check CR10, CR11
5A	1	Collector Q17		Go to 5A2	Check connection at XA6-21
	2	Collector Q9		Check connection between buffer A38 and TP6	Temporarily open Q8 collector and go to 5A3

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

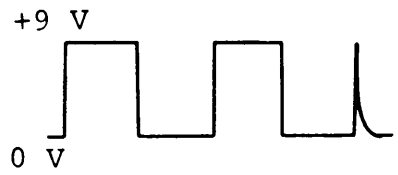
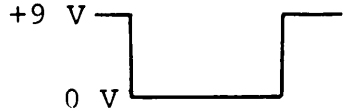
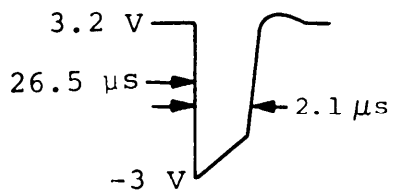
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
5A (Cont)	3	Collector Q9		Check Q8, CR17, CR19, R41, R39, C13	Check Q9, CR18, CR20, CR22, R37, R42, R95, R38, R40, C11, C12. Reconnect Q8 connector.
5B	1	Collector Q9		Check connection between buffer A38 and TP6	NA (See 5A2)
	2	Collector Q1		Check connection between buffer A38 and TP7	Temporarily open Q2 collector. Go to 5B3.
	3	Collector Q1		Check Q2, CR2, CR4, R3, R5, C6, R8	Q1, CR1, CR3, R2, R7, R94, R6, R4, C5, C3, C4. Reconnect Q2 collector.
6C	1	Cathode CR3		Check connection at XA6-T	Go to 6C2

Table 5-13, Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

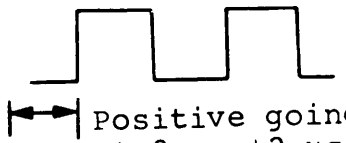
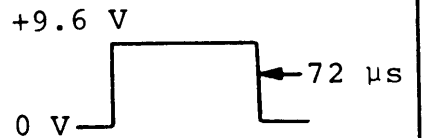
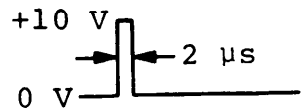
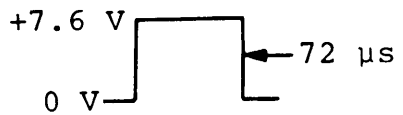
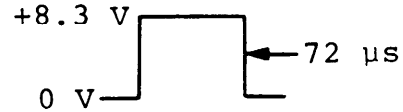
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6C (Cont)	2	TP6		Check CR6, CR7	Check CR22, R26, R25
7A	1	Collector Q14		Check connection between buffer A38 and TP4	Note whether abnormal waveform is 12 V or 0 V. If 12 V, check Q7 and if good, go to 7A2. If 0 V, open Q14 collector and go to 7A2.
	2	Collector Q15		Check Q14, CR28, C16	Check connection at XA6-T. Check Q15, CR29, R30, R93, R31, R33. Reconnect Q14 collector.
7B	1	Emitter Q6		Check connection at XA6-F	Go to 7B2
	2	Base Q6		Check Q6	Check Q6, if good go to 7B3

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

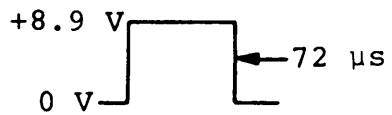
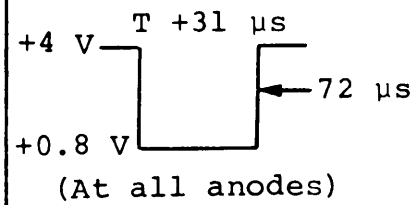
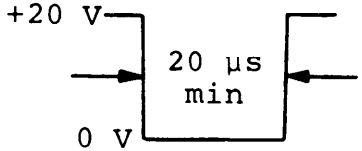
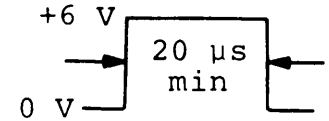
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7B (Cont)	3	Emitter Q7		Check CR10 If good, go to 7B4	Check Q7 and track
	4	Collector Q5		Check CR15	Check Q5
7C	1	Anodes CR14, CR15, CR16	 (At all anodes)	Check connection at XA6-M and -15 & -16. Check track from CR14 to XA6-M, CR15 to XA6-15, CR16 to XA6-16	Replace diode which has abnormal waveform
8A	1	Collector Q12		Check connection at XA6-14	Go to 8A2
	2	Collector Q13		Check Q12, R56, R54	Go to 8A3

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

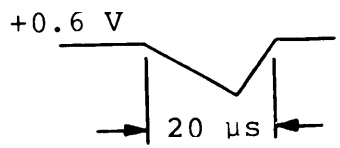
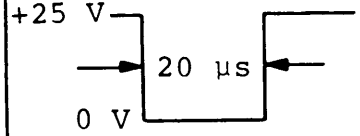
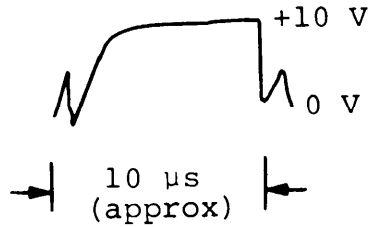
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
8A (Cont)	3	Base Q13		Check Q13	If baseline more positive than .6 V, check Q13. If no pulse, go to 8A4.
	4	XA6-13		Check C17, R71, R72, Q13	Check connection at XA6-13
9A	1	If, in Step 2B4, a ground was left on the collector of Q20, remove the ground, temporarily open the collector of Q21 and go to 9A3.			
	2	Emitter Q18	+0.3 V max	Check connection between buffer A38 and TP3	Temporarily open the collector of Q21 and go to 9A3
	3	Emitter Q18		Check Q21, CR38, CR39, R77, R79	Temporarily ground cathode of CR37 and go to 9A4

Table 5-13, Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

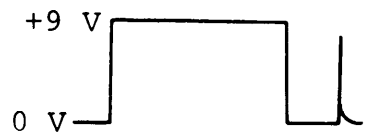
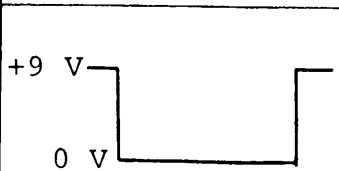
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9A	4	Collector Q20	+25 V	Go to 9A5	Check CR37, Q20. Correct, and restore connections at Q21 and CR37 to normal.
	5	Emitter Q18	+0.3 V max	Check C22, R89	Check Q19, Q18, R73, R75, R76. Correct and restore connections at Q21 and CR37 to normal.
9B	1	Collector Q9		Go to 9B2	Check CR20, R46, R70
	2	Collector Q1		Check connection between buffer A38 and TP7	Check CR2

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

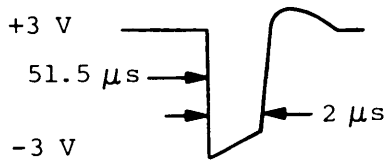
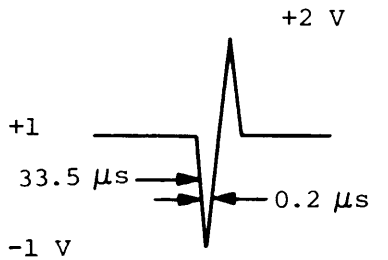
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
9C	1	Cathode CR3		Check connection at XA6-7	Check CR6, CR5
10B	1	Cathode CR8		Check connection between buffer A38 and TP8	Go to 10B2
	2	Collector Q18	+0.6 V max	CR24-CR25	Go to 10B3
	3	Cathode CR35	+1.2 V max	Check Q18	Check Q18. If good, go to 10B4
	4	Cathode CR33	+5.4 V min	Check CR35, R67, R68	Go to 10B5
	5	Anode CR33	+6.0 V min	Check CR33, CR34	Check connection at XA6-K

Table 5-13. Encoder Gating (A6), Fault Isolation Procedure for RT-859A/APX-72 (Cont)

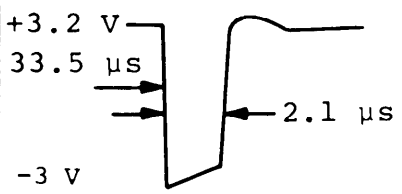
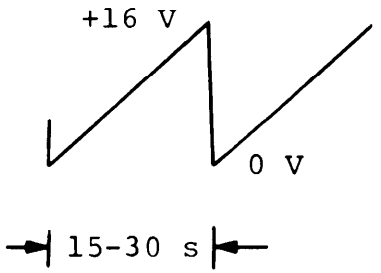
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10C	1	Cathode CR3		Check connection at XA6-T	Check CR8
11D		NOTE: If lamp 11D lights, rotate test switch to position 10 to perform the following analysis:			
	1	Emitter Q22		Check CR39, CR42, CR23, R82	If sawtooth is present but time is wrong, check C24, RT1, R85, R90. If no sawtooth, check Q22, R84.

Table 5-14. Modulator (A7), Fault Isolation Procedure

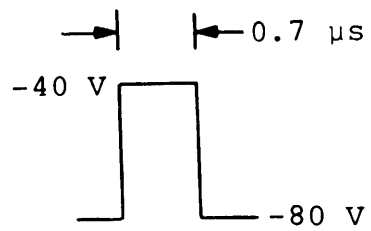
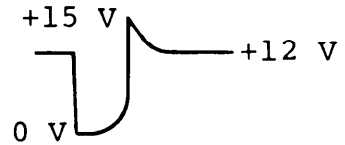
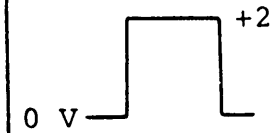
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1D	1	A7-8		Check connection at XA7-8	If no pulse, go to 1D2. If amplitude normal but width is incorrect, adjust R4 as required; if correction is not possible go to 1D6. If incorrect amplitude, go to 1D-4.
	2	A7-2		Go to 1D-3	Check connection at XA7-2.
	3	A7-8	Same as 1D1	Check connection at XA7-8	If -1 VDC, check Q5. If -80 V go to 1D-4.
	4	Base Q5		Check Q5, R18, R19	Check R17, R15, R16. If good, go to 1D-5
	5	Emitter Q4		Check T1, R14, C5	Go to 1A4

Table 5-14. Modulator (A7), Fault Isolation Procedure (Cont)

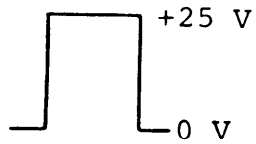
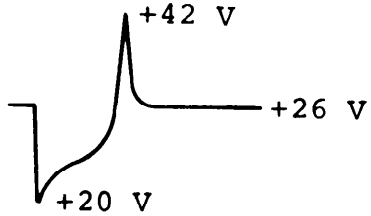
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1D (Cont)	6	Base Q4		Check Q4	Check Q4, R5, RT1. If good go to 1D7.
	7	Collector Q1		Check T-2, 6-5 secondary	Check T2, Q1, CR1, CR2, R2, R3, R4, R1, C2, C1

Table 5-15. Sensitivity (A8), Faut Isolation Procedure

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
Normal Sensi-tivity A	1	A8 Pin 5	0.6 V p-p, 100 kHz ripple max and +2.5 VDC max	Check Seating of pc board in test fixture	If 100 kHz ripple larger than 0.6 V p-p is observed, replace C2 and C3. If the dc voltage at Pin 5 is more positive than +2.5 VDC, place the test switch in low position and refer to Test Sequence Low-B1.
Normal Sensi-tivity B	1	A8 Terminal 7	+3.75 V min	Go to Normal-Sensitivity B-2	Go to Normal Sensitivity B-3
	2	A8 Terminal 8	+3.85 V min	Check Seating of pc board in test fixture	Check R1

Table 5-15. Sensitivity (A8), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
Normal Sensitivity B (Cont)	3	Junction R6 and relay contact A1	+5 V	Remove pc board from test fixture. Inspect R1 and R2 for damage. If good, adjust R6 to maximum clockwise position. Replace board in test fixture. If indicator B is still lighted, replace R6.	Go to Normal Sensitivity B-4
	4	A8 Terminal 4	+5 V	Go to Normal B5	If +5 VDC overload indicator is lighted, replace C4. If overload indicator is not lighted, check seating of pc board in test fixture.
	5	A8 Terminal 2	+25 V	Go to Normal Sensitivity B6	
	6	A8 Terminal 3	0 V (gnd)	Replace relay K1	Check seating of pc board in test fixture

Table 5-15. Sensitivity (A8) , Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
Low Sensitivity A	1	A8 Terminal 6	A dc voltage +2.4 V to +3.8 V	Check seating of pc board in test fixture	For future use note whether the voltage is high or low compared to the Normal waveform. Go to Low Sensitivity A-2.
	2	Junction R5 and relay contact A3	+5 V	Remove pc board from test fixture. Inspect R3 for damage. Adjust R5 CW if voltage measured in Step 1 was low, CCW if it was high. Replace board and measure voltage at terminal 6. Repeat adjustment until the correct voltage is observed. If unable to adjust, replace R5.	Go to Low Sensitivity A-3
	3	A8 Terminal 4	+5 V	Replace relay K1	If +5 VDC overload indicator is lighted, replace C4. If overload indicator is not lighted check seating of pc board in test fixture.

Table 5-15. Sensitivity (A8), Fault Isolation Procedure (Cont)

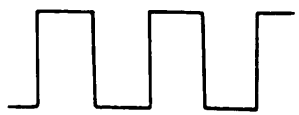
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
Low Sensitivity B	1	A8 Terminal 5	+2.5 VDC max	Check seating of pc board in test fixture	Check seating of pc board. Go to Low Sensitivity B-2.
	2	Anode CR2	-2.5 V	Check R8, R9	Go to Low Sensitivity B-3
	3	Cathode CR2	 8 V p-p	Replace CR2	Go to Low Sensitivity B-4
	4	A8 Terminal 1	 8 V p-p	Check CR1, C1, R7	Check seating of pc board in test fixture

Table 5-16. Detector and Video Amplifier (AR3), Fault Isolation Procedure

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
		NOTE: This procedure applies for AR3 part Nos. 4023409-0501 and 4023409-0502 only.			
1A	1	Collector Q14	+4.500 ±0.025 V	Check for broken wire between TP2 and pc board #2	Go to 1A-2
	2	Junction of R78, R79	+12 V	Go to 1A-3	Check for broken wire between pc board #2 and terminal 1
	3	Junction of R79, VR2	+8.4 V	Go to 1A-4	Replace pc board #2
	4	Collector Q14	+4.500 ±0.025 V	NA	Adjust R73 until +4.500 V is measured at collector Q14. If unable to adjust to this voltage, disconnect +4.5 VDC (red wire) between pc board #1 and pc board #2. If R73 can now adjust to correct voltage, replace pc board #1. If correct voltage still cannot be obtained, replace pc board #2.

Table 5-16. Detector and Video Amplifier (AR3), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
2A	1	Collector Q15	-4.500 ± .025 V	Check for broken wire between TP3 and pc board #2	Adjust R76 until -4.500 VDC is observed at collector of Q15. If unable to adjust to this voltage, disconnect the -4.5 VDC jumper (blue wire) between pc board #1 and pc board #2. If R76 can now adjust to this voltage, replace pc board #1. If correct voltage still cannot be obtained, replace pc board #2.
3A	Test positions 3,4 and 5 represent pulse testing of the Video Amplifier with 3 different levels of input signal. The operator shall rotate the Video Amplifier test switch through positions 3,4 and 5, observing the condition of indicator A in each of these positions. One of the following Fault Isolation Procedures must be selected which corresponds to the lamp inications observed.				
	Indicator A Lighted in Position 3 only - Go to 3A-1 Lighted in Position 3 and 4 - Go to 3A-2 Lighted in Position 3 and 5 - Go to 3A-3 Lighted in Positions 3,4 and 5 - Go to 3A-4 Lighted in Position 4 only - Go to 4A-1 Lighted in Position 4 and 5 - Go to 4A-2 Lighted in Position 5 only - Go to 5A-1				

Table 5-16. Detector and Video Amplifier (AR3), Fault Isolation Procedure (Cont)

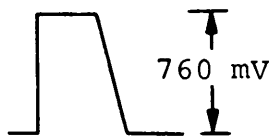
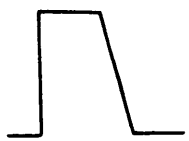
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A (Cont)	1	Indicator A Lighted in Position 3 Only Check for a broken jumper wire (white/yellow) between R35 of pc board #1 and the junction of R57 and R58 on pc board #2. If the connection is good, replace pc board #1.			
	2	Indicator A Lighted in Positions 3 and 4 Replace pc board #1.			
	3	Indicator A Lighted in Positions 3 and 5 Replace pc board #2.			
	4	Indicator A Lighted in Positions 3,4 and 5 Rotate the test selector switch to Position 5. Observe the waveform at TP4.			
		TP4		Check connection between TP4 and the Test Set	Go to 3A-5
	5	Junction R59 & R60 on pc board #2		Go to 3A-6	Check -4.500 VDC jumper (blue wire) connection to pc board #1. Check +4.500 VDC jumper (red wire) connection to pc board #1. If both connections are good, replace pc board #1.

Table 5-16. Detector and Video Amplifier (AR3), Fault Isolation procedure (Cont)

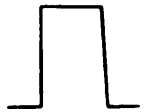
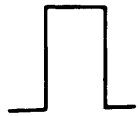
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A (Cont)	6	Emitter Q1 on pc board #1		Replace pc board #2	Disconnect the white jumper wire between the detector assembly output and the junction of R1 and R2. Go to 3A-2.
	7	Detector Assembly Output		Replace pc board #1	Replace detector assembly.
4A	1	Indicator A Lighted in Position 4 Only Replace pc board #1			
	2	Indicator A Lighted in Positions 4 and 5 Check jumper connection (yellow wire) between pc board #1 and pc board #2			
5A	1	Indicator A Lighted in Position 5 Only Replace pc board #2			

Table 5-16. Detector and Video Amplifier (AR3), Fault Isolation Procedure (Cont)

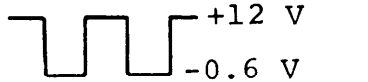
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6A	1	Collector Q9	 100 kHz square wave 11 V p-p	Check the connection (violet wire) between Q9 and Pin 4 of pc board #1. Check the seating of Video Ampl. assembly in the holding fixture.	Go to 6A-2
	2	Junction C11 and R40	 100 kHz square wave 4 V p-p	Go to 6A-3	Replace pc board #1
	3	Base Q8	 100 kHz square wave	Replace pc board #1	Disconnect the jumper (white/brown) wire from CR2 on pc board #1 to Q16 on pc board #2. If the correct waveform is observed at Base Q8, replace pc board #2. If incorrect waveform is observed, replace pc board #1.

Table 5-16. Detector and Video Amplifier (AR3), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
7A	1	Collector Q9	+1.8 V max	NA	Go to 7A-2
	2	Junction R81 and white/ green wire	+5 V	Check jumper connection (white/brown wire) between Q16 on pc board #2 and CR2 on pc board #1. If connection is good replace pc board #2.	Check connection (white/green wire) between pc #2 and Pin 5. Check seating of Video Amplifier in test holding fixture.

NOTES FOR TABLE 5-17

POWER SUPPLY (PS1), FAULT ISOLATION PROCEDURE

General note on replacement of assemblies
(to be observed if applicable)

when any non-repairable subassembly or component is replaced, or if adjustment of power supply is indicated, assembly 21435 shall be replaced with assembly 21435-1.

Indicators A and B, Explanation

Indicators A and B in positions 1 through 8 test the power output voltages under normal load for a nominal 28 percent tolerance, except for the 110V and 1000V outputs which are tested to zero tolerance on the low side. Positions 1 through 5 measure the positive outputs and indicator A reflects an out of tolerance voltage which is excessively positive while indicator B reflects an out of tolerance voltage which is not sufficiently positive; i.e., A is over voltage and B is under voltage. Positions 6 through 8 measure negative voltages and the same statements apply except that B is over voltage and A is under voltage.

Disassembly of the Power Supply

The operator is directed to Section IV, Paragraph 4-33 of Technical Manual, Intermediate and Direct/General Support Maintenance with Depot Overhaul Instructions, RECEIVER-TRANSMITTER, RADIO RT-859/APX-72, NAVAIR 16-30APX72-2, NAVSHIPS 0967-217-4020, TM11-5895-490-35, T.O. 12P4-APX72-2 for disassembly instructions.

Power Supply Extender Cables

Extender cables are supplied which permit troubleshooting of the power supply PS1 on a work surface adjacent to the test set. When it becomes necessary to open a power supply for troubleshooting, place the test set power switch to OFF. Unplug power supply connector P3 from the power supply under test, and remove the power supply from the Power Supply Holding Fixture and connector J4. Insert the ground plug from P1 of extender cable W3 into the ground terminal on the front panel of the test set; then insert connector P3 of the test set

into P1 of W3. The ground terminal is located directly below Jl, the input power connector. Insert the ground connection of P2 into TP1 of the power supply; then insert P2 of W3 into PS1P2 of the Power Supply. Insert P2 of extender W2 into PSIP1; then insert P1 of W2 into J4 of test set.

Table 5-17. Power supply (PS1), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A,B	1	TP4	+5.7 to +6.3 V	Check connection between PS1P2-14 and Test Set	Rotate test selector through positions 2 through 8 and observe A & B indicators. If all or most indicators light as follows, a general over voltage exists: go to 1A,B-2 1 2 3 4 5 6 7 8 A A A A A B B B If the indicator pattern is reversed (B's for A's, etc.) a general under voltage exists, go to 1A,B-3. If most or all indicators do not light in positions 2 through 8, check CR29, CR30, C32, C33, L12, & L13. If good, replace T3.
	2	TP3 TP5 TP6 E13 TP7 TP8 TP9	+5.9 to +6.6 V +11.4 to +12.6 V +23.8 to +26.2 V +1000 to +1100 V -6.2 to -5.7 V -84 to -76 V -110 to -122 V	Check connection between PS1P2 and Test Set	Adjust PS1R63 to correct voltages. If not successful, go to 1A,B-3.

Table 5-17. Power supply (PS1), Fault Isolation procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A,B (Cont)	3	A2-4	+17.5 V adjustable with R63	NA	(a) If a steady 0 volts, or much less than 17 volts and not adjustable, check C14 & C15. If good, go to 1A,B-4. (b) If over 17 V, not adjustable, and voltages in step 1A,B-2 were not zero, check Q1 & Q2. If not shorted, replace A1 & A2. (c) If over 17 V, not adjustable, and voltages in step 1A,B-2 were all zero, go to 1A,B-6. (d) If approximately 17 V, and adjustable, replace T3,A4,FL3,FL2. (e) If zero volts with momentary increases at approx 3 second intervals, remove plug from PS1P2 and go to 1A,B-7.
	4	Q2, Collector	+35 V ±20%	NA	(a) If zero, or much less than 17 volts, check FL1, T1, CR1 & CR2, and L1. If OK, replace A8. (b) If 35 V, or more, note reading and go to 1A,B-5.
	5	A2-1	Same as step 4	NA	(a) If voltage is the same as in 1A,B-4(b), check Q1, Q2, CR3 and C11. If all good, replace A2; if any are bad, replace A8. (b) If voltage is not the same as in 1A,B-4(b), replace A7.

Table 5-17. Power Supply (PS1), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A,B (Cont)	6	Q15 Collector	 35 V p-p 10 kHz squarewave	Replace A4, FL3 or FL2 assemblies	Replace Q15/Q16 assy, A3, A4, FL3 or FL2
	7	A2-4	Steady +17.5 V	Reconnect plug to PS1P2 and adjust R64 CCW until steady 17.5 V is obtained	(a) Disconnect wire at A5E11 and reconnect plug to PS1P2. If voltage (at A2-4) becomes a steady 17 V, replace A5. (replace wire) (b) If voltage does not become steady, replace wire and check test points for resistance to ground*. If not as listed, replace component indicated. TP3 > 3K ohms (+) FL2 TP5 > 13K ohms (+) FL3 TP6 > 50 ohms (+) FL3 E13 > 800K ohms (+) A5 TP7 > 6K ohms (-) FL3 TP8 > 500K ohms (-) FL3 TP9 > 150K ohms (-) FL3 *Measure TP3 to L3V ret. Measure E13 to PS1P2-9 Ohmeter polarity to be as noted in parenthesis. > = greater than If all are OK, go to 1A,B-8.

Table 5-17. Power Supply (PS1), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1A,B		With PS1P2 disconnected, temporarily ground A1-10 and apply power for only a few seconds.			
	8	Q15 Collector	 35 V p-p	Replace A1	Check Q15/Q16 assy. If OK, replace A3, T3.
1C	1	TP4	Ripple less than 0.060 V p-p	NA	Check C33, C32, L12, L13, C29, C30. If good, replace T3.
1F	1	PS1P1-1	0 ohms to PS1P2-1	Go to 1F2	Repair open connections or replace flex cable as required
	2	PS1P1-6	0 ohms to PS1P2-6	Go to 1F3	
	3	PS1P1-10	0 ohms to PS1P2-10	Go to 1F4	
	4	PS1P1-12	0 ohms to PS1P2-2	Go to 1F5	
	5	PS1P1-15	0 ohms to PS1P2-3	Go to 1F6	
	6	PS1P1-A2	0 ohms to PS1P1-A2	Check connections to test set	

Table 5-17. Power Supply (PS1), Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
1G	1	PS1P1-1	∞ ohms to gnd	Go to 1G2	Replace grounded connections or replace cable as required
	2	PS1P1-6	∞ ohms to gnd	Go to 1G3	
	3	PS1P1-10	∞ ohms to gnd	Go to 1G4	
	4	PS1P1-12	∞ ohms to gnd	Go to 1G5	
	5	PS1P1-15	∞ ohms to gnd	Go to 1G6	
	6	PS1P1-A2	∞ ohms to gnd	Check connections to test set	
	NOTE: If 1F and 1G faults are both indicated, perform 1G fault isolation first and then re-test. In the following A-B sequence fault isolation procedures it is assumed that the fault occurs in only one position. However, whenever an A or B fault is indicated, all positions should be checked and if many positions show fault it may be necessary to follow the procedures of 1A, B.				
2A,B	1	TP3	+5.9 V to 6.6 V	Check connections to Test Set	Check C37, C36, CR34-CR35, L10, L11. If good replace T3.
2C	1	TP3	Ripple less than 0.250 V p-p	NA	Check C37, C36, CR34-CR35, L10, L11. If good replace T3.

Table 5-17. Power Supply (PS1), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
3A,B	1	TP5	+11.4 to 12.6 V	Check connections to Test Set	Check C31, C38, CR27, CR28, L7. If good, replace T3.
3C	1	TP5	Ripple less than 0.060 V p-p	NA	Check C31, C38, CR27, CR28, L7. If good, replace T3.
4A,B	1	TP6	+23.8 V to 26.2 V	Check connections to Test Set	Check C28, CR23, CR24, L4. If good, replace T3.
4C	1	TP6	Ripples less than 0.125 V p-p	NA	Check C28, CR23, CR24, L4. If good, replace T3.
5A,B	1	E13	+1000 V to 1110 V	Check connections to Test Set	Go to 5A,B-2
	2	E11 - E12	Approx 500 V p-p 10 kHz square wave	Replace A5	Replace T3
5C	1	E13	Ripple less than 5 V p-p	NA	Check C25, C26, CR19, CR20, CR37, CR38. If good, replace T3.

Table 5-17. Power Supply (PS1), Fault Isolation Procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
6A,B	1	TP7	-6.3 V to -5.7 V	Check connections to Test Set	Check C35, C34, CR31, CR32, CR42, R58, R59. If good, replace T3.
6C	1	TP7	Ripple less than 0.120 V p-p	NA	Check C35, C34, CR31, CR32, R58, R59. If good, replace T3.
7A,B	1	TP8	-8 V to -76 V	Check connections to Test Set	Check C29, CR22, CR25, R57. If good, replace T3.
7C	1	TP8	Ripple less than 0.40 V p-p	NA	Check C29, CR22, CR25, R57. If good, replace T3.
8A,B	1	TP9	-110 V to -122 V	Check connections to Test Set	Check C30, CR21, CR26, L6. If good, replace T3.
8C	1	TP9	Ripple less than 1.1 V p-p	NA	Check C30, CR21, CR26, L6. If good, replace T3.
9F	1	PS1P1-11	0 ohms to ground	Check connections to Test Set	Repair open connection or replace cable as required

Table 5-17. Power Supply (PS1), Fault Isolation Procedure (Cont)

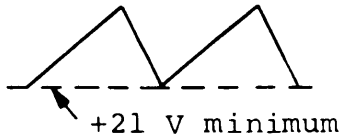
TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
10F	1	PS1P2-11	0 ohms to ground	Check connections to Test Set	Repair open connections or replace cable as required
11F	1	PS1P1-4	0 ohms to TP5	Go to 11F2	Repair open connections or replace cable as required
	2	PS1P1-5	0 ohms to TP6	Go to 11F3	
	3	PS1P1-7	0 ohms to L1-1	Check connections to Test Set	
12F	1	PS1P1-8	0 ohms to L1-1	Go to 12F2	Repair open connections or replace cable as required
	2	PS1P1-13	0 ohms to TP7	Go to 12F3	
	3	PS1P1-14	0 ohms to TP4	Check connections to Test Set	
13A,B	1	Collector Q2		Measure waveform with DCVM, note value, and go to 13A,B-2	Check C2 thru C8, CR1, CR2, T1
	2	A2-1	Minimum of +1.5 V more than noted in preceding step	Check Q1, Q2 Replace A2	Replace A7

Table 5-17. Power Supply (PSI), Fault Isolation procedure (Cont)

TEST SEQUENCE	STEP NO.	TEST POINT	NORMAL WAVEFORM	ACTION FOR NORMAL WAVEFORM	ACTION FOR ABNORMAL WAVEFORM
14			No test		
15A,B	1	A2-4	Momentarily move switch to position 14 and note voltage. Position 15 should then be slightly higher.	Check CR39, CR35, C36, C37, L10, L11. If good, replace T3.	Replace A1,A2
15D	1	TP3	+5.9 V to +6.6 V	Fault D indicates that power supply under test is shut down due to actuation of overcurrent circuitry on A1. This is further evidenced by TP3 measuring 0 volts but with momentary voltage appearing at intervals of 3 sec. To correct this condition turn R64 on A1 CCW in increments of ½ turn until normal voltage indication remains steady. If this procedure is not successful, replace A1.	
16E	1	TP3	0 V except for brief increase of voltage at intervals of approx 3 s	NA	
			Fault E indicates that power supply under test is not shutting down even though the Test Set is now overloading the output. This is further evidenced by TP3 remaining steady at approx 6 V. To correct this condition turn R64 on A1 CW until voltage drops to 0 V and increases momentarily at approx 3 sec intervals. If this adjustment is successful, then position 15 must be rechecked, i.e., both 15 and 16 must show no fault. If this is not possible, check R36. If good, replace A1.		

SECTION VI

WIRING DIAGRAMS

6-1. GENERAL

6-2. This section contains the schematic diagrams and wiring diagrams for the Receiver-Transmitter RT-859/APX-72, and RT-859A/APX-72. Electrical and electronic symbols and reference designations used are in accordance with military standards MIL-STD-15, MIL-STD-16, MIL-STD-806B, and MIL-M-81260 (WP). Circuitboard wiring diagrams show lower track and components from track side, and upper track and components from the component side. Avionics Changes (AC) and Engineering Change Proposals (ECP) referred to in schematic notes are listed in Section I of this manual.

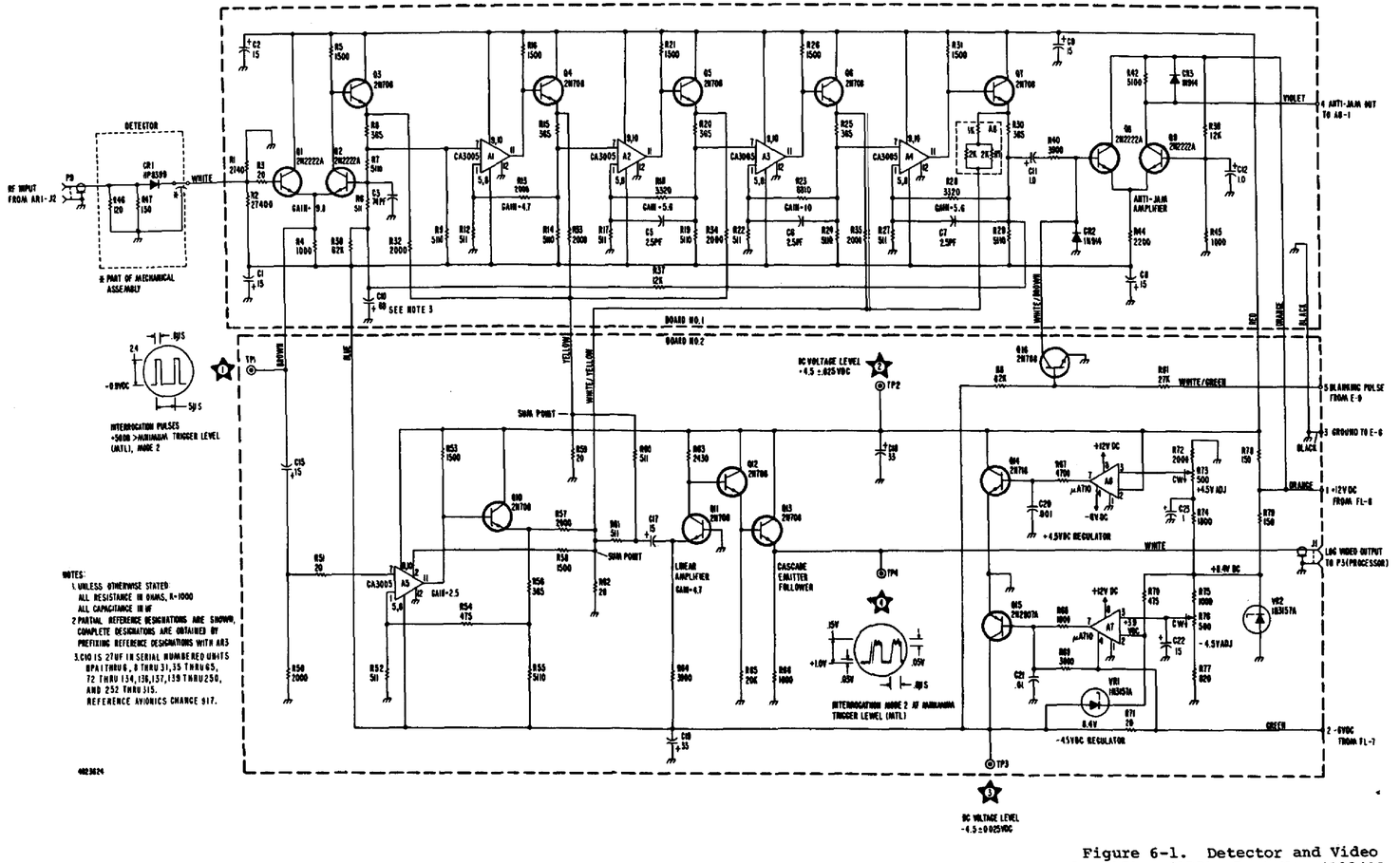
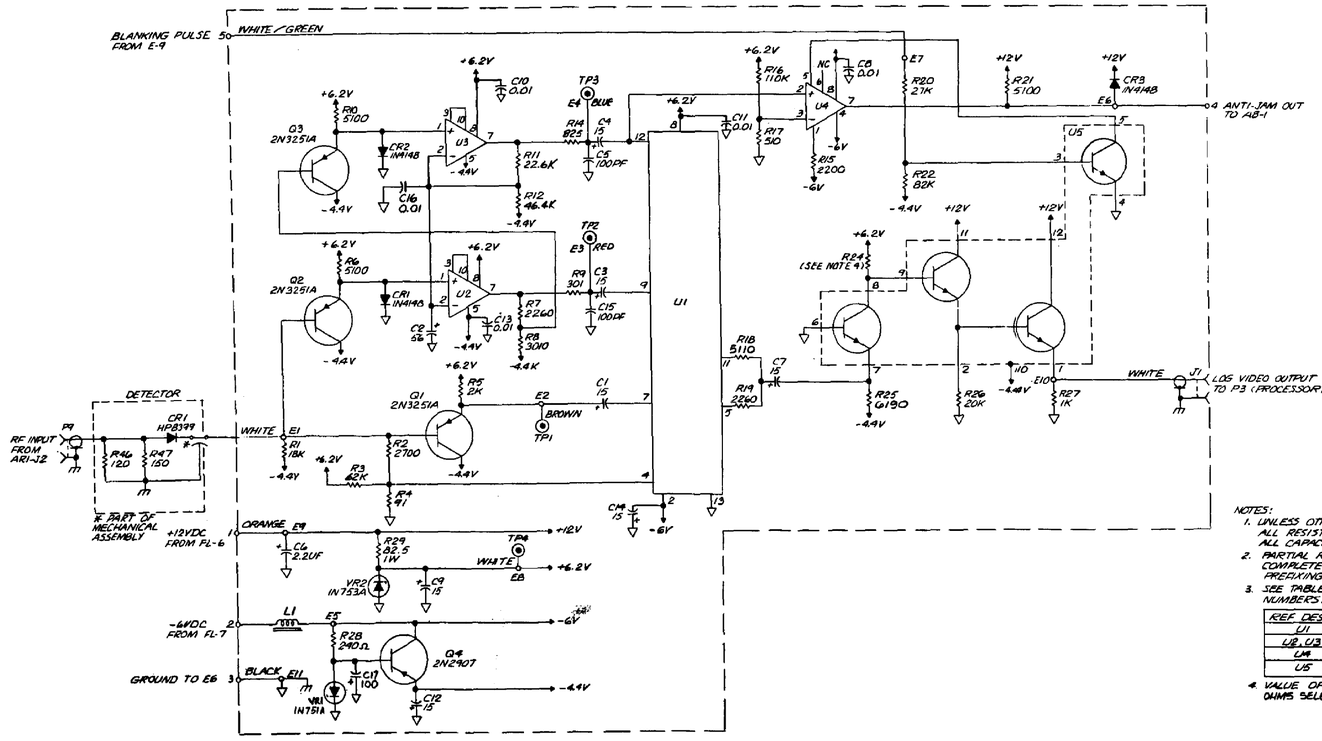


Figure 6-1. Detector and Video Amplifier (AR3), Part No. 4023409-0501, 0502, Schematic Diagram

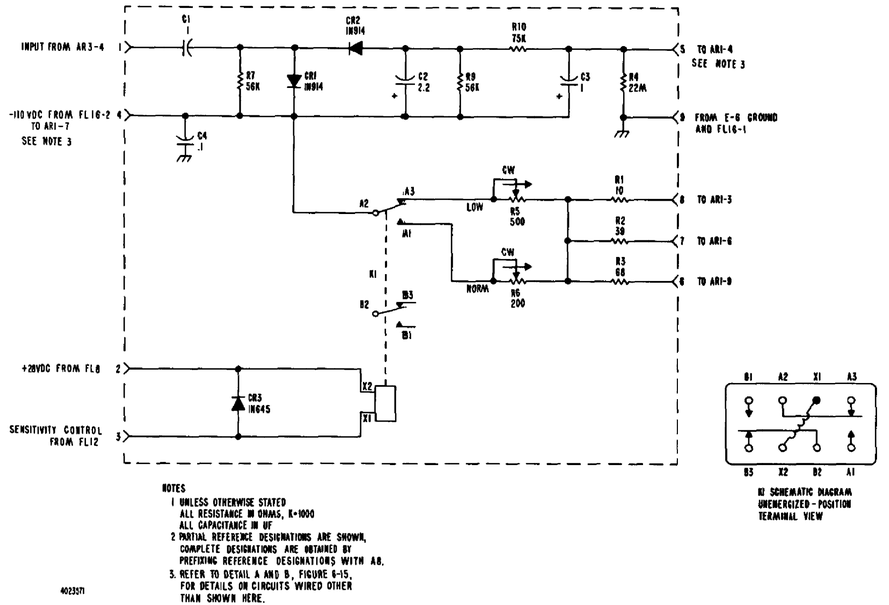


NOTES:
1. UNLESS OTHERWISE STATED:
   ALL RESISTANCE IN OHMS, K=1000
   ALL CAPACITANCE IN UF.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, COMPLETE DESIGNATIONS ARE OBTAINED BY PREFIXING REFERENCE DESIGNATIONS WITH AR3
3. SEE TABLE FOR INTEGRATED CIRCUIT PART NUMBERS.

REF DESIG	PART NO.
U1	911312-1
U2, U3	911313-1
U4	911314-1
U5	911315-1

4. VALUE OF R24 4220, 4640, 5110, 5620 OR 6190 OHMS SELECTED AT TIME OF TEST.

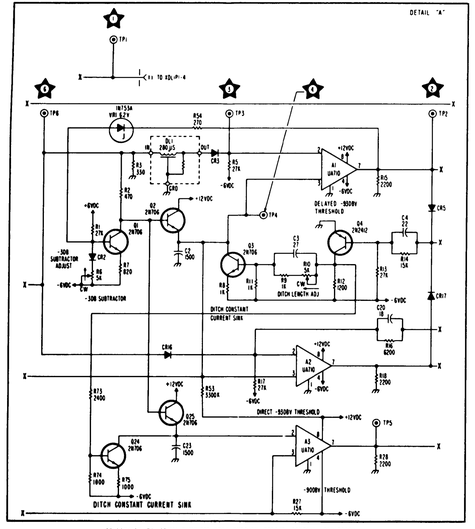
Figure 6-2. Detector and Video Amplifier (AR3), Part No. 4023409-0503, Schematic Diagram



NOTES
1 UNLESS OTHERWISE STATED
ALL RESISTANCE IN OHMS, K=1000
ALL CAPACITANCE IN UF
2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, COMPLETE DESIGNATIONS ARE OBTAINED BY PREFIXING REFERENCE DESIGNATIONS WITH A8.
3. REFER TO DETAIL A AND B, FIGURE 6-15, FOR DETAILS ON CIRCUITS WIRED OTHER THAN SHOWN HERE.

402357I

Figure 6-3. Sensitivity (A8), Schematic Diagram



RT-859/APX-72 SERIAL NUMBERED BPA1 THROUGH BPA572 CONTAIN PROCESSOR ASSEMBLY 4023410-0502 WIRED AS SHOWN IN DETAIL "A" ABOVE REFER TO AVIONICS CHANGE 915.

4026730-55

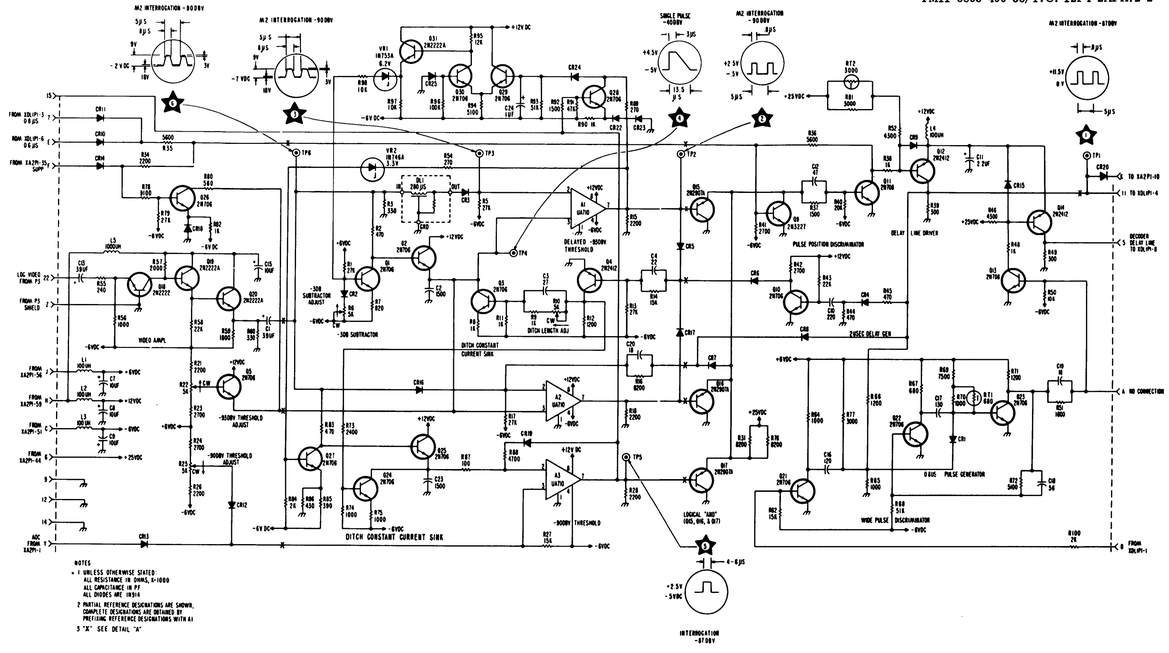


Figure 6-4. Processor (A1), Used With RT-859/APX-72, Schematic Diagram

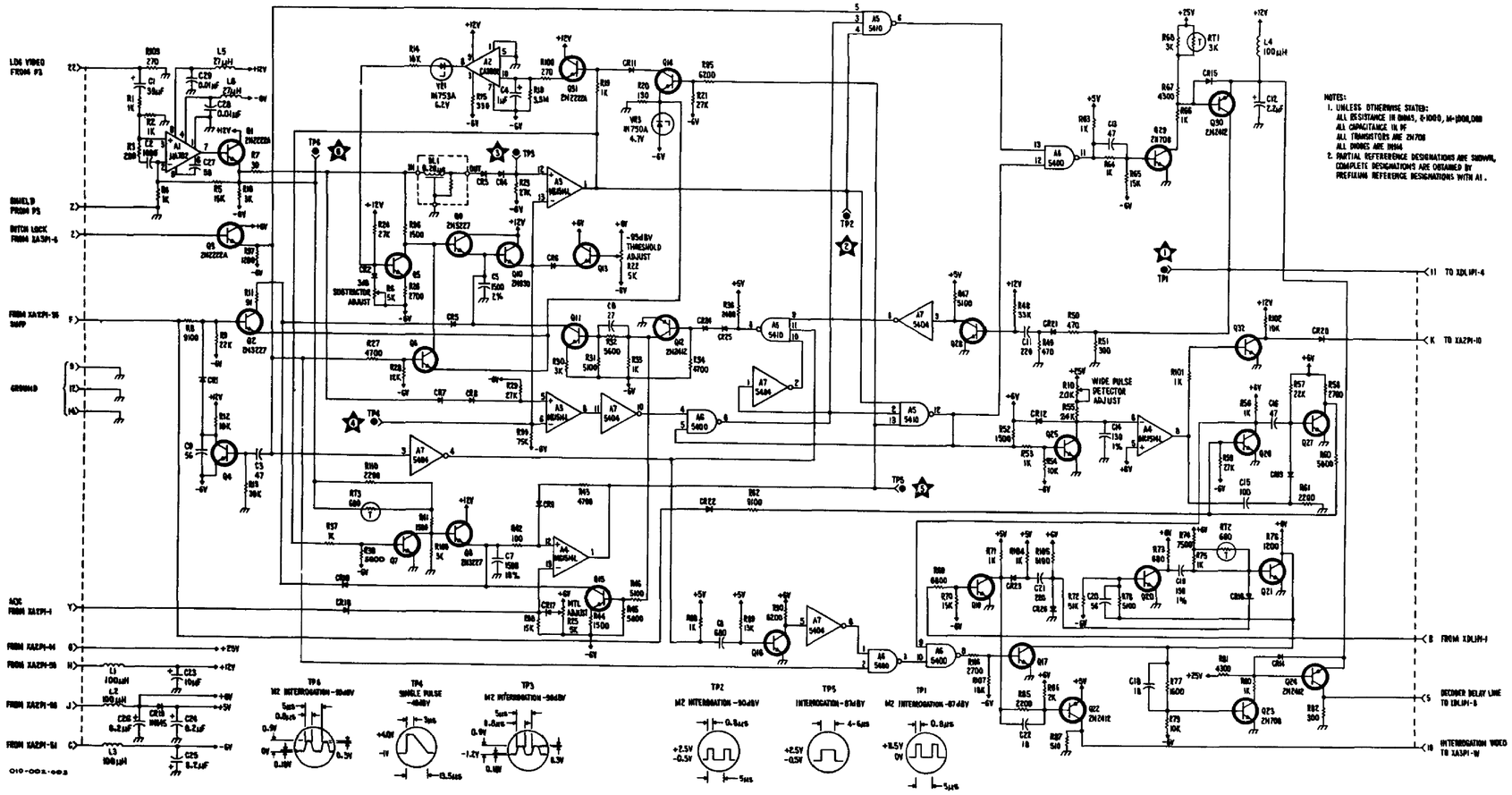


Figure 6-5. Processor (A1), Used With RT-859A/APX-72, Schematic Diagram

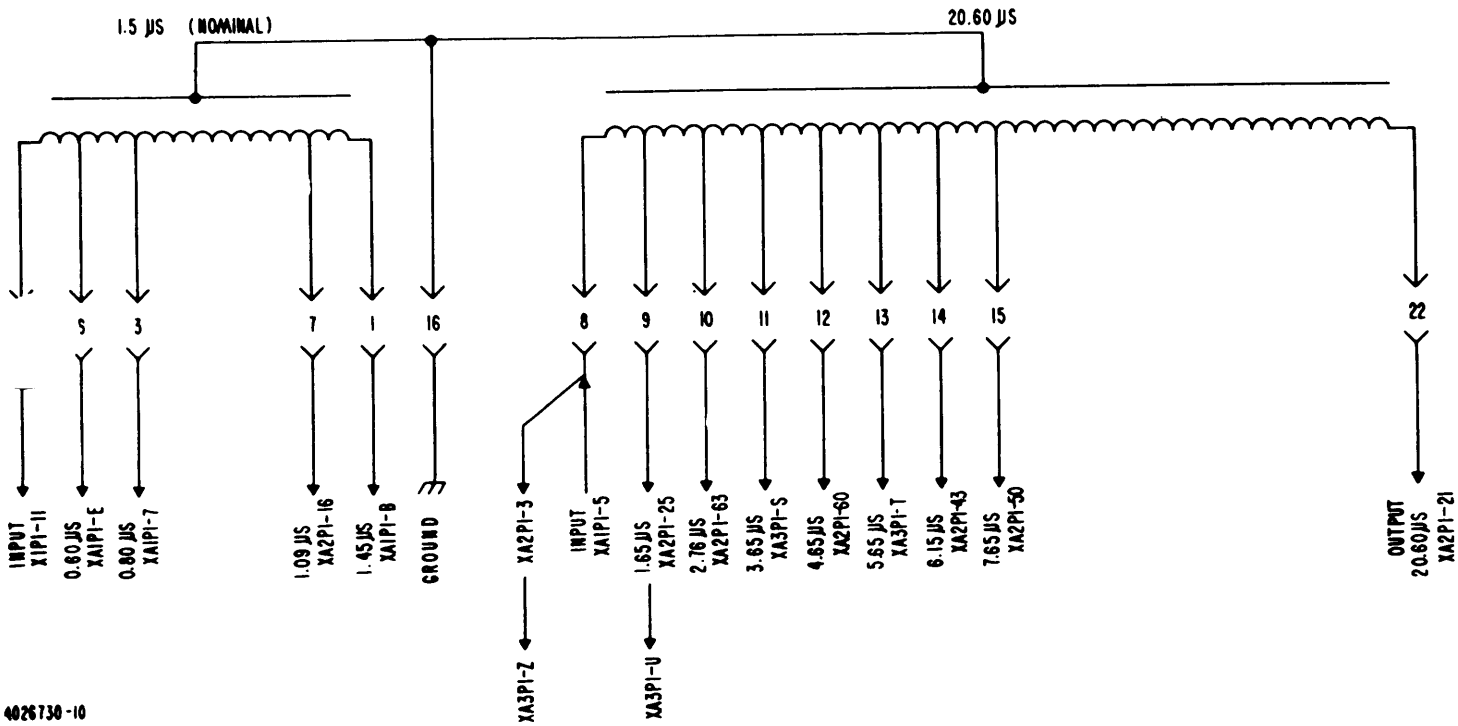


Figure 6-6. Delay Line (DL1), Used With RT-859/APX-72, Schematic Diagram

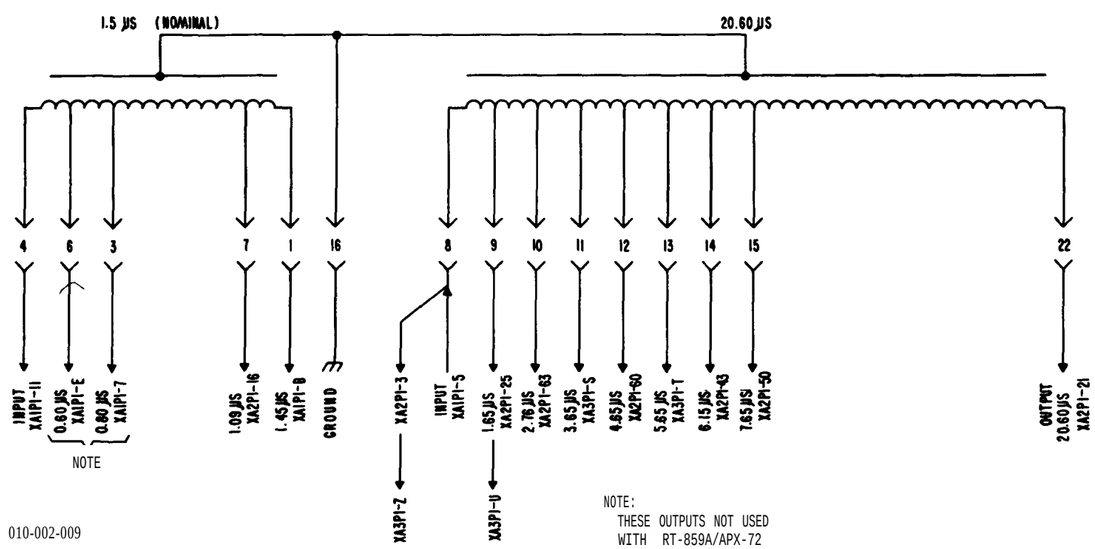


Figure 6-7. Delay Line (DL1), Used With RT-859A/APx-72, Schematic Diagram

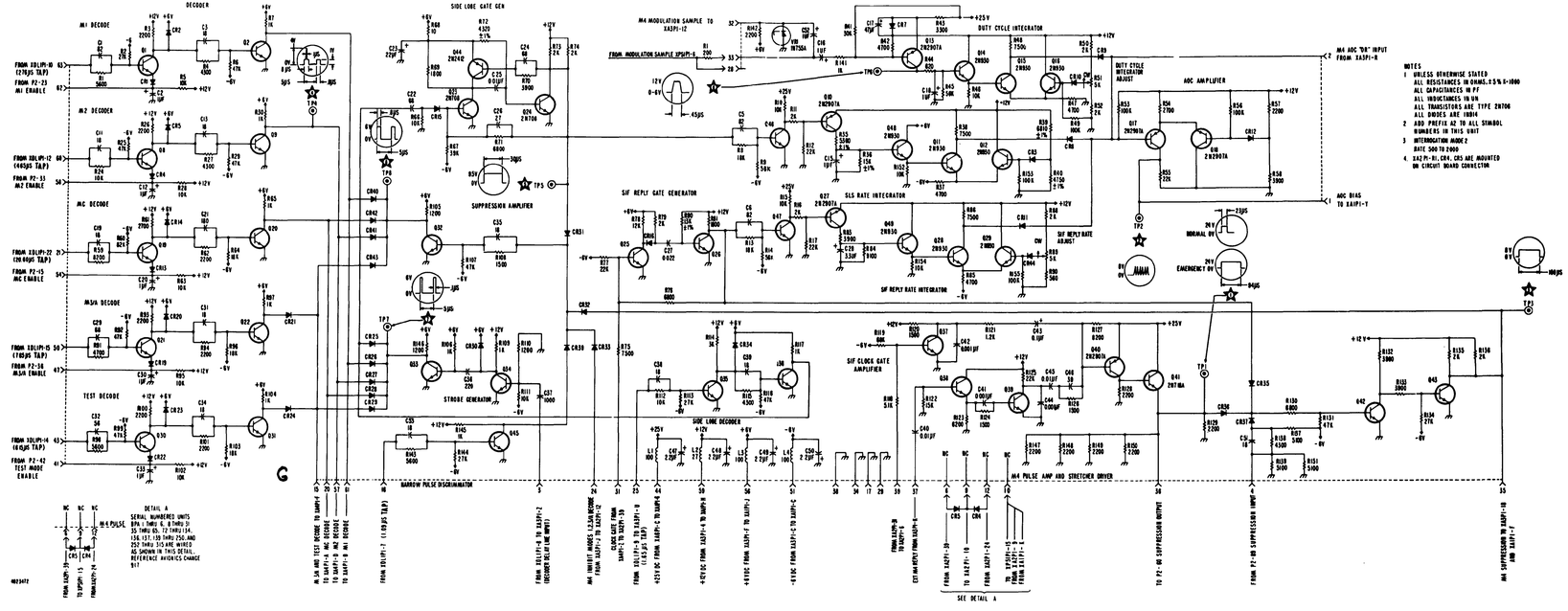


Figure 6-8. Decoder (A2), Used With RT-859/APX-72, Schematic Diagram

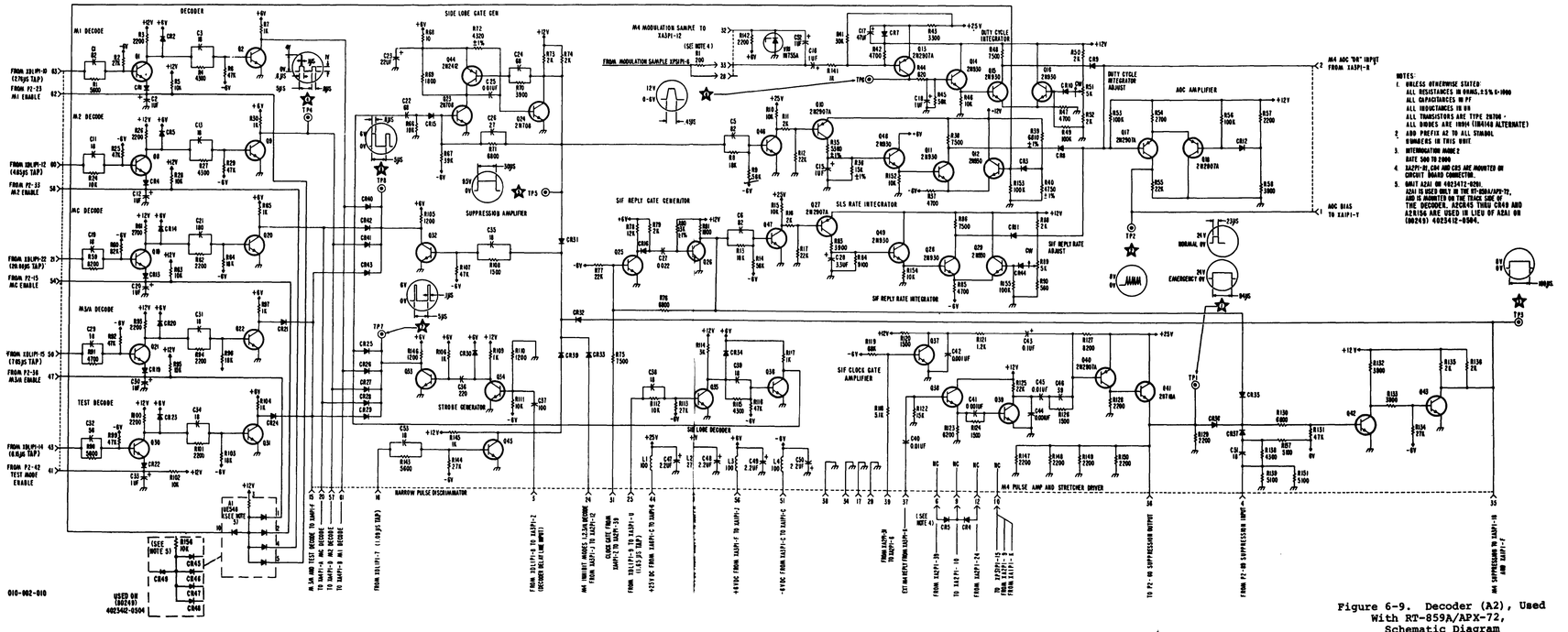
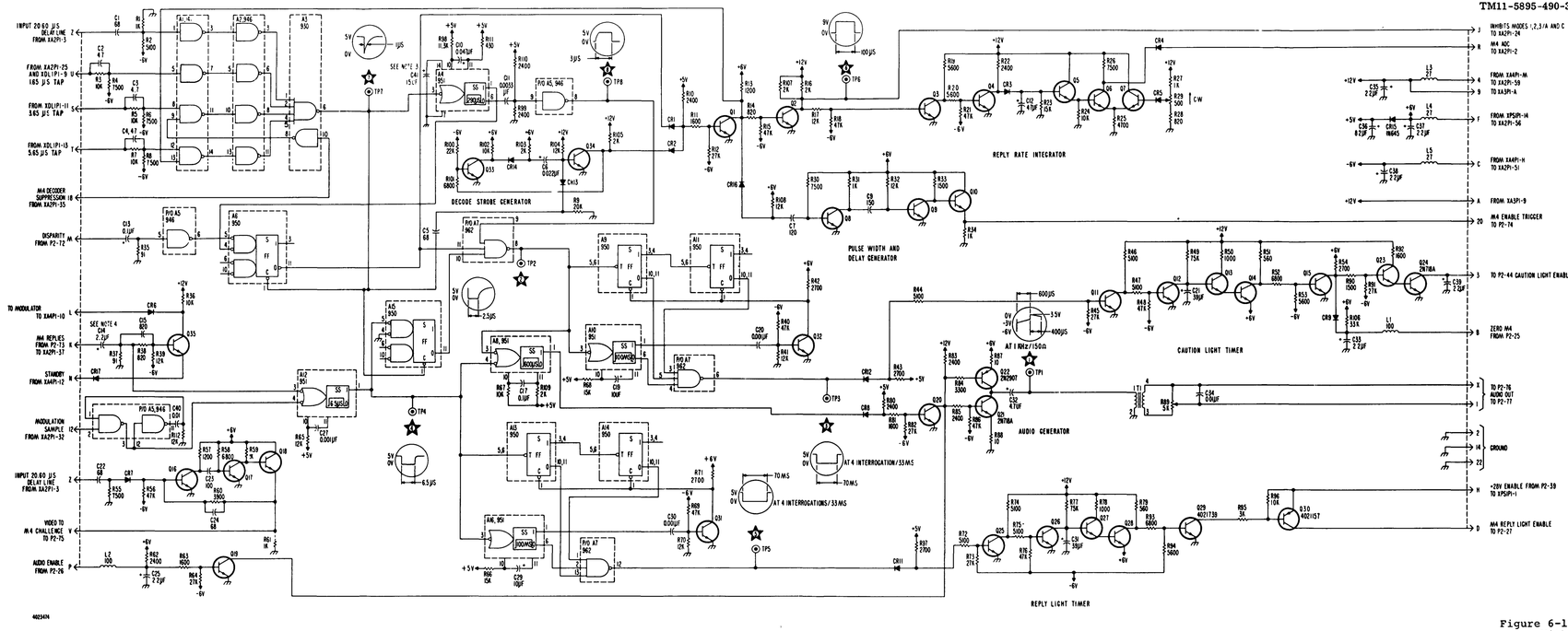


Figure 6-9. Decoder (A2), Used With RT-859A/APX-72, Schematic Diagram



NOTES:
1. UNLESS OTHERWISE STATED
   ALL RESISTANCE IN OHMS, K=1000
   ALL CAPACITANCE IN PF
   ALL TRANSISTORS ARE 2N706
   ALL DIODES ARE 1N914
   ALL INDUCTANCE IN UH
   ALL MODULES EXCEPT A1
   PIN 7 CONNECTS TO CHASSIS GROUND
   PIN 14 CONNECTS TO +5VOLTS
   MODULE A1
   PIN 10 CONNECTS TO CHASSIS GROUND
   PIN 4 CONNECTS TO +5VOLTS
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, COMPLETE DESIGNATIONS ARE OBTAINED BY PREFIXING WITH A3
3. C41 NOT INSTALLED IN SERIAL NUMBERED UNITS BPA1 THRU 8,8 THRU 31, 35 THRU 88, 73 THRU 84, 86 THRU 134, 136, 137, 139 THRU 191, 193 THRU 204, 207 THRU 210, 215, 216, 220, 221, 223 THRU 225, 228, 235, 241 THRU 250, AND 252 THRU 270 C41 IS 10UF IN SERIAL NUMBERED UNITS BPA 211 THRU 345, 350 THRU 1597, AND 1650 THRU 3207 REFER TO AVIONIC CHANGE 916
4. C14 IS .01UF IN ALL SERIAL NUMBERED UNITS LISTED IN NOTE 3 ABOVE REFER TO AVIONICS CHANGE 916

Figure 6-10. Mode 4 (A3), Used With RT-859/APX-72, Schematic Diagram

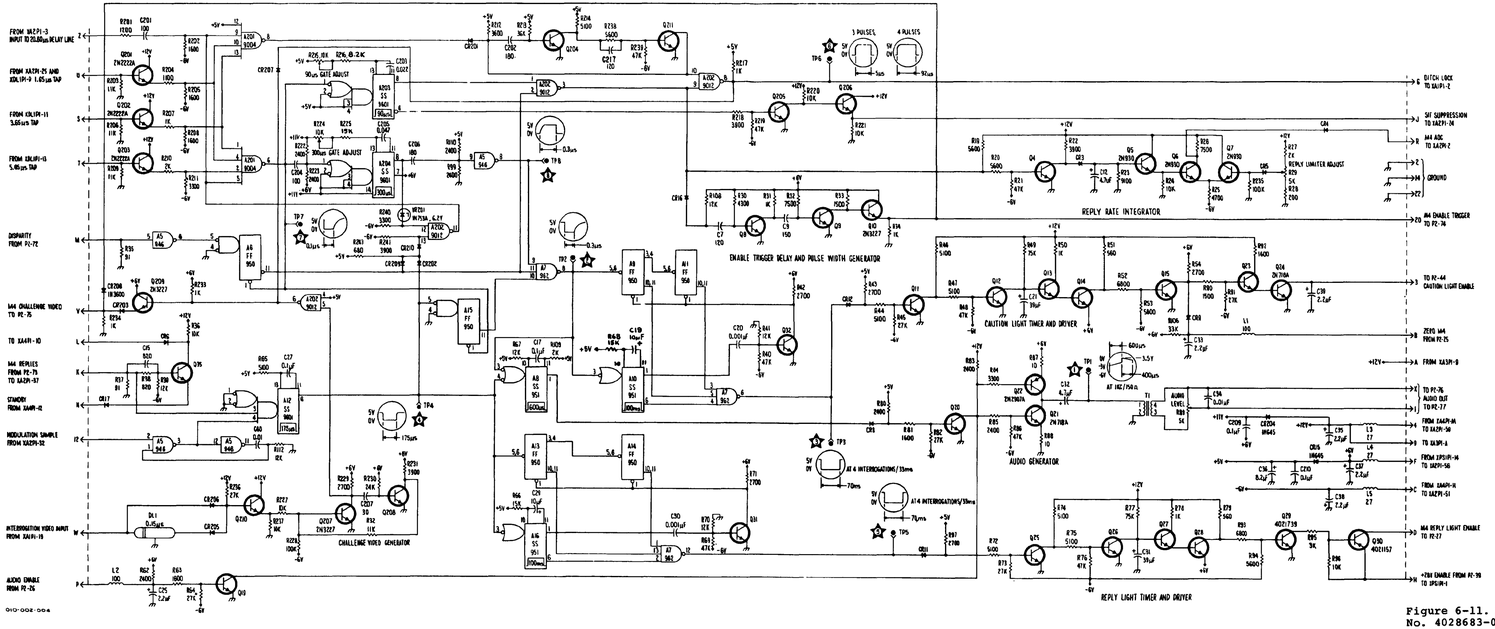
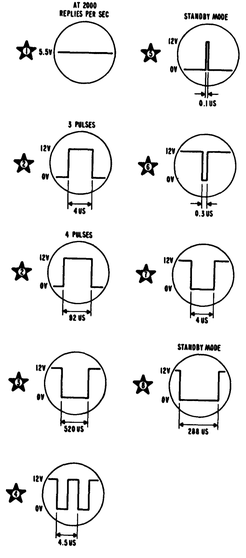
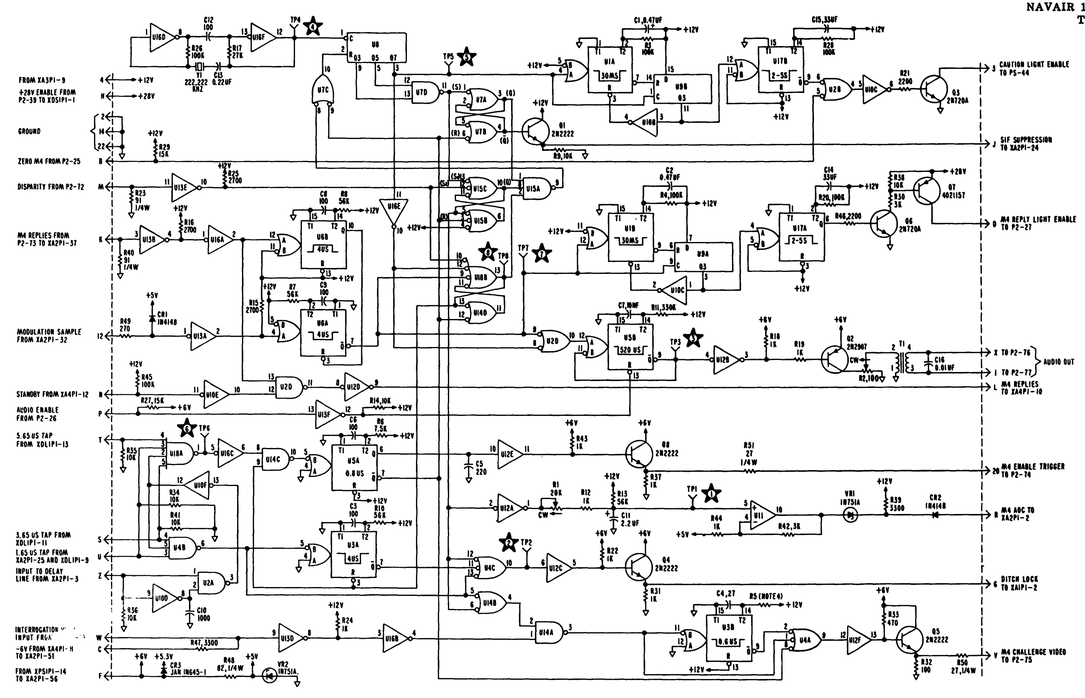


Figure 6-11. Mode 4 (A3), Part No. 4028683-0502, Used with RT-859A/APX-72, Schematic Diagram

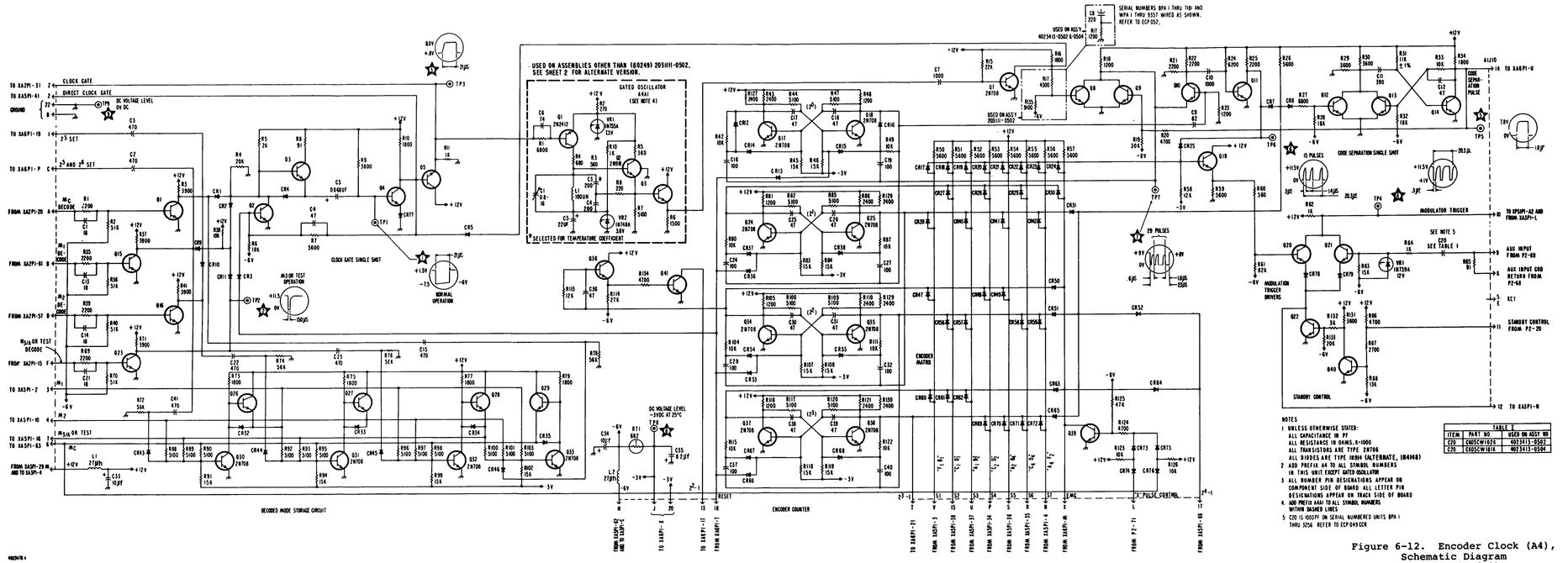




NOTES:
1. UNLESS OTHERWISE INDICATED:
   ALL RESISTANCES IN OHMS, K=1000
   ALL CAPACITANCES IN PF.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; COMPLETE DESIGNATIONS ARE OBTAINED BY PREFIXING WITH A3.
3. R5 IS SELECTED AT FINAL TEST IT MAY HAVE VALUE OF 15, 15.1K, OR 16K.
4. INTEGRATED CIRCUIT CHART

REF DESIG	DEVICE	QTY	+12	GND	+5.5
U1, U17	14538	2	16	8	
U2, U7, U11, U14	4011	4	14	7	
U3, U5, U6	14528	3	16	8	
U4, U15	4013	2	14	7	
U8	4024	1	14	7	
U9	4015	1	16	8	
U10, U16	4049	2	16	8	
U11	741	1	11	6	
U12	54C906	1	14	7	
U13	5406	1		7	14
U18	4012	1	14	7	

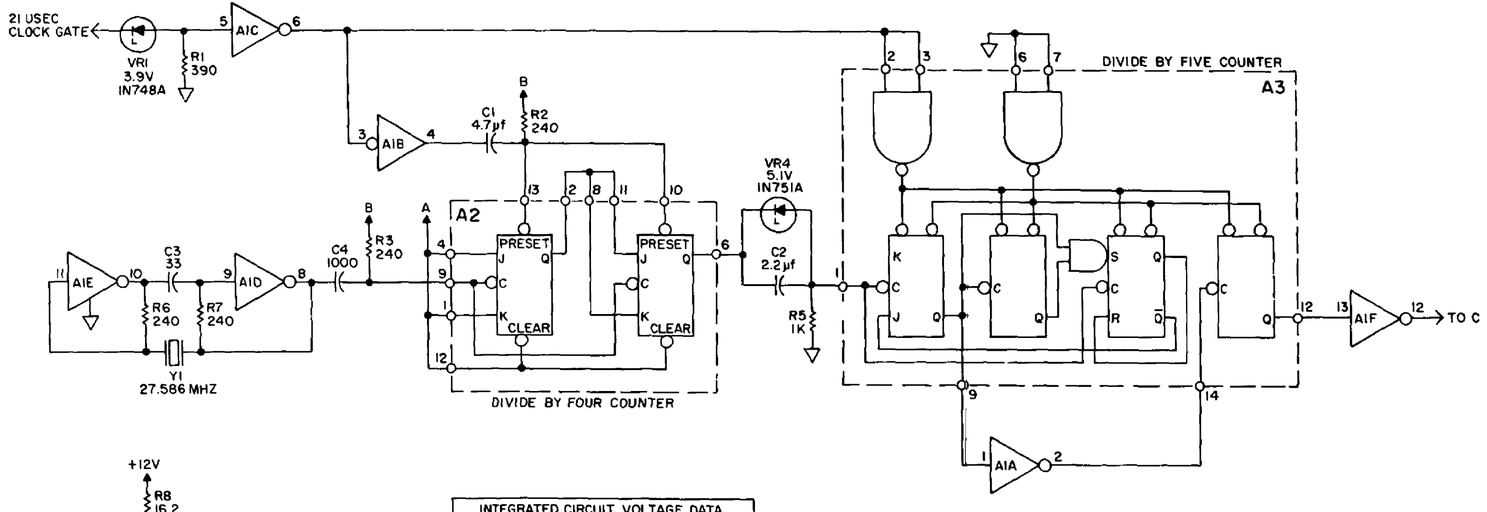
Figure 6-11A. Mode 4 (A3), Part No. 116104-1, Used With RT-859A/APX-72, Schematic Diagram



NOTES
1 UNLESS OTHERWISE STATED:
ALL CAPACITANCE IN PF
ALL RESISTANCE IN OHMS, K=1000
ALL TRANSISTORS ARE TYPE 2N706
ALL DIODES ARE TYPE 1N914 (ALTERNATE, 1N4148)
2 ADD PREFIX A4 TO ALL SYMBOL NUMBERS IN THIS UNIT EXCEPT GATED OSCILLATOR
3 ALL NUMBER PIN DESIGNATIONS APPEAR ON COMPONENT SIDE OF BOARD ALL LETTER PIN DESIGNATIONS APPEAR ON TRACK SIDE OF BOARD
4 ADD PREFIX A4A1 TO ALL SYMBOL NUMBERS WITHIN DASHED LINES
5 C20 IS 1000PF ON SERIAL NUMBERED UNITS BPA-1 THRU 3256 REFER TO ECP-049CCR

TABLE I		
ITEM	PART NO	USED ON ASSY NO
C20	C40DC1W102K	4023413-0502
C20	C40DC1W181K	4023413-0504

Figure 6-12. Encoder Clock (A4), Schematic Diagram (Sheet 1 of 2)



INTEGRATED CIRCUIT VOLTAGE DATA			
REF DESIG	PART NO.	PIN	VOLTAGE
A1	911480-1	7 14	GND B
A2	SN54H108J	7 14	B A
A3	SN5490J	5 10	B GND

GATED OSCILLATOR REF DESIG PREFIX A4A1.

USED ON 80249 ASSEMBLY 2031111-0502.
SEE SHEET 1 FOR ALTERNATE VERSION.

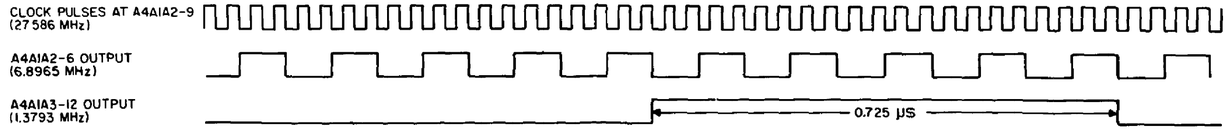


Figure 6-12. Encoder Clock (A4) Schematic Diagram (Sheet 2 of 2)

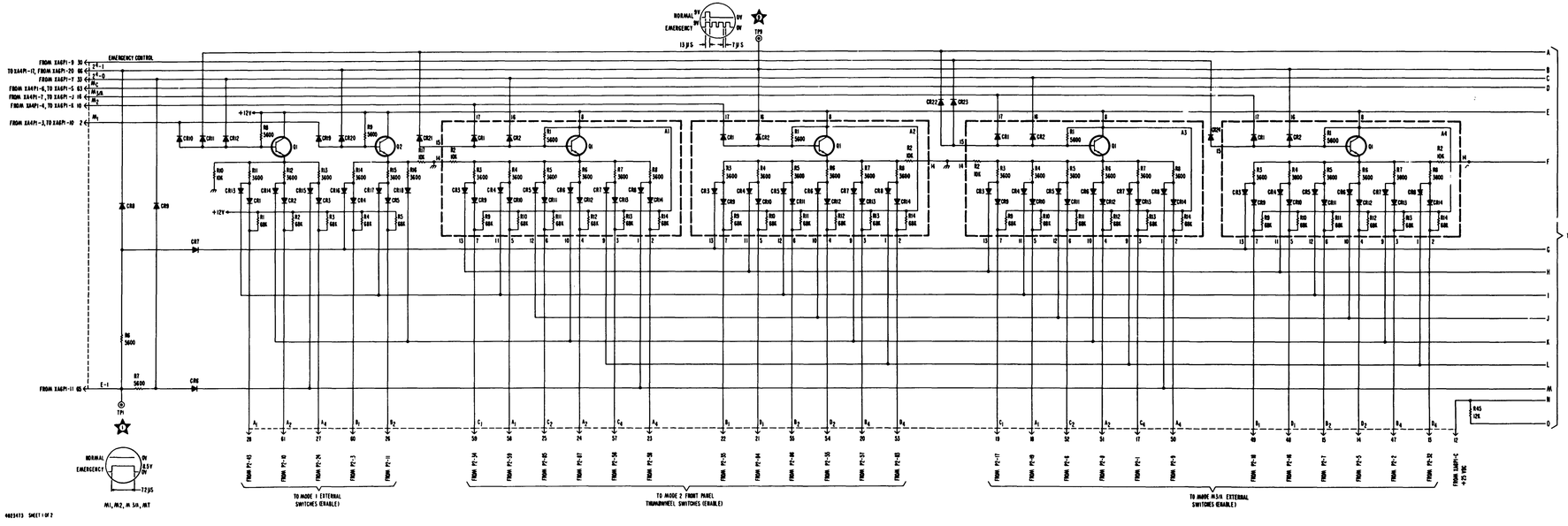
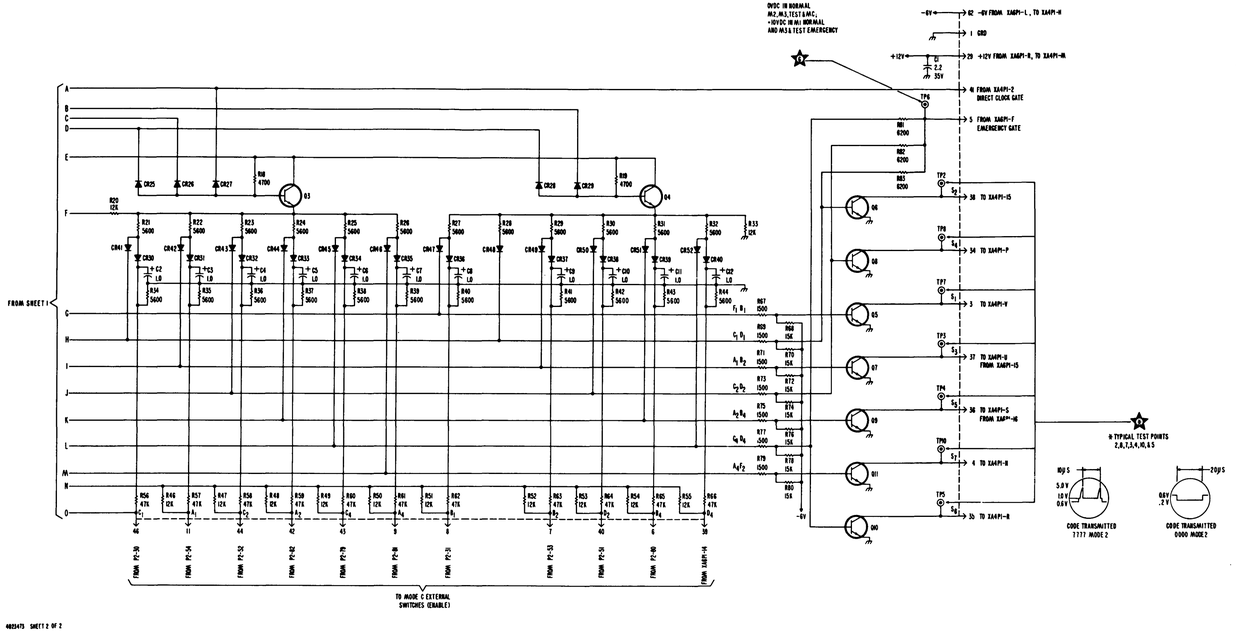


Figure 6-13. Encoder Control (A5), Schematic Diagram (Sheet 1 of 2)



4003473 SHEET 2 OF 2

Figure 6-13. Encoder Control (A5), Schematic Diagram (Sheet 2 of 2)

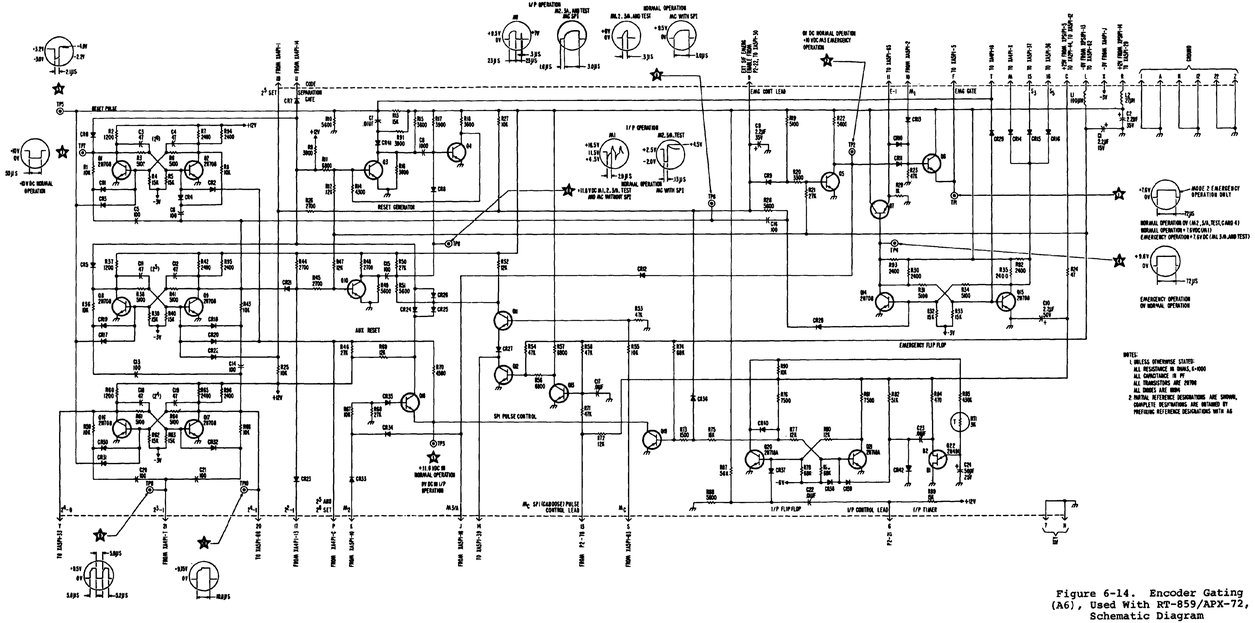


Figure 6-14. Encoder Gating (A6), Used With RT-859/APX-72, Schematic Diagram

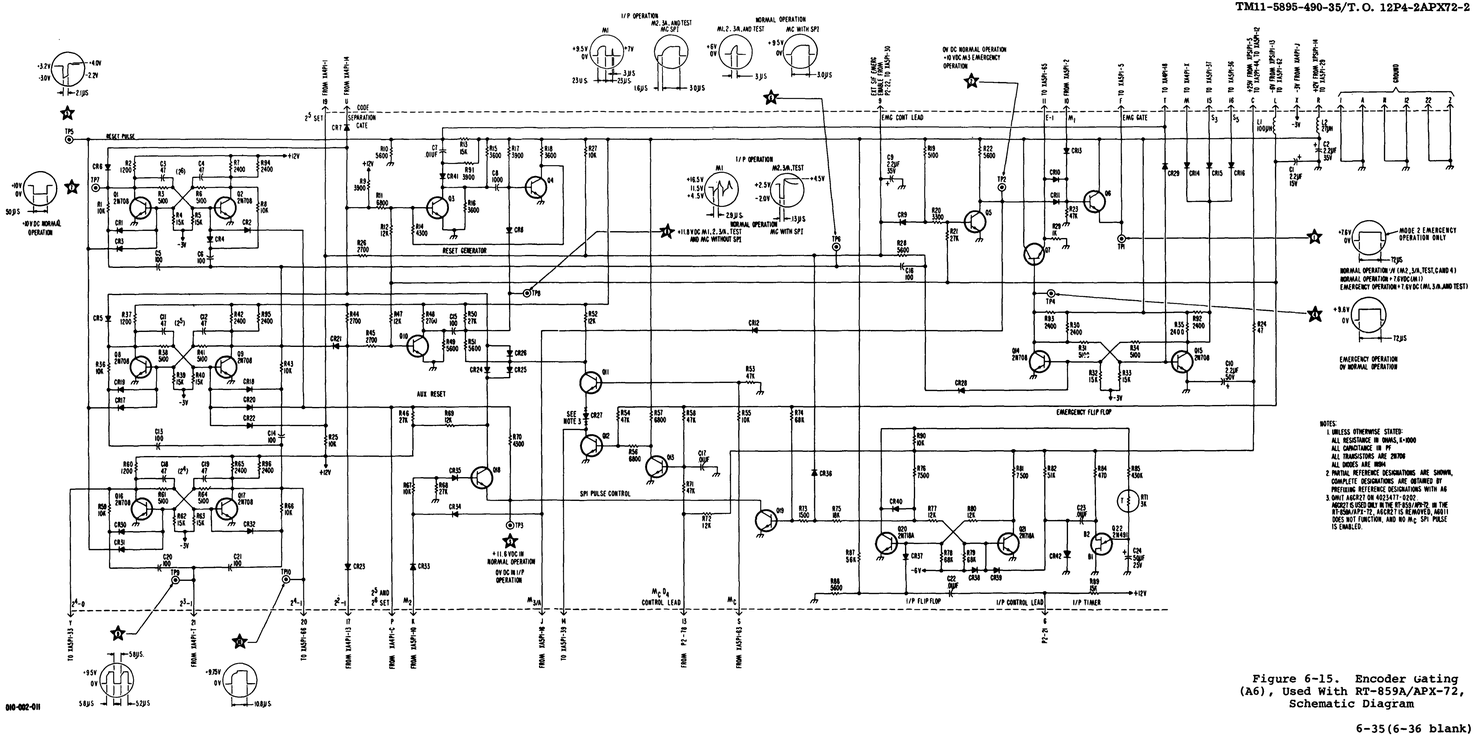
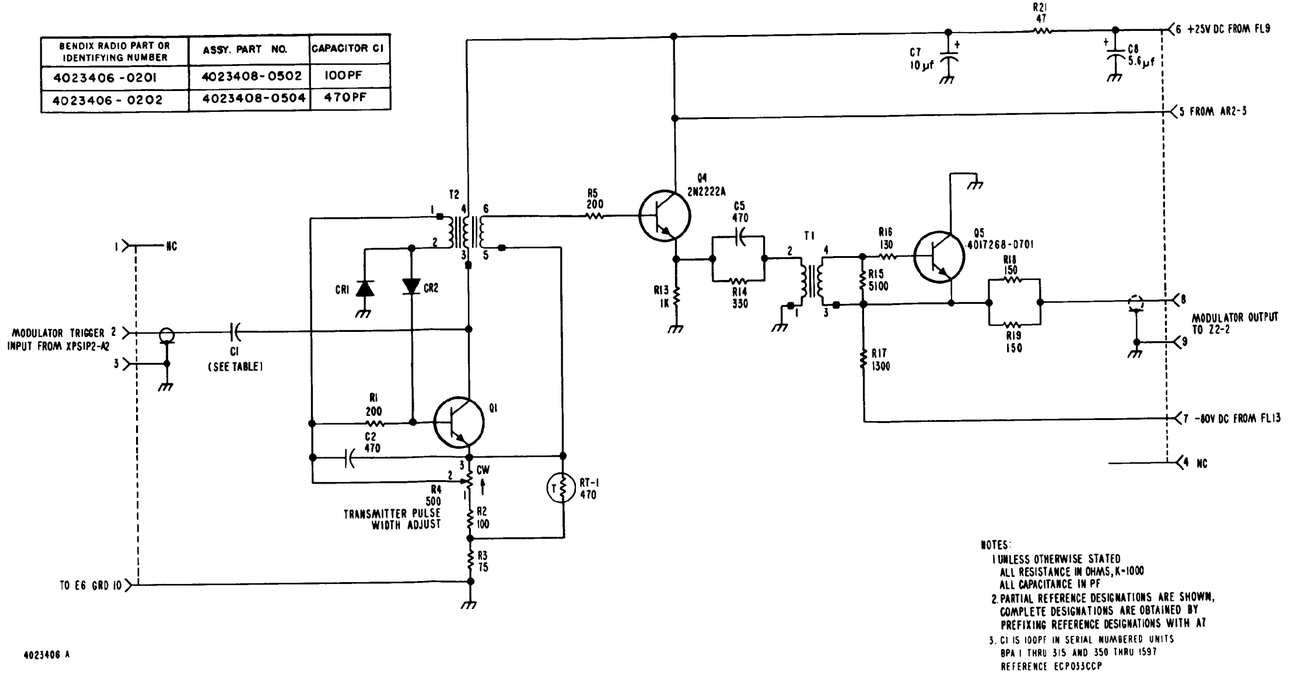


Figure 6-15. Encoder Gating (A6), Used With RT-859A/APX-72, Schematic Diagram

BENDIX RADIO PART OR IDENTIFYING NUMBER	ASSY. PART NO.	CAPACITOR C1
4023406-0201	4023408-0502	100PF
4023406-0202	4023408-0504	470PF



NOTES:
1. UNLESS OTHERWISE STATED
ALL RESISTANCE IN OHMS, K=1000
ALL CAPACITANCE IN PF
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, COMPLETE DESIGNATIONS ARE OBTAINED BY PREFIXING REFERENCE DESIGNATIONS WITH A7
3. C1 IS 100PF IN SERIAL NUMBERED UNITS BPA 1 THRU 315 AND 350 THRU 1597 REFERENCE ECP053CCP

Figure 6-16. Modulator (A7), Schematic Diagram

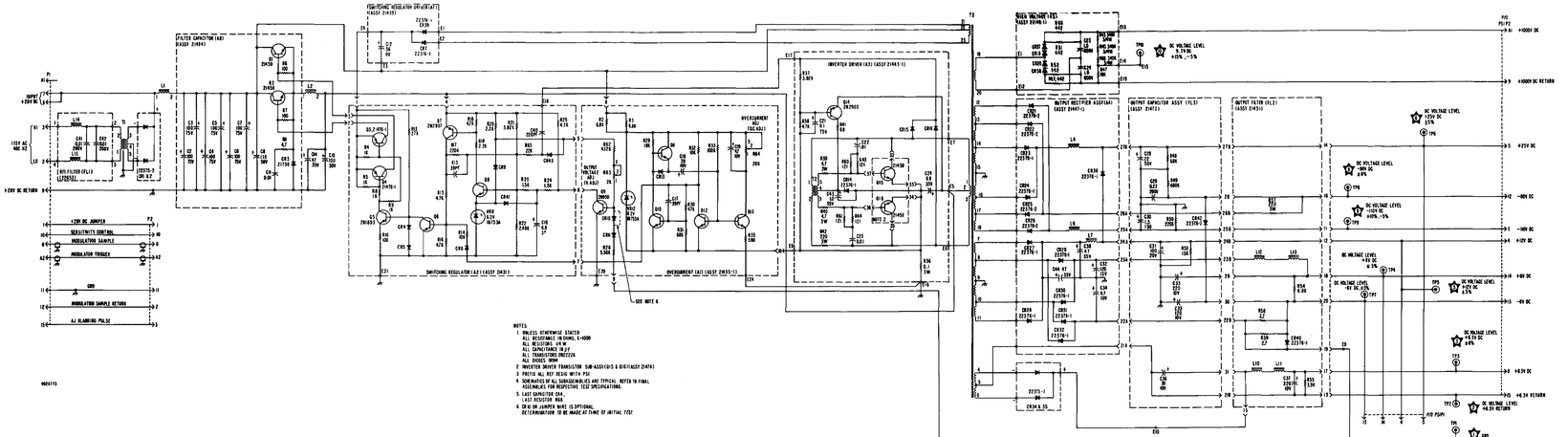
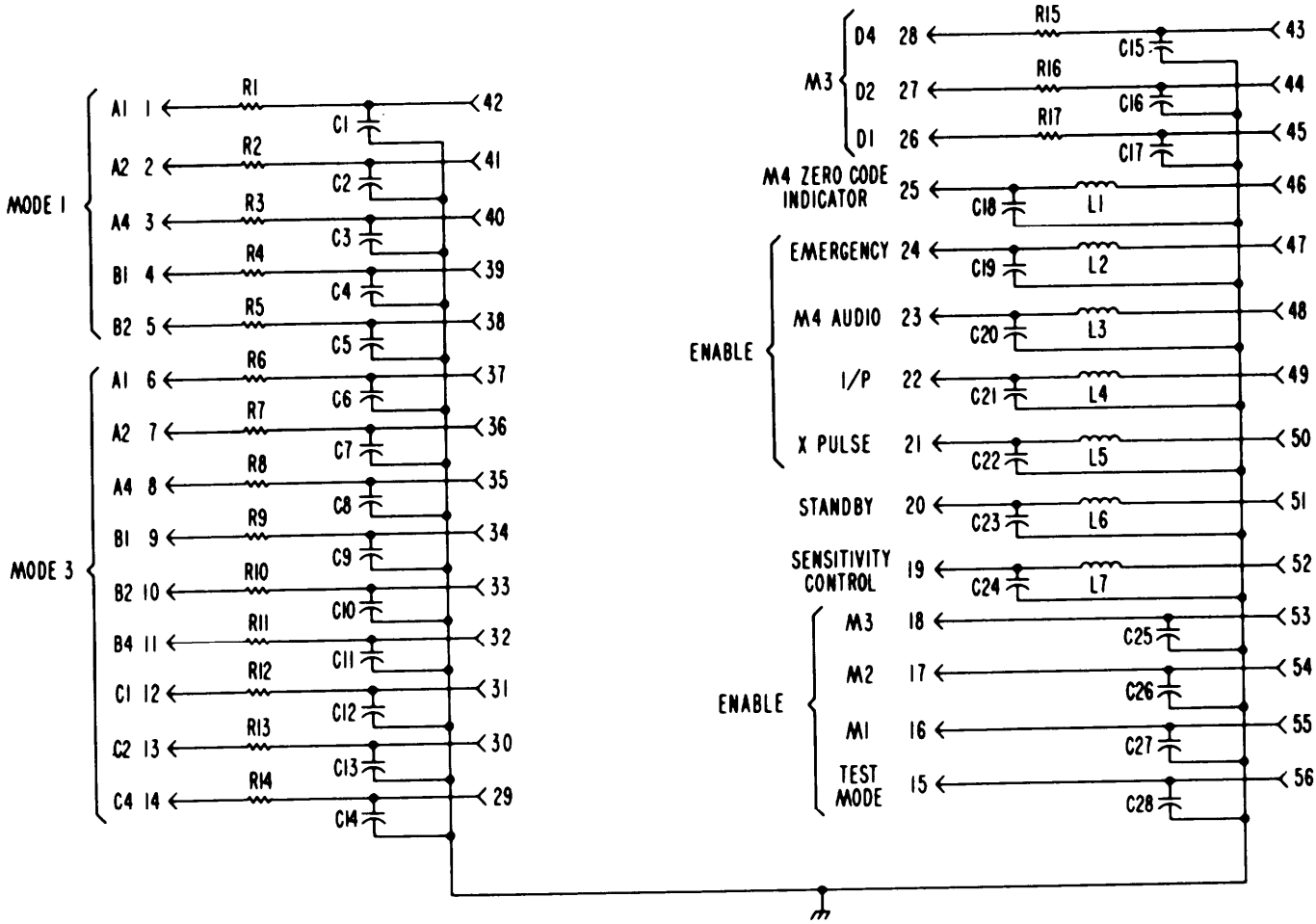


Figure 6-17. Power Supply (PS1), Schematic Diagram



4023612 B

Figure 6-18. Filter FL1, Schematic Diagram

NOTES

1. CAUTION: DO NOT INSTALL RT-859/APX-72 UNIT IN AN/APX-64 INSTALLATIONS UNTIL EXTERNAL COMPUTER RESET TRIGGER COAXIAL CABLE (WIRE NO. 833A, REF DWG 1041/1082) HAS BEEN REMOVED FROM P1-49, CANNON DPJM-59C10-34S-A (NOTE 2). CONNECT JUMPER TO P1-49 AS DIRECTED IN NOTE 3.
2. POWER AND VIDEO CONTROL PLUG P1(AT INSTALLATION) MUST MATE WITH J1(AT RT-859/APX-72 RECEIVER/TRANSMITTER)
   AT RT-859/APX-72 RECEIVER/TRANSMITTER:
   BENDIX PART NO. 2004514-0102
   REF: ITT CANNON-DPJ-59C10-33P-B
   AT INSTALLATION:
   SUGGESTED: PLUG-ITT CANNON-DPJM-59C10-34S-A WITH GLEMAIR DPJ-( )HOOD SPLIT.
3. PRIME POWER CONNECTIONS
   3.1 TYPE I UTILIZATION; AC POWER, SINGLE PHASE, 115 VOLT, 380 TO 420 Hz, CATEGORY "B". CONNECT 115V BUS TO P1-5. THE RT-859 IS FUSED (FRONT PANEL, 115V-5A) TO PROTECT UNIT. THE AC RETURN, P1-1 MAY BE CONNECTED TO AIRFRAME GROUND OR RETURNED BALANCED AS AIRCRAFT POWER DISTRIBUTION SYSTEM REQUIRES. DC POWER, 28.0 VOLTS, CATEGORY "B" REQUIRED FOR POWER & CONTROL RELAYS OPERATION: 200 MA PLUS CAUTION LIGHT CURRENT (1 AMP MAXIMUM). CONNECT 28V BUS TO P1-2. THE RT-859 IS FUSED (FRONT PANEL, 28V-5A) TO PROTECT INSTALLATION. THERE IS NO CONNECTION TO COAX TERMINAL P1-49.
   3.2 TYPE II UTILIZATION; DC POWER, 28.0 VOLTS, CATEGORY "B". THERE IS NO CONNECTION TO P1-1&5, CONNECT 28VDC BUS TO P1-2. CONNECT A SHORTING JUMPER BETWEEN THE SHIELD AND CENTER PIN TERMINALS OF COAX TERMINAL P1-49 IN THE PLUG P1 ONLY, THIS JUMPER SHOULD NOT BE TAKEN THROUGH THE CABLE. THE RT-859 IS FUSED (FRONT PANEL, 28V-5A) TO PROTECT UNIT.
4. ANTENNA CONNECTION PLUG P5 TO MATE WITH J5 BENDIX 2053448-0701 (UG-680A EQUIVALENT) AND ACCEPT 50 OHM COAXIAL CABLE (AS RG-225A/U).
5. SHIELDED LINES CONNECTING TO THE FOLLOWING P1 COAXIAL TERMINALS TO BE RG-195A/U OR EQUIVALENT: P1-9,10,11,12,13,45,46,47,48&49.
6. AUXILIARY TRIGGER WILL BE CONNECTED IN SPECIAL INSTALLATION WHEN REQUIRED. UNLESS REQUIRED, NO CONNECTION TO P1-13 IS ALLOWED.
7. CONNECT TO AUDIO WARNING SIGNAL INPUT OF INTERCOMMUNICATIONS SET AT STATION OF CREW MEMBER RESPONSIBLE FOR IFF OPERATION. THE AUDIO SIGNAL IS ADJUSTABLE IN THE IFF RECEIVER/TRANSMITTER TO A LEVEL OF 0-3 VOLTS PEAK ACROSS A RESISTIVE LOAD OF 150 OHMS OR 0-5 VOLTS PEAK ACROSS A RESISTIVE LOAD OF 600 OHMS. OUTPUT IS BALANCED.
8. TO TACAN AND OTHER L BAND EQUIPMENTS.
9. AC RETURN FOR 115VAC SWITCHED AC FROM P1-7 TO BE CONNECTED TO SAME POINT AS AC RETURN FROM P1-1.
10. DC RETURN FOR 28VDC SWITCHED DC FROM P1-6 TO BE CONNECTED TO SAME POINT AS DC RETURN FROM P1-2.
11. INSTALLATION SHALL BE IN ACCORDANCE WITH SPECIFICATION MIL-I-8700.
12. AIRCRAFT WIRING SHALL BE IN ACCORDANCE WITH SPECIFICATION MIL-W-5088.
13. NOT USED.
14. COAXIAL CABLES SHALL BE IDENTIFIED BY A PERMANENT MARKING ON A NON-METALLIC BAND OR SLEEVE & THE SLEEVE ATTACHED ONE INCH FROM EACH CABLE PLUG.
15. SEGMENT LETTERS IN ADDITION TO THOSE SHOWN MAY BE USED AS NECESSARY.
16. THE BLOCK OF NUMBERS ASSIGNED FOR USE WITH THE AN/APX-72 IS APX 72-1 THROUGH APX 72-47. THE HIGHEST NUMBER USED IS APX 72-47.
17. WIRE CODING FOR PANEL LIGHTING WIRES SHALL BE ASSIGNED BY THE INSTALLING ACTIVITY. IN NEW AIRCRAFT THIS WILL BE AS SEGMENTS OF THE PANEL LIGHTING CIRCUIT USING LETTER "L" PER SPECIFICATION MIL-W-5088. FOR OLD AIRCRAFT THIS WILL BE AS SEGMENTS OF THE EXISTING CODING ON WIRES AT POINT OF TIE-IN.
18. INFORMATION CONTAINED ON THIS DRAWING IS IDENTICAL TO THAT ON SIGNAL CORPS DRAWING NO. ES-J-18150.

CONNECTION TABLE FOR RT-859/APX-72			
P1 CONNECTION	SYSTEM OPERATING VOLTAGE	CONDUCTED CURRENT AMPERES	MAXIMUM ALLOWABLE VOLTAGE DROP
1	AC RET.(GRD)	0.728 MAX*	0.25
2	28VDC	3.8 MAX*	0.1
3	GRD	3.0	0.1
5	115VAC	0.728 MAX*	0.25
6	28VDC	1.0 MAX	N/A
7	115VAC	1.0 MAX	N/A
14	RETURN	0.002 MAX	0.1
20	RETURN	0.116	0.1
34	28VDC	0.1 MAX	N/A
53	28VDC	1.0 MAX	N/A
ALL MODE C CONTROL LINES FROM CPU-66/A	30VDC	0.0025 MAX	0.1
ALL REMAINING CONTROL AND ENABLE LINES	12VDC	0.0015 MAX	0.1

* EXCLUDES CURRENT REQUIRED FOR EXTERNAL LOADS.

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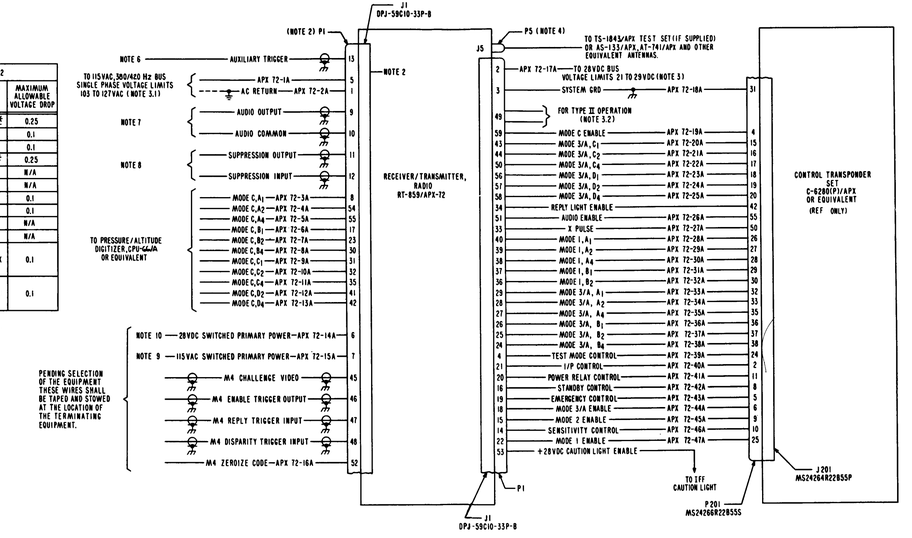


Figure 6-20. Transponder System, External Wiring Diagram

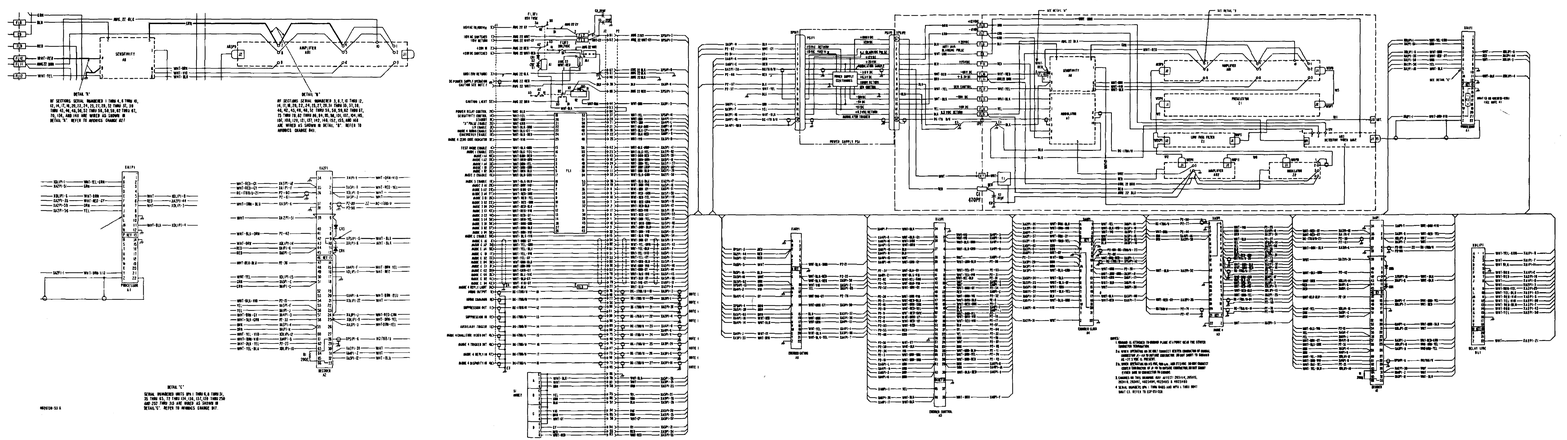


Figure 6-21. Receiver-Transmitter, Radio RT-859/APX-72, Wiring Diagram

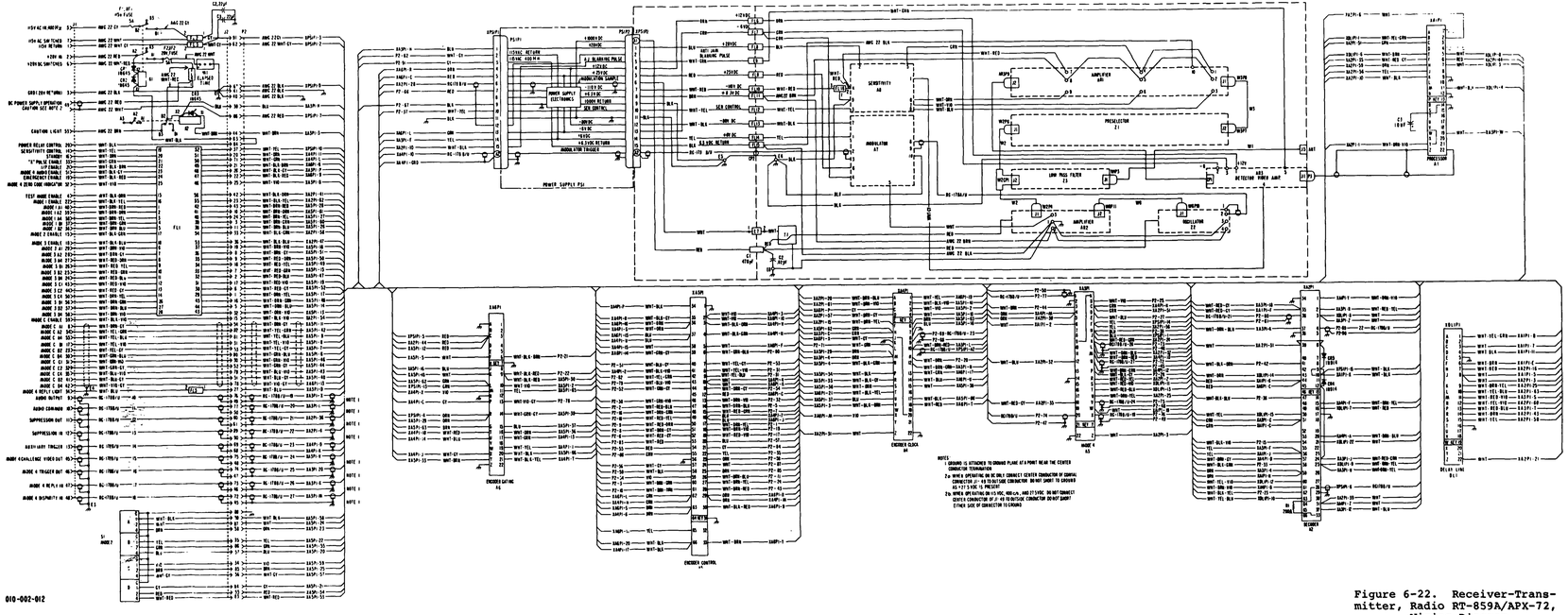
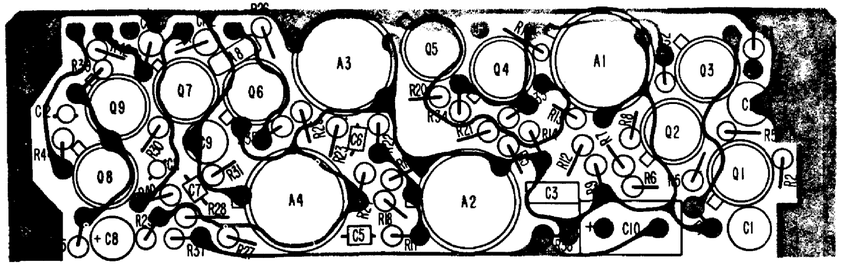


Figure 6-22. Receiver-Transmitter, Radio RT-859A/APX-72, Wiring Diagram



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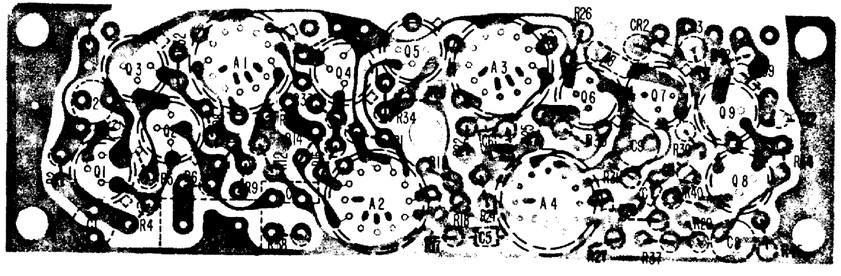
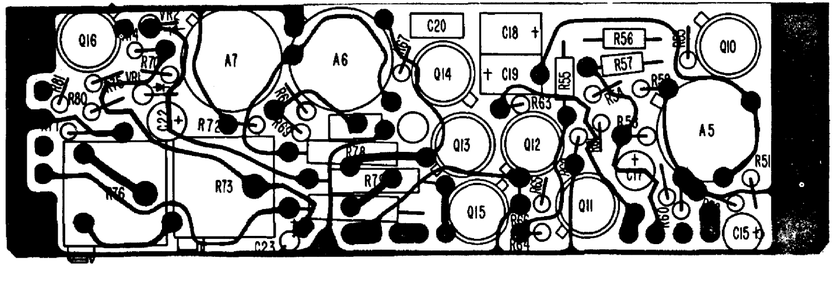




4026730-27

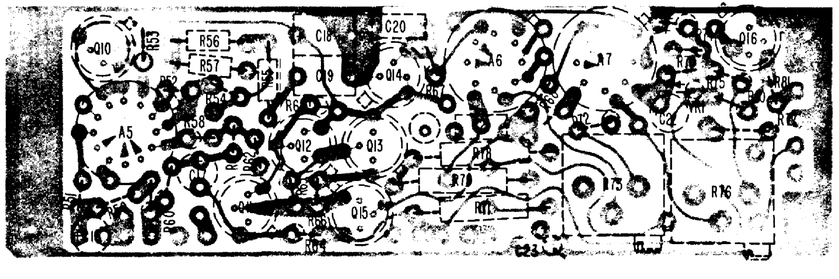
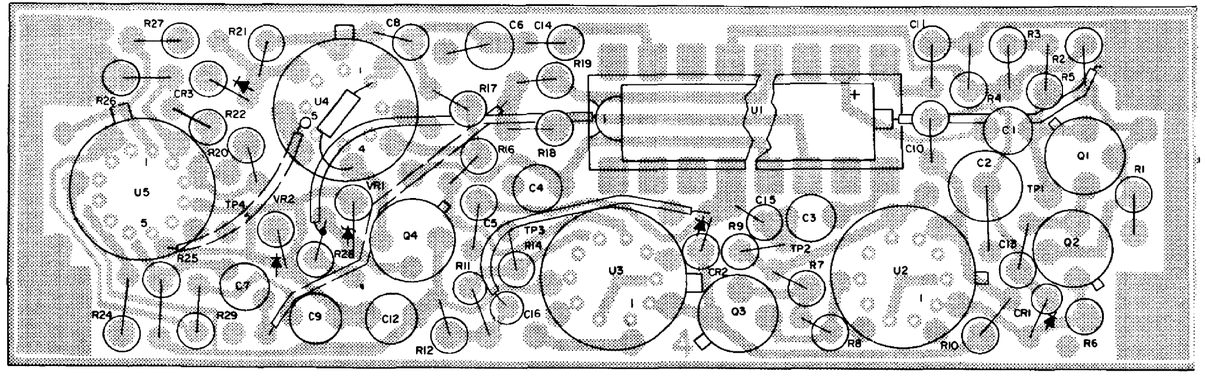


Figure 6-23. Detector and Video Amplifier (AR3), Part No. 4023409-0501, 0502, Wiring Diagram



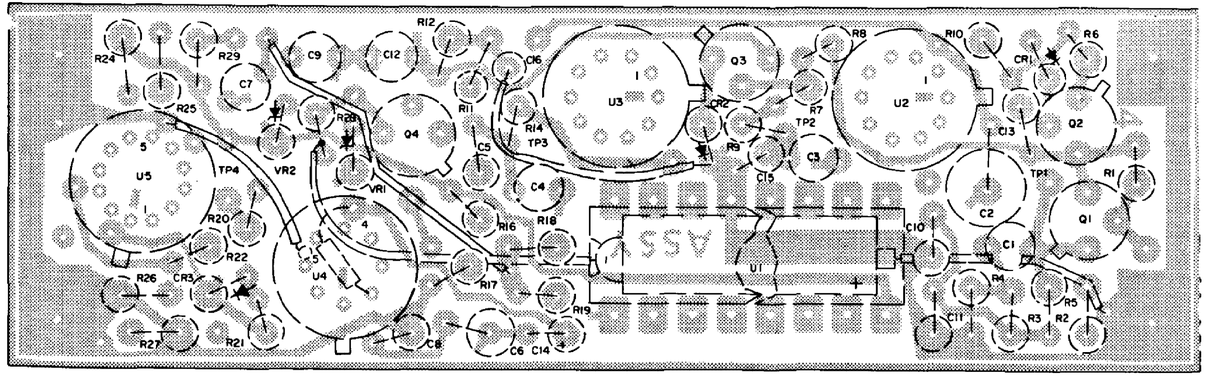


Figure 6-24. Detector and Video Amplifier (AR3), Part No. 4023409-0503, Wiring Diagram

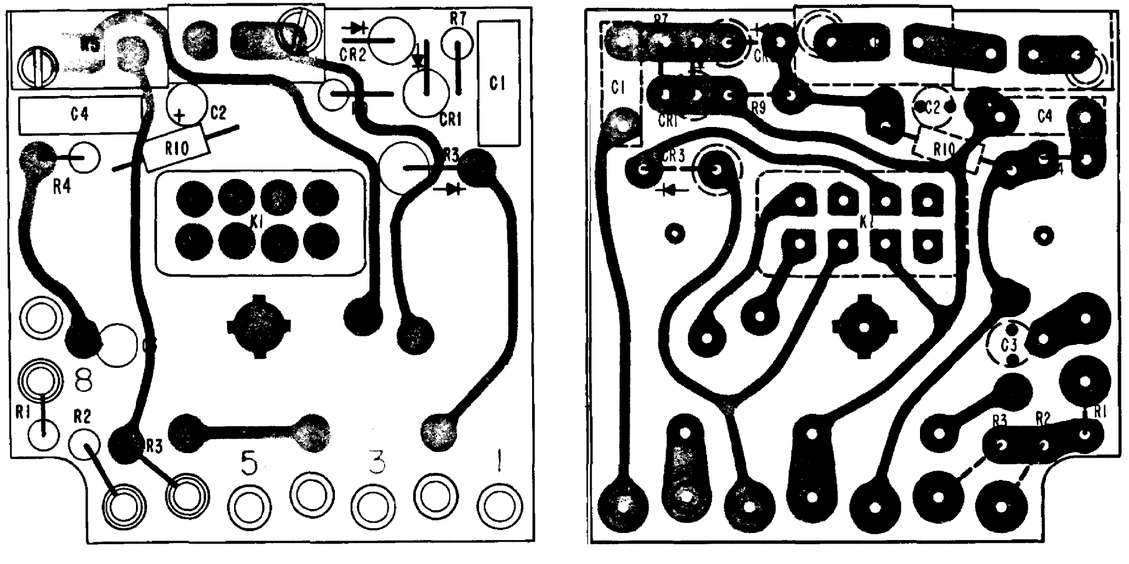


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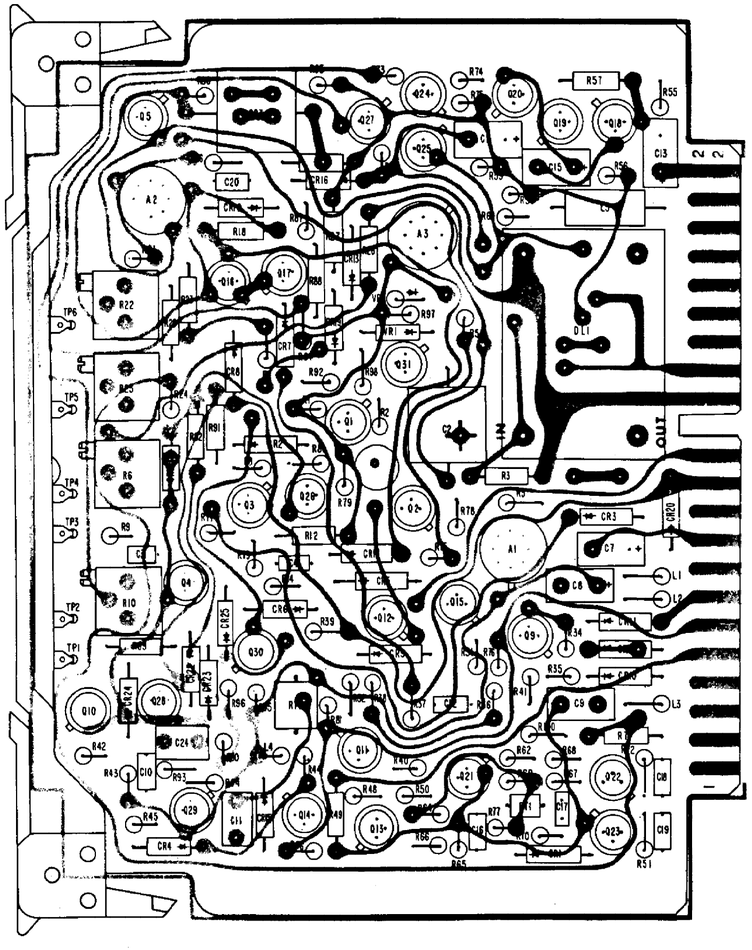
Figure 6-25. Sensitivity A8, Wiring Diagram



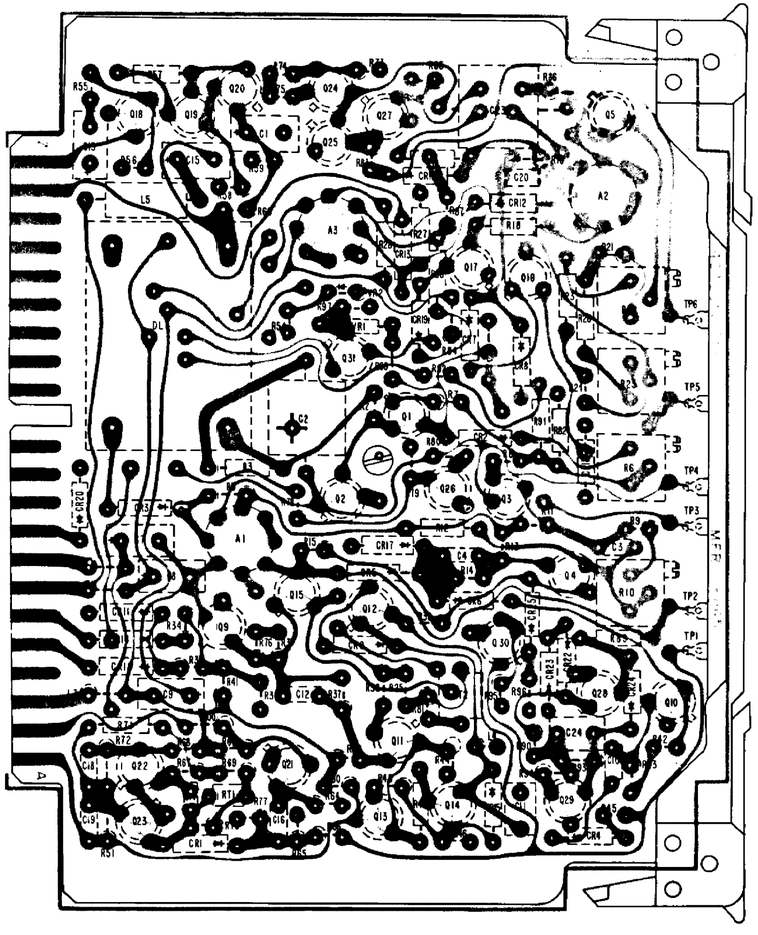


Figure 6-26. Processor (A1), Used With RT-859/APX-72, Wiring Diagram

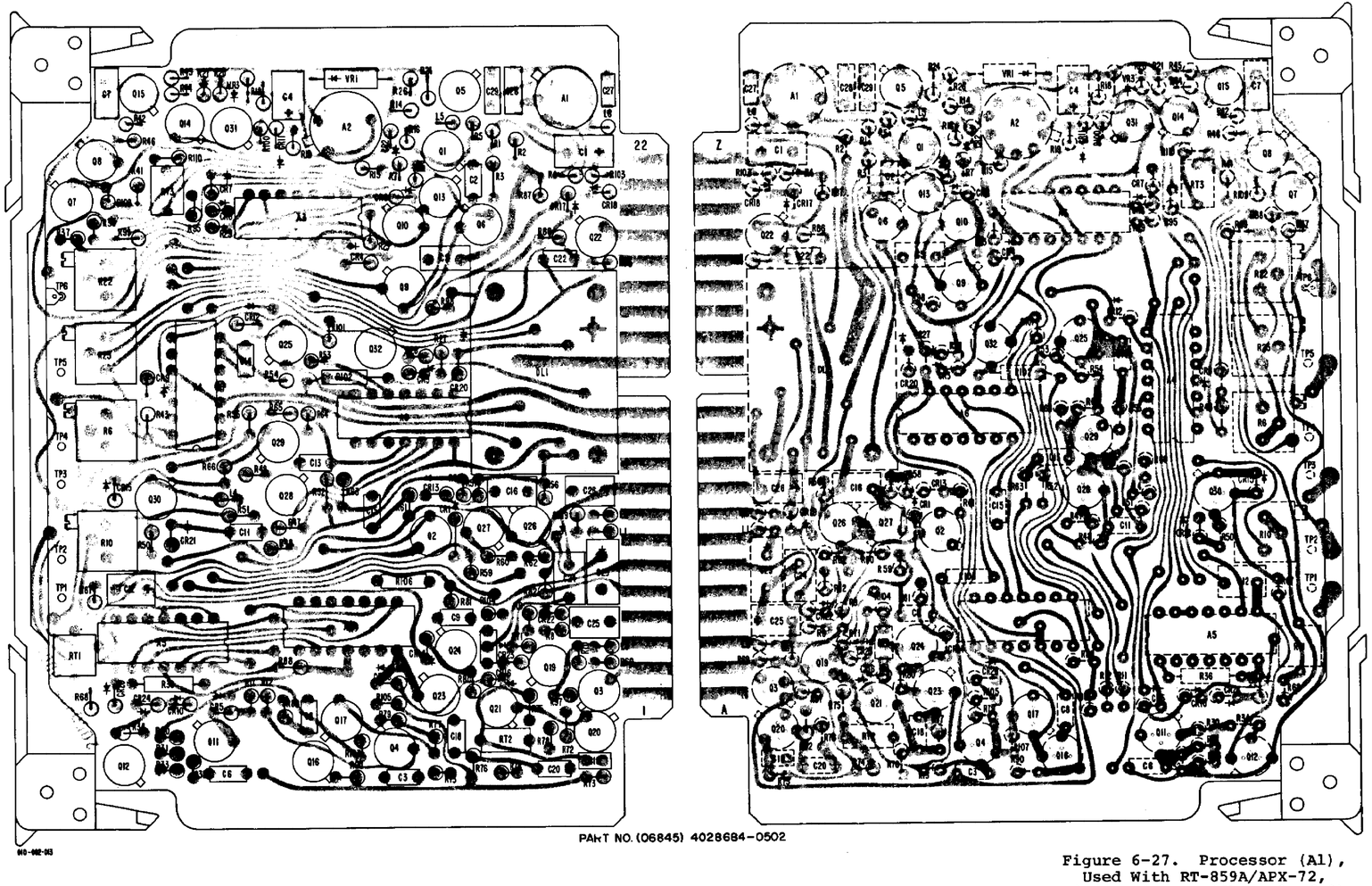


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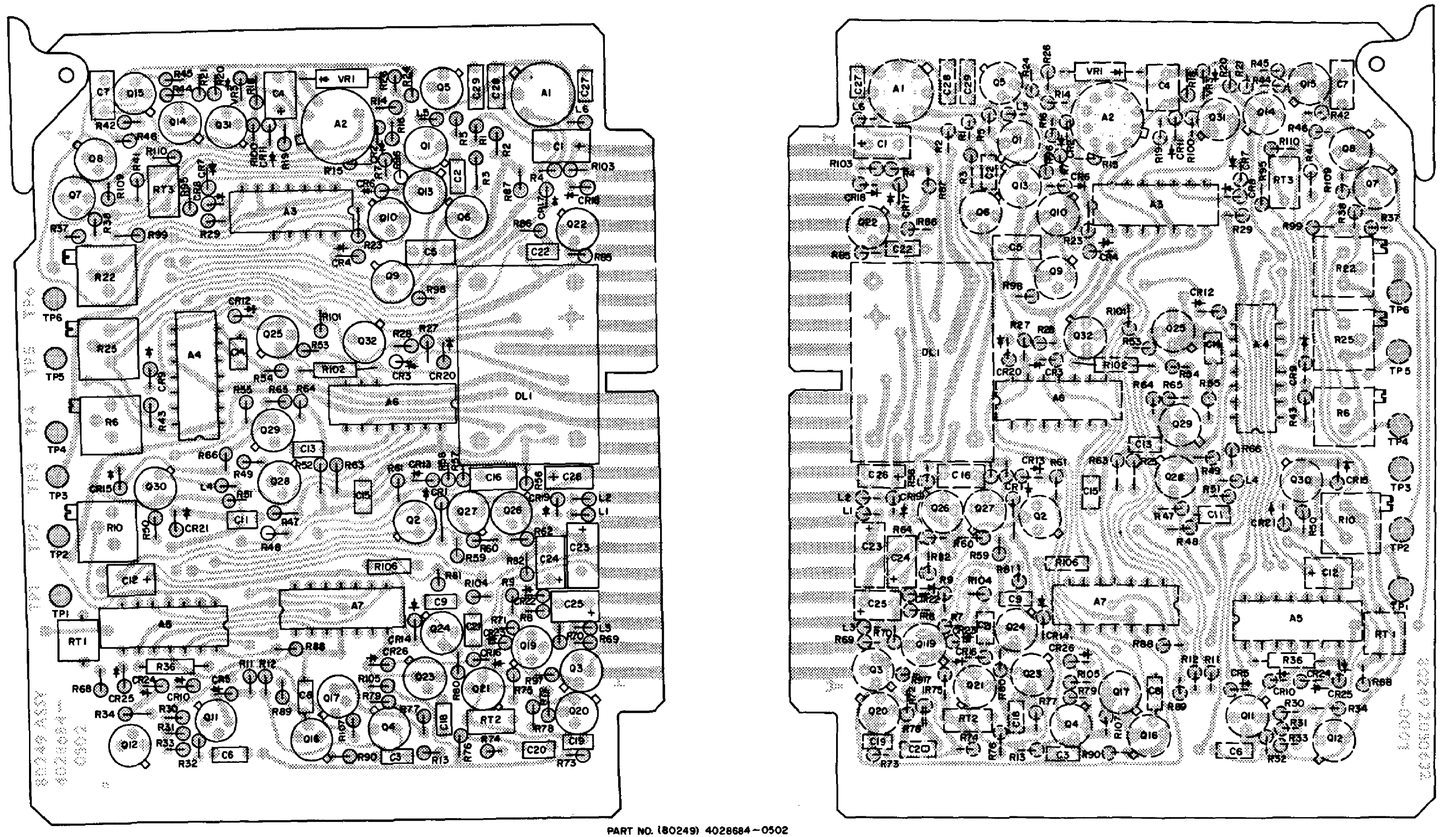
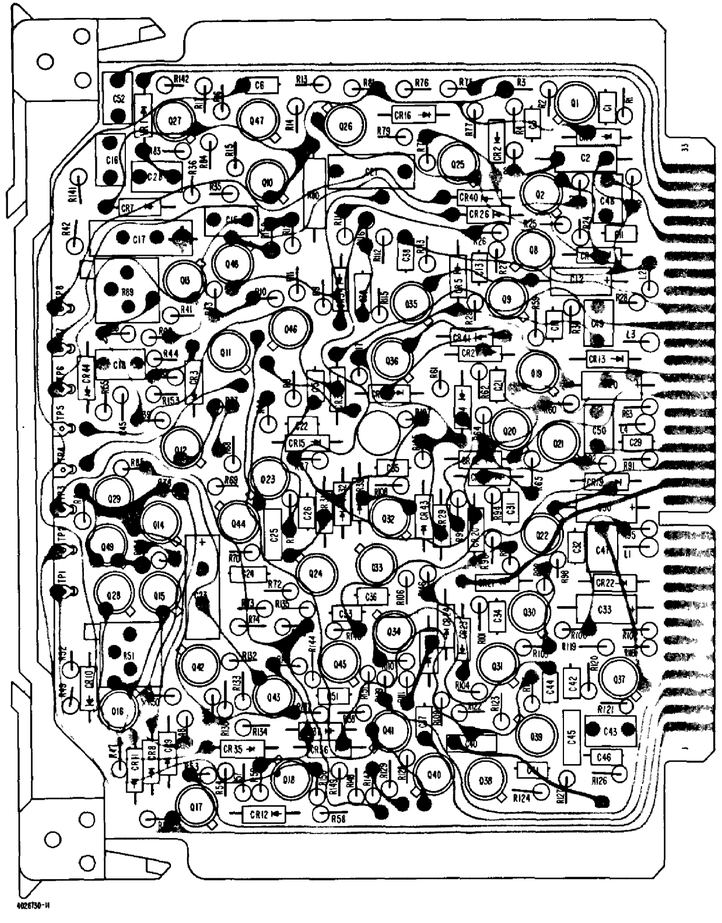
Figure 6-27. Processor (A1), Used With RT-859A/APX-72, Wiring Diagram (Sheet 1 of 2)



PART NO. (80249) 4028684-0502

Figure 6-27. Processor (A1), Used With RT-859A/APX-72, Wiring Diagram (Sheet 2 of 2)



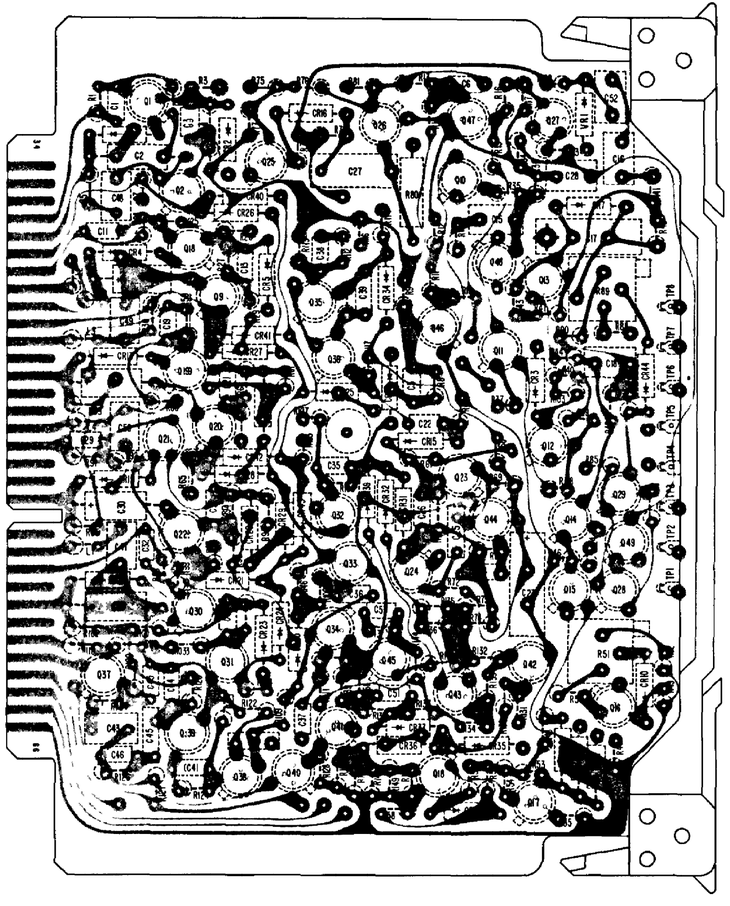


Figure 6-28. Decoder (A2), Used With RT-859/APX-72, Wiring Diagram

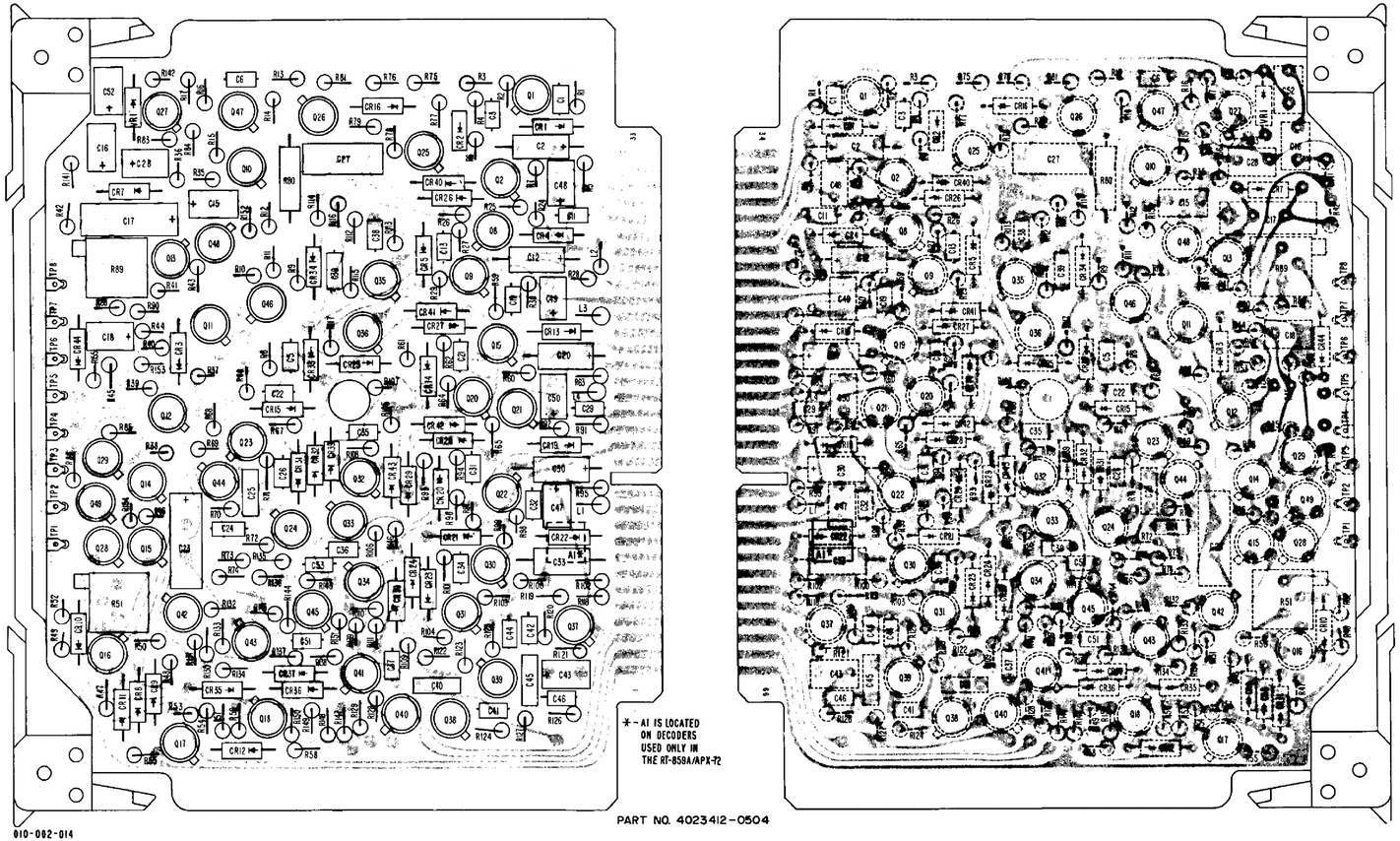
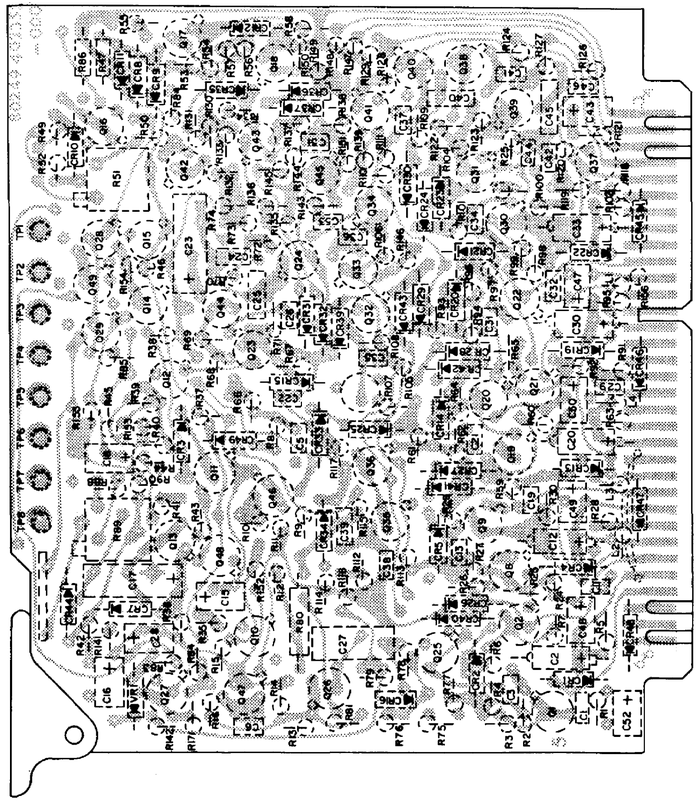


Figure 6-29. Decoder (A2), Used With RT-859A/APX-72, Wiring Diagram (Sheet 1 of 2)



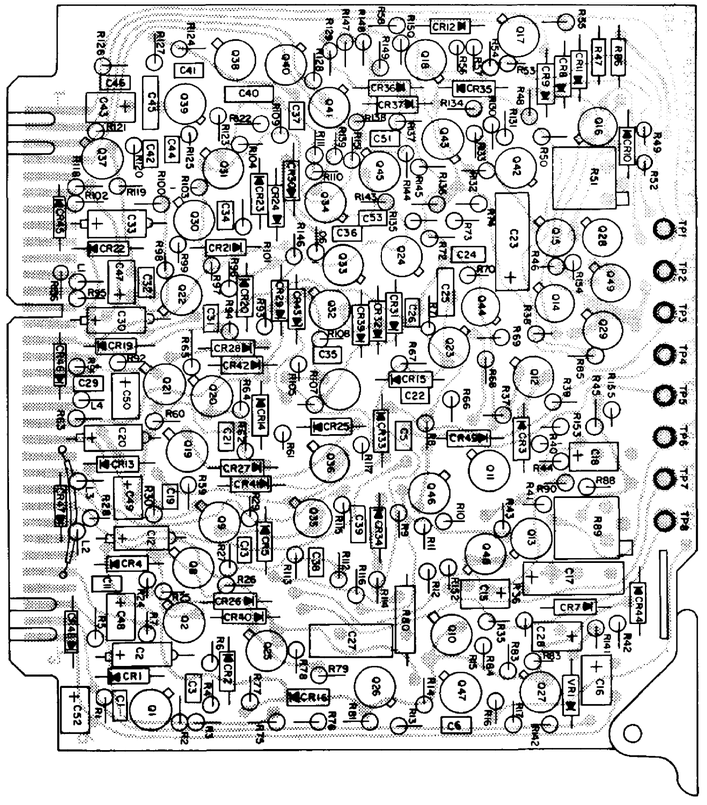


Figure 6-29. Decoder (A2), Used With RT-859A/APX-72, Wiring Diagram (Sheet 2 of 2)

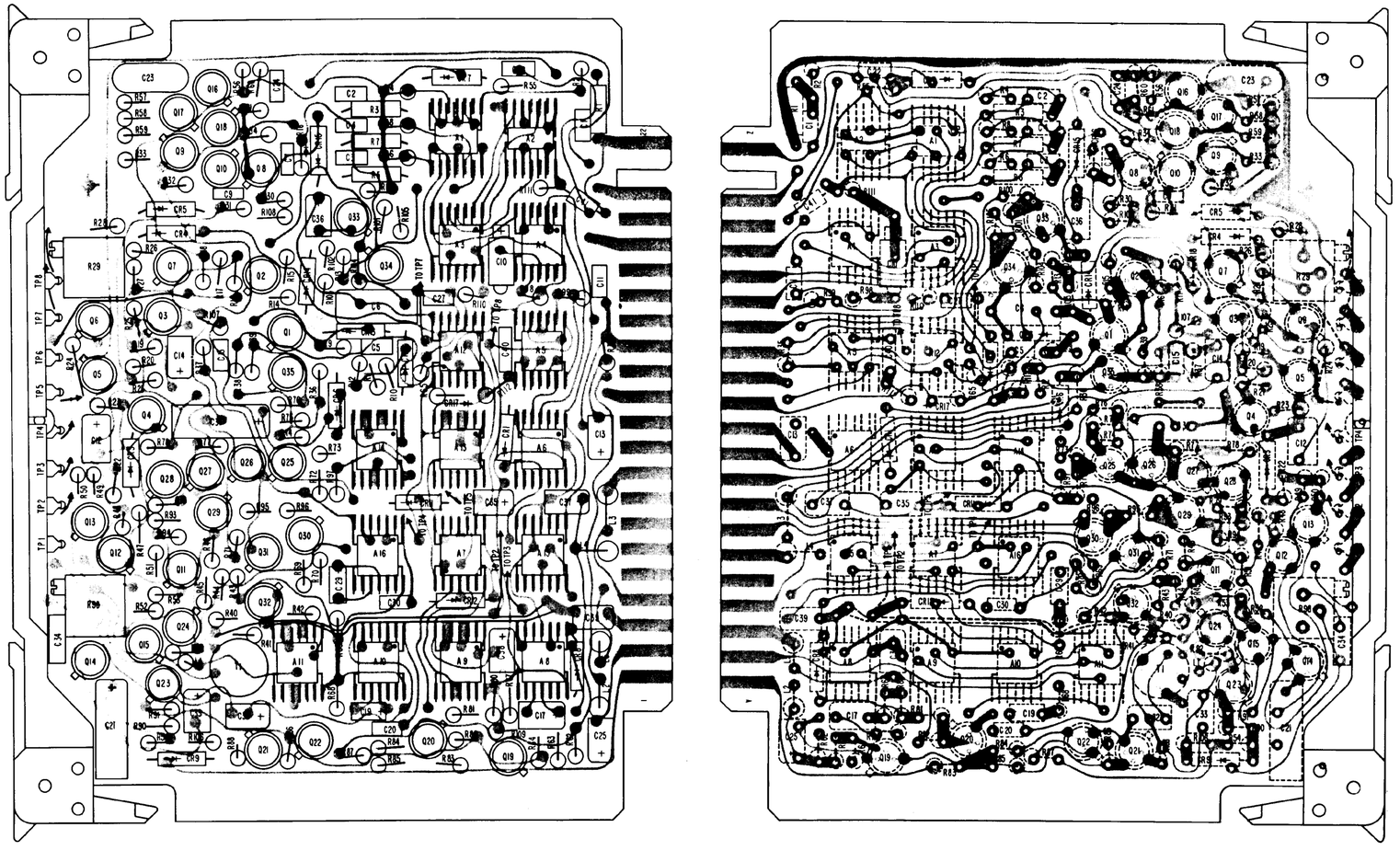
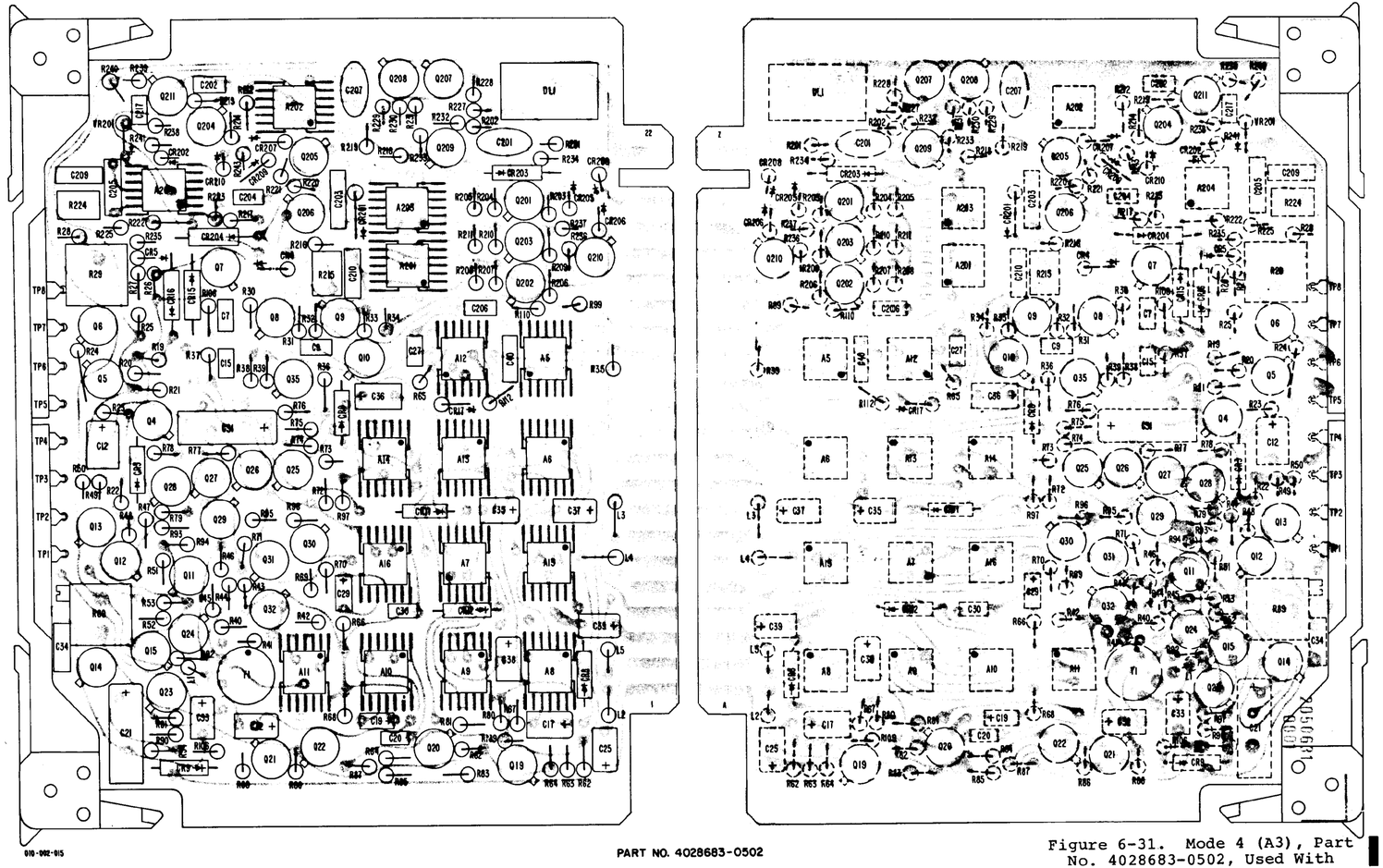
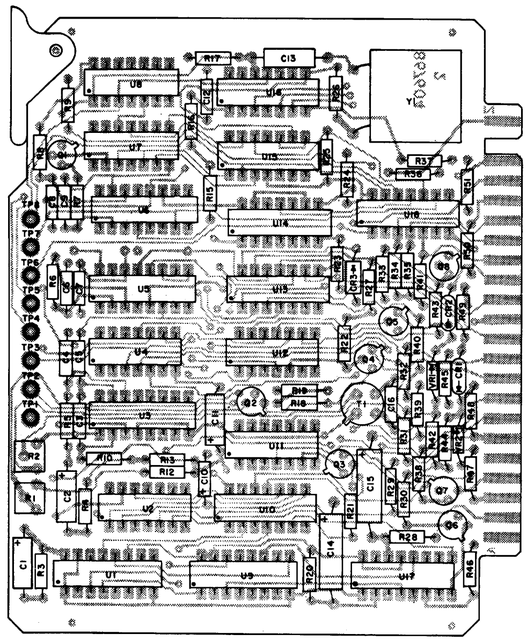


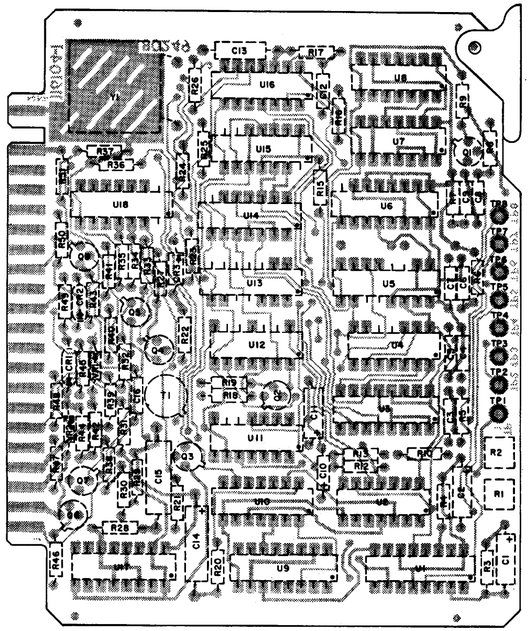
Figure 6-30. Mode 4 (A3), Used With RT-859/APX-72, Wiring Diagram



PART NO. 4028683-0502

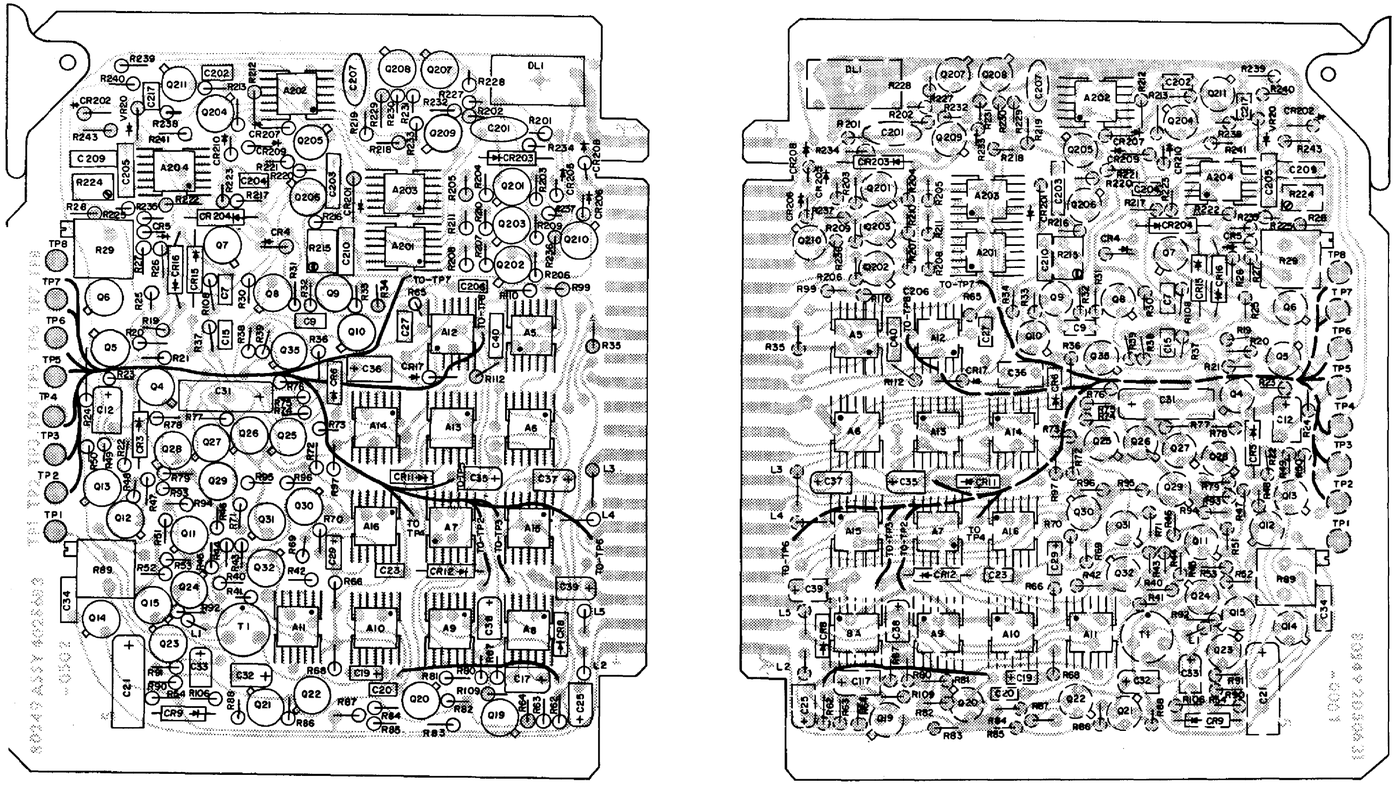
Figure 6-31. Mode 4 (A3), Part No. 4028683-0502, Used With RT-859A/APX-72, Wiring Diagram (Sheet 1 of 2)





PART NO. 116104-1

Figure 6-31A. Mode 4 (A3), Part No. 116104-1, Used With RT-895A/APX-72, Wiring Diagram



PART NO. (40249) 4028683-0502

Figure 6-31. Mode 4 (A3) Used With RT-859A/APX-72, Wiring Diagram (Sheet 2 of 2)

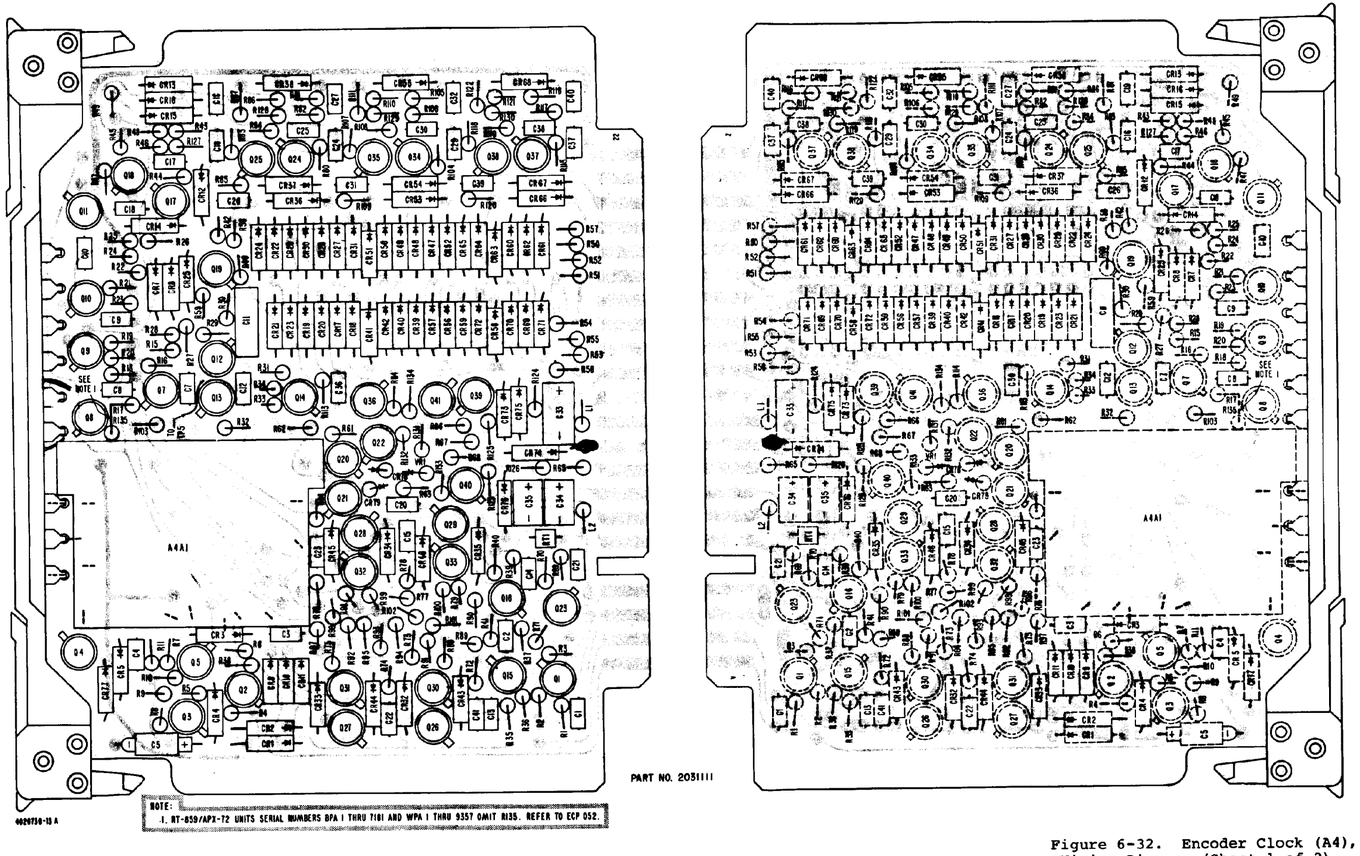
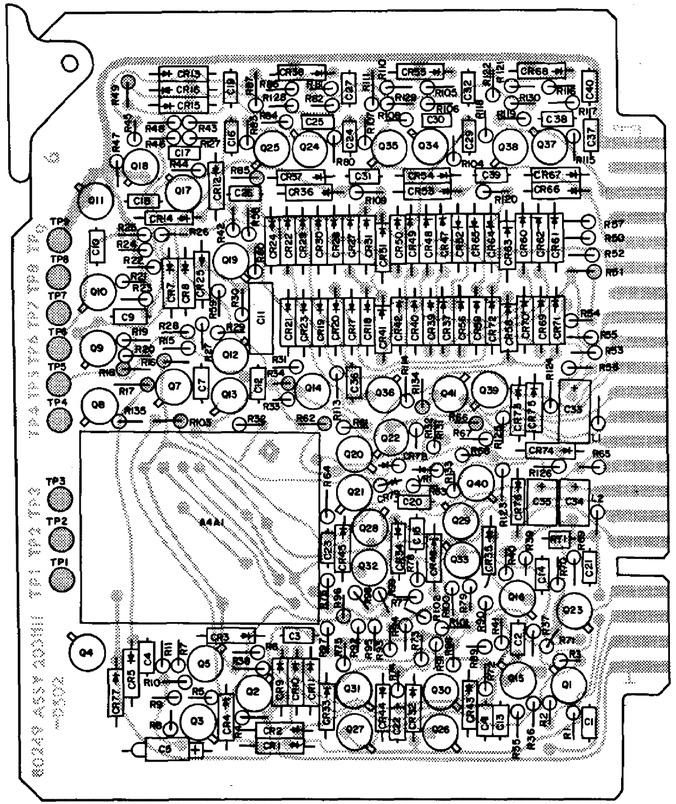


Figure 6-32. Encoder Clock (A4), Wiring Diagram (Sheet 1 of 2)



PART NO. (80249) 2031111

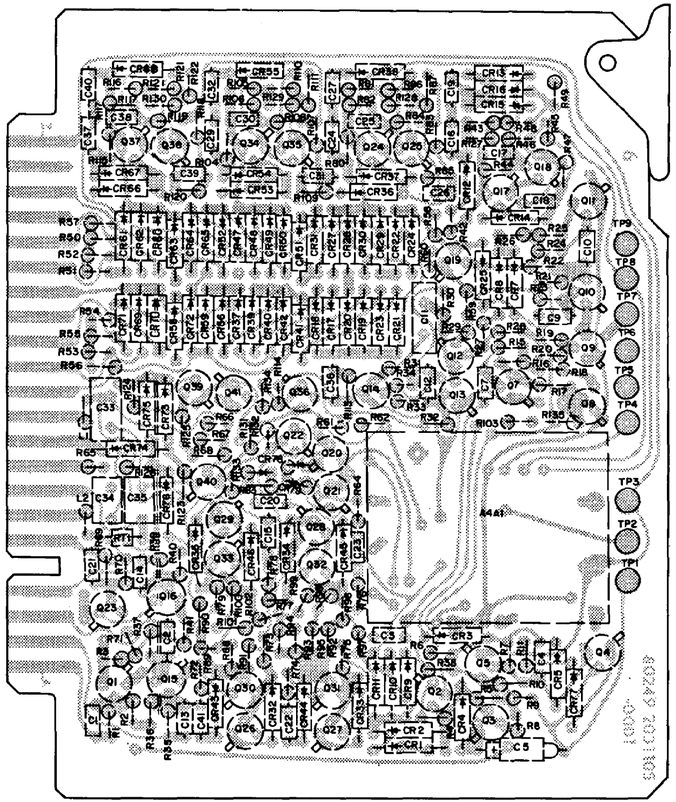
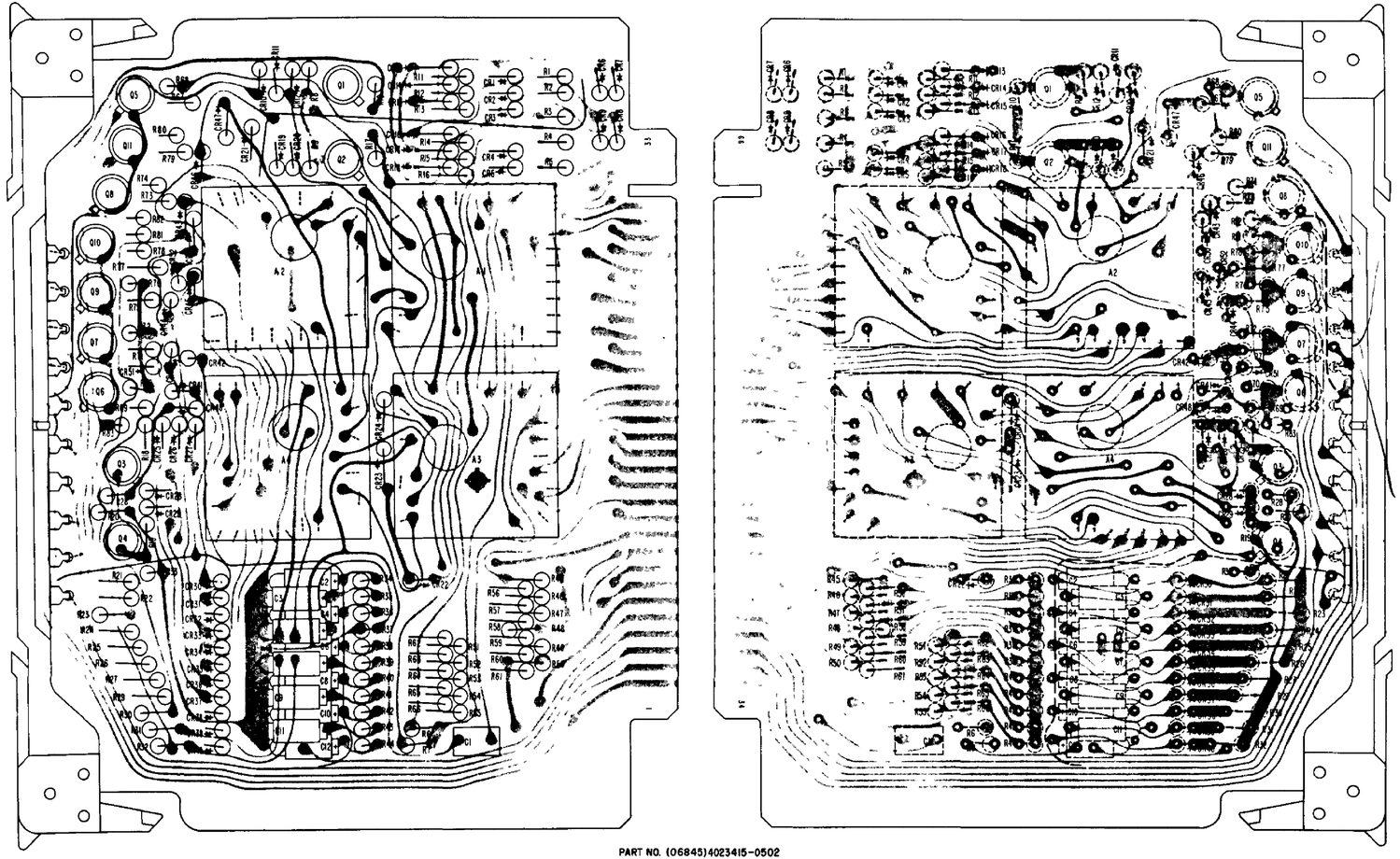


Figure 6-32. Encoder Clock (A4), Wiring Diagram (Sheet 2 of 2)



PART NO. (06845)4023415-0502

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Figure 6-33. Encoder Control (A5), Wiring Diagram (Sheet 1 of 2)

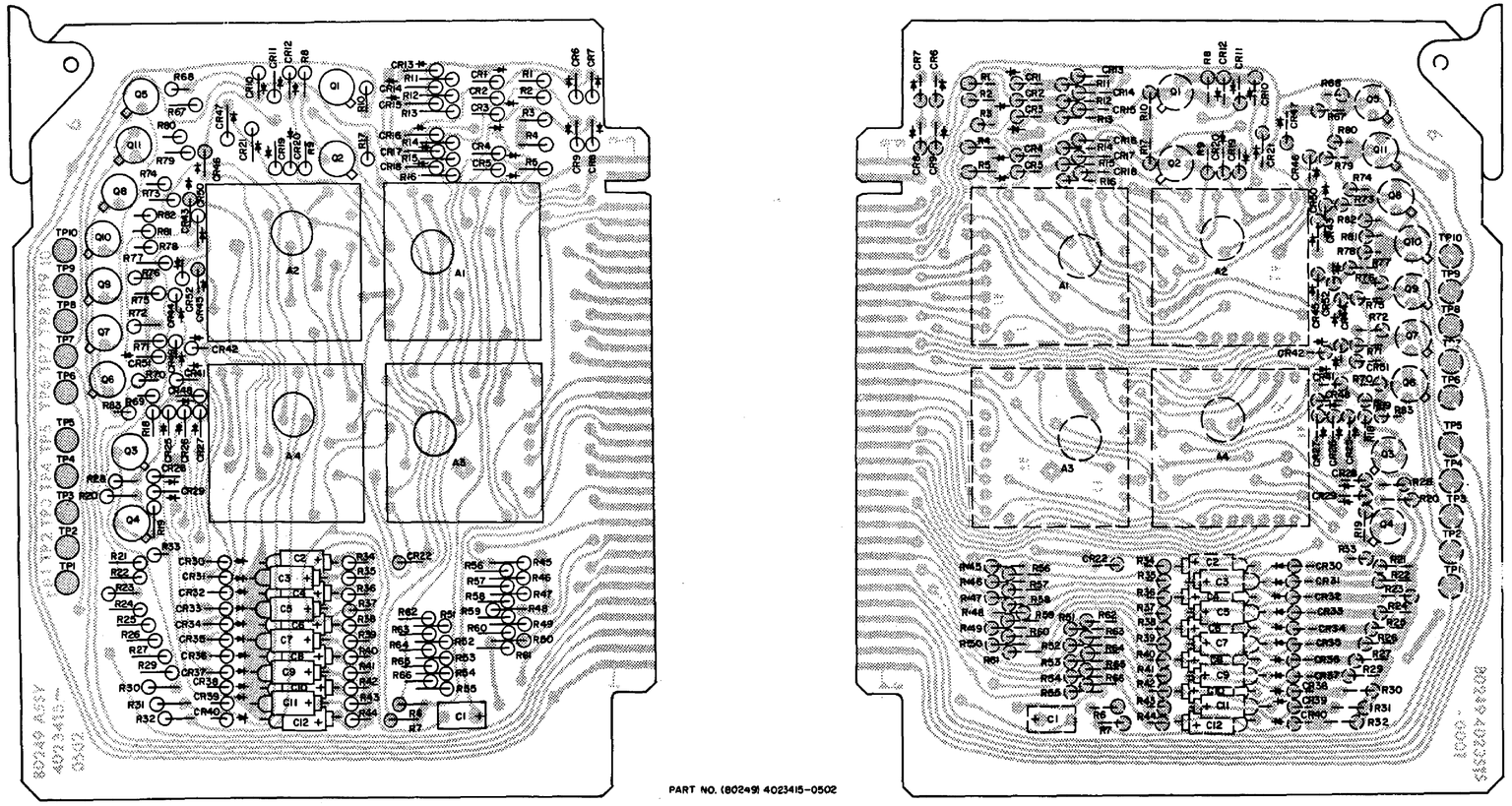
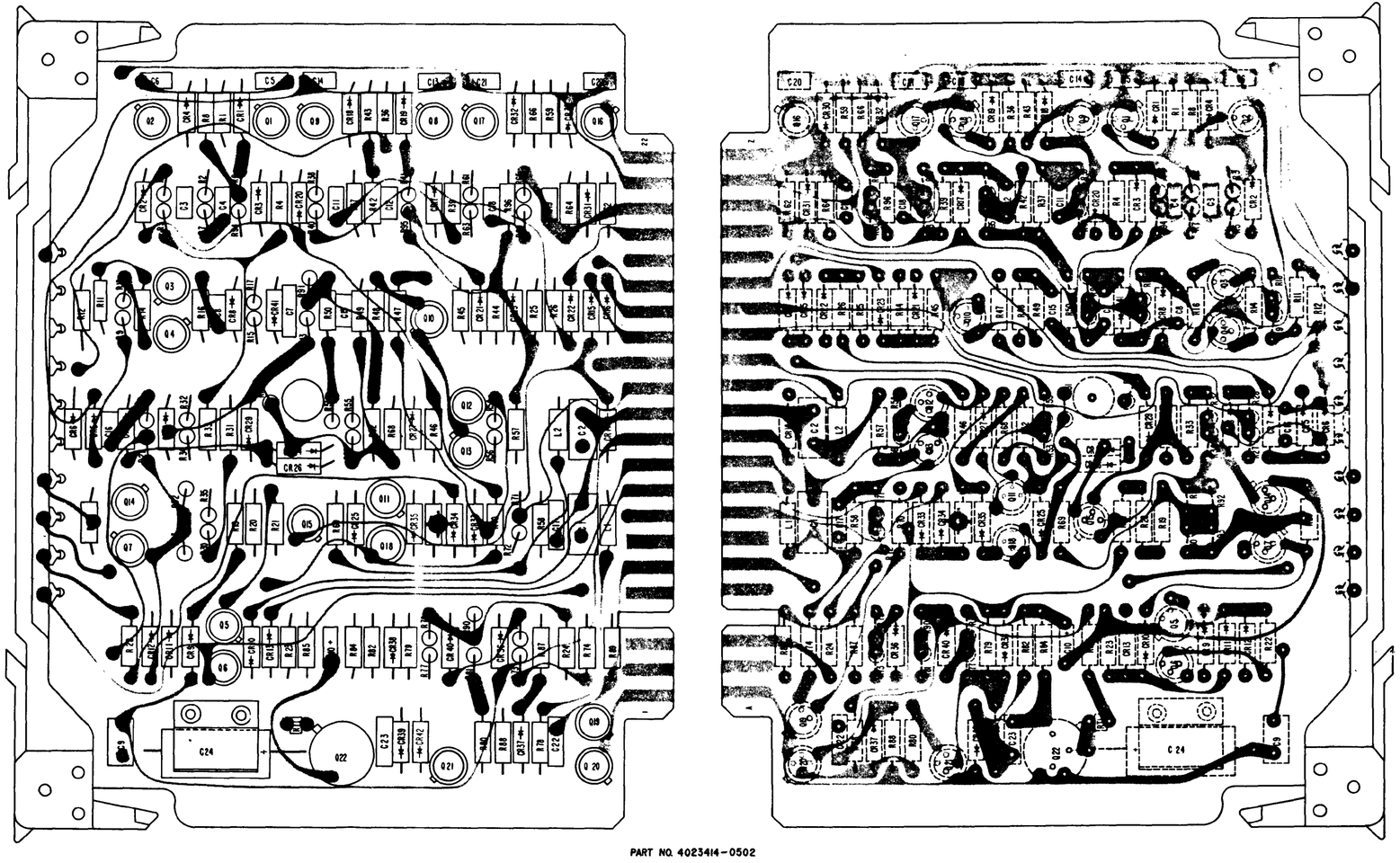


Figure 6-33. Encoder Control (A5), Wiring Diagram (Sheet 2 of 2)



PART NO. 4023414-0502

Figure 6-34. Encoder Gating (A6), Wiring Diagram (Sheet 1 of 2)

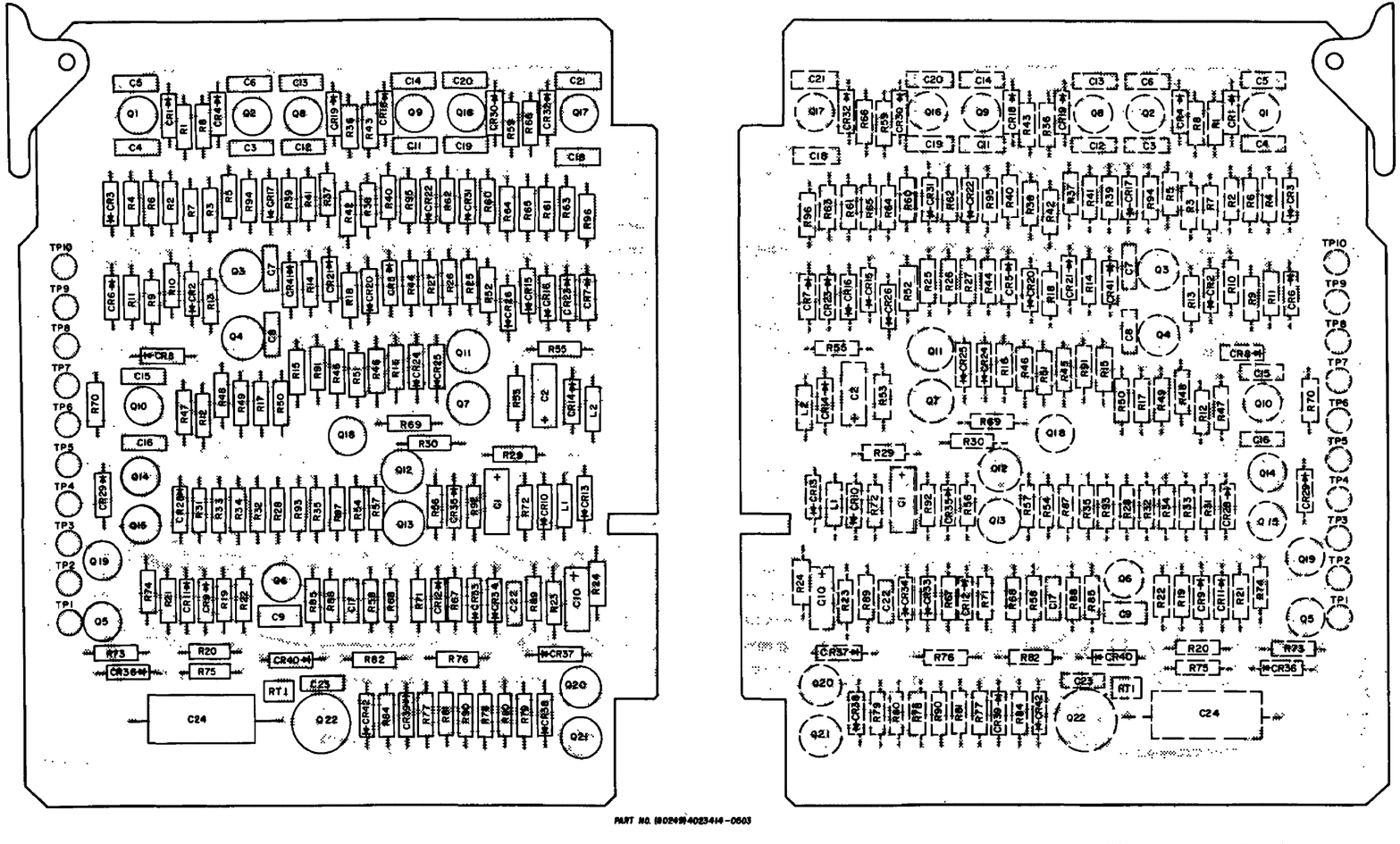


Figure 6-34. Encoder Gating (A6), Wiring Diagram (Sheet 2 of 2)

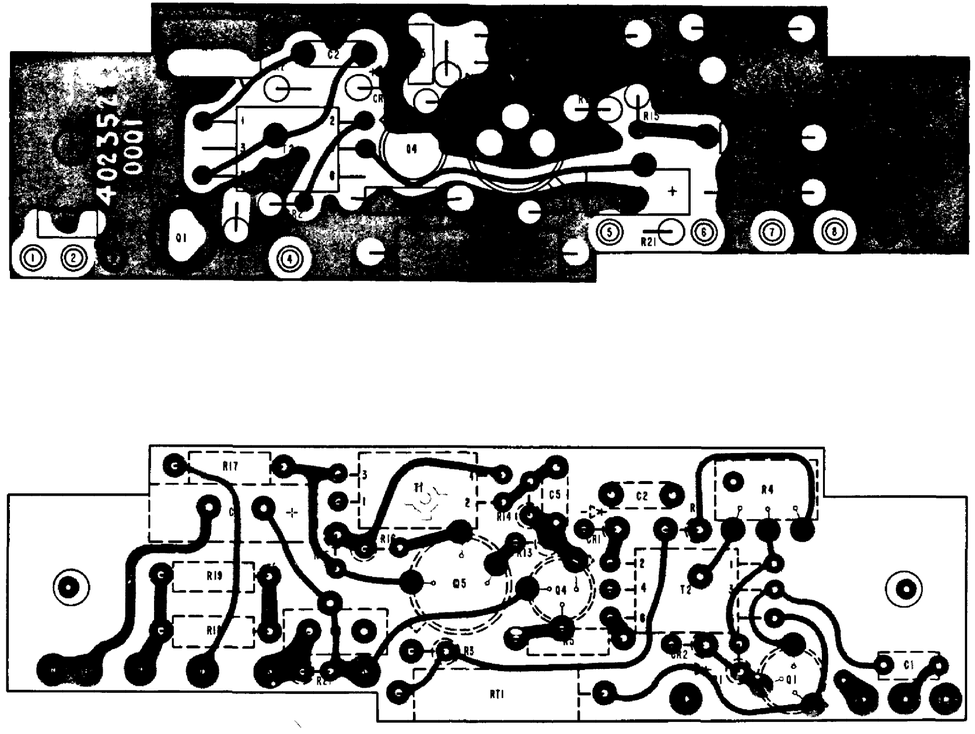


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Figure 6-35. Modulator (A7), Wiring Diagram

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ALPHABETICAL INDEX (Cont)

ALPHABETICAL INDEX (Cont)

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2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

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